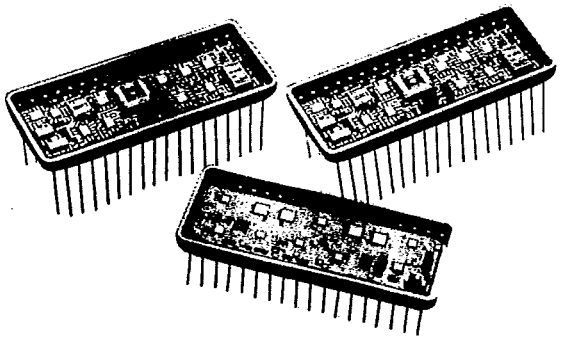
HYBRID TWO-SPEED TRACKING CONVERTER
Resolution to 20 Bits; Any Speed Ratio



DESCRIPTION

The HSDC-360 is an application of the hybrid control transformer and data processor modules in the HSDC-14 to form a two-speed tracking converter. A circuit diagram with a list of discrete components is provided so that a crossover detector and other required circuit elements can be added to two standard hybrid control transformer modules and one standard data processor module. The additional components and their interconnections determine the speed ratio and resolution of the converter. The circuit for a 1 and 36 speed converter with 16 bit output is described in the data sheet; circuit diagrams for other speed ratios and resolutions will be supplied on request.

The HSDC-360 has most of the characteristics listed in the description of the HSDC-14, including ratiometric conversion, phase sensitive detection, broadband inputs, and DC analog velocity output. The power supply voltage ranges are the same, and the −15V power supply can also be eliminated with a trade-off reduction in the maximum tracking rate.

The accuracy of the HSDC-360 depends on the speed ratio and resolution, and on whether standard or high-accuracy control transformers are used. For a 16 bit, 1 and 36 speed converter the accuracy can be as high as ±1.2 LSB, including the ±1 LSB quantizing error.

APPLICATIONS

The HSDC-360 may be used wherever analog angle data from a two-speed synchro or resolver system must be converted rapidly and accurately to digital form for transmission, storage, or analysis. Because of the small size, low weight, low power requirement, and high MTBF of its hybrid components, the HSDC-360 is well suited for remotely located and hard to access equipment. All hybrid modules are processed to MIL-STD-883 (burn-in is optional), and can be used in the most stringent industrial and military ground or avionics applications. Designed for printed circuit board mounting by standard techniques, the HSDC-14 can be readily incorporated into other equipment for computer control.

FEATURES

- *THREE STANDARD HYBRID MODULES PLUS DISCRETE COMPONENTS WIRED BY CUSTOMER TO DETERMINE SPEED RATIO AND RESOLUTION*
- *SIGNAL AND REF. INPUTS:*
  Internal solid state isolation or external isolation transformers
  All common synchro and resolver L-L voltage levels and frequencies
- *LOGIC:*
  TTL and CMOS compatible
  Up to 20 bit parallel binary angle output
  Converter Busy and Inhibit
- *POWER REQUIRED:*
  ±15V DC and logic voltage supply

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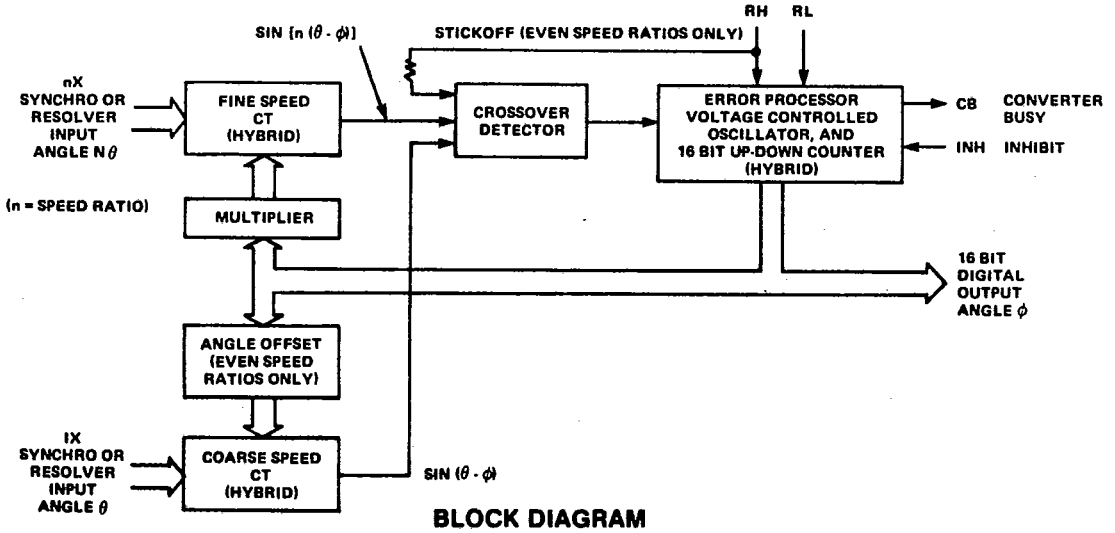
*Patented



BLOCK DIAGRAM

SPECIFICATIONS

Apply over reference amplitude, temperature, and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 to 20 bits
ACCURACY	
Depends on Speed Ratio, Resolution and Whether Option "a" (±2 min) Is Used	$\frac{\pm 4 \text{ min (or 2 min)}}{\text{speed ratio}}$ ±0.9 LSB
Accuracy For 1:36 Speed Ratio and 16 Bit Resolution	±0.45 min with standard CT ±0.39 min with high accuracy CT
SPEED RATIO	Any speed ratio can be accommodated by an appropriate multiplier and angle offset made with discrete components. Consult factory for circuit diagram.
SIGNAL AND REFERENCE INPUT	
SOLID STATE BUFFER INPUT (HSCT AND HRCT UNITS)	
Carrier Frequency Range	47 – 1000 Hz
Synchro and Resolver Input Characteristics	
Voltage Options and Minimum Input Impedance (Balanced)	

Synchro (HSCT)	Z_{IN} Line to Line	Z_{IN} Each Line to Gnd
90V L-L (Option H)	130 KΩ	85 KΩ
11.8V L-L (Option L)	17.5 KΩ	11.5 KΩ

Resolver (HRCT)	Z_{IN} Single Ended	Z_{IN} Differential	Z_{IN} Each Line to Gnd
90V L-L (Option H)	175 KΩ	350 KΩ	175 KΩ
26V L-L (Option M)	50 KΩ	100 KΩ	50 KΩ
11.8V L-L (Option L)	23 KΩ	46 KΩ	23 KΩ

Common Mode Range (DC Common Mode Plus Recurrent AC Peak)

	$-V_S = 0V$	$V_L = +6.2V$ and $-V_S = -7V$
90V L-L (Option H)	150V max	300V max
26V L-L (Option M)	45V max	90V max
11.8V L-L (Option L)	20V max	60V max

VOLTAGE FOLLOWER INPUT (FOR HXCT UNITS)	
Carrier Frequency Range	47 – 1000 Hz
Voltage Range	
$-V_S = 0V$	1V rms nominal; 1.15V max; 0.1V min
$V_L = +6.2$ and $-V_S = -7V$	3V rms nominal; 3.5V max; 0.1V min
Max Voltage Without Damage	15V rms continuous 100V peak transient
Input Impedance	Z_{IN} > 10 MΩ (transient protected voltage follower)

TRANSFORMER CHARACTERISTICS (FOR HXCT UNITS)	
400 Hz TRANSFORMERS	
Reference Transformer (Optional for Both Solid State and Transformer Input Options)	
Carrier Frequency Range	Option 4 = 360 – 1000 Hz
Voltage Range	18 – 130V
Input Impedance	40 KΩ min
Breakdown Voltage to GND	1200V peak
Signal Transformer	
Carrier Frequency Range	Option 4 - 360 – 1000 Hz
Minimum Input Impedances (Balanced)	

	Synchro Z_{IN} (Z_{SO})	Resolver Z_{IN}
90V L-L (Option 4H)	180 KΩ	100 KΩ
26V L-L (Option 4M)	–	30 KΩ
11.8V L-L (Option 4L)	20 KΩ	30 KΩ
Breakdown Voltage to GND	700V peak	

PARAMETER	VALUE
60 Hz TRANSFORMERS	
Reference Transformer (Optional for Both Solid State and Voltage Follower Input Options)	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	80 – 138V rms; 115V rms nominal
Input Impedance	600 KΩ min, resistive
Input Common Mode Voltage	±500V rms, transformer isolated
Output Description	+R (in phase with RH-RL) and -R (in phase with RL-RH) derived from op-amps. Short circuit proof.
Output Voltage	3.0V nominal riding on DC reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15V supplies.
Signal Transformer	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	10 – 100V rms; L-L 90V rms L-L nominal
Input Impedance	148 KΩ min L-L balanced resistive
Input Common Mode Voltage	±500V rms, transformer isolated
Output Description	Resolver output ±sine (±S) and ±cosine (–C) derived from op-amps. Short circuit proof
Output Voltage	1.0V rms nominal riding on DC reference V. Output voltage level tracks input level.
Power Required	4 mA type 7 mA max from +15V supply
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/DTL/CMOS compatible, depending on logic supply voltage
Outputs	
14 Parallel Data Bits	Natural binary angle positive logic
Converter Busy (CB)	1.5 – 3μs positive pulse, leading edge initiates counter update
Drive Capability	2 or 4 standard TTL loads
Inhibit Input (INH)	Z_{IN} > 80 KΩ pull-up resistor to V_M (V_M = logic supply voltage or ±15 supply voltage. See Interconnection Diagrams.)
ANALOG OUTPUTS	
Internal D.C. Ref. (V)	+3.9 VDC nominal
AC Error Voltage (θ)	0.38 mV rms per LSB of error
DC Error Voltage (E)	--1 VDC per ± LSB of error
DC Velocity Voltage (θ)	
For 16 Bit Resolution	+1.0V DC per +112°/sec at 400 Hz +1.0V DC per +28 °/sec at 60 Hz
For Higher Resolutions	Scales according to number of bits. At 400 HZ for instance, a 1.0V DC θ output corresponds to 28 /sec at 16 bits and 7°/sec at 20 bits.
DYNAMIC CHARACTERISTICS	
Input Rate For Full Accuracy	
For 16 Bit Resolution	
At 400 Hz	0 to ·2.5 rps min
At 60 Hz	0 to ±0.625 rps min
For Higher Resolutions	Maximum input rate scales according to number of bits: 1/4 at 18 bits, and 1/16 at 20 bits.
Velocity Constant	$K_V = \infty$ (No limitation with Type II servo loop)
Acceleration Constant	
At 400 Hz	K_a = 58,000 sec^{-2} nominal
At 60 Hz	K_a = 3,600 sec^{-2} nominal
Settling Time	
For Normal Tracking	No lag error up to specified input rates
For 179° Step Change with 1:36 Speed Ratio	
At 400 Hz	270 msec typ to 1 LSB 350 msec max to final value
At 60 Hz	1080 msec typ to 1 LSB 1400 msec max to final value
For 179 Step Change With Other Speed Ratio	Consult factory. Depends on slew rate and small signal settling time.

TECHNICAL INFORMATION

T-71-35-03

INTRODUCTION

The applications information for the HSDC-360 has much in common with that for the HSDC-14, since the same control transformer and data processor modules are used. The HSDC-14 data sheet will be referenced frequently to avoid repeating information and diagrams.

The block diagram shows the main components of the HSDC-360. The multiplier, angle offset, stickoff resistor, and crossover detector are composed of discrete components.

The operation of a two-speed S/D is essentially the same as a single speed except there are two control transformers (CT) which generate two error voltages. These two CTs are fed by a common up-down counter with the counter data multiplied by the speed ratio for the fine speed CT.

Assuming an off-null condition, as when the system is first energized, the crossover detector feeds the coarse (1X) CT error signal output to the demodulator and error processor. The converter seeks a null as it would for a single speed S/D. As null is approached (to within 2.5° nominally) the coarse CT output drops below a preset threshold and the crossover detector then switches the fine speed CT error signal into the demodulator and error processor. Since the counter angle θ is multiplied by the speed ratio, the gradient of the fine speed CT is n times the coarse (1X) CT output. The servo loop then is able to seek an even finer null, using the fine speed CT error signal. The converter will continue to use the fine error signal for continuous tracking, swtiching back to the coarse signal only when the coarse error exceeds the crossover threshold. An angle offset and stickoff voltage are introduced in the coarse channel for even speed ratios in order to eliminate the false stable nulls which can occur when the fine and coarse speed angles are simultaneously at 180°.

MODULE INTERCONNECTIONS

A circuit diagram and list of components for a 16 bit 1:36 speed converter are given to illustrate the most common resolution and speed ratio. Interconnection layout is not critical. The analog outputs are derived from op-amps, have low output impedance, and are short circuit proof.

The output drive capability can be either 2 or 4 standard TTL loads as indicated in the Notes. The penalty for 4 TTL load capability is that the Inhibit input, which is internally connected to V_M by an 80 KΩ pull-up resistor, will be referenced to the +15V supply rather than to the logic supply voltage.

SIGNAL AND REFERENCE INPUTS AND TRANSFORMERS

All information listed under this section heading in the HSDC-14 data applies. Note especially the protective voltage suppressors that must be installed on all 90V L-L solid state input modules to prevent voltage transients from destroying the input resistor networks.

LOGIC INPUTS AND OUTPUTS

Logic outputs consist of 16 to 20 parallel data bits and a Converter Busy (CB). These outputs are short circuit proof to ground or to positive voltages as high as V_L.

Information about the Inhibit (INH) is given in the corresponding section of the HSDC-14 data.

ANALOG OUTPUTS

The analog outputs are V, e, E, and θ. V is an internal D.C. ground, +3.9V DC nominal, and is used as reference ground with the voltage follower buffer input option (HXDC). The other analog outputs, which ride on the D.C. reference V, are not used externally in normal operation.

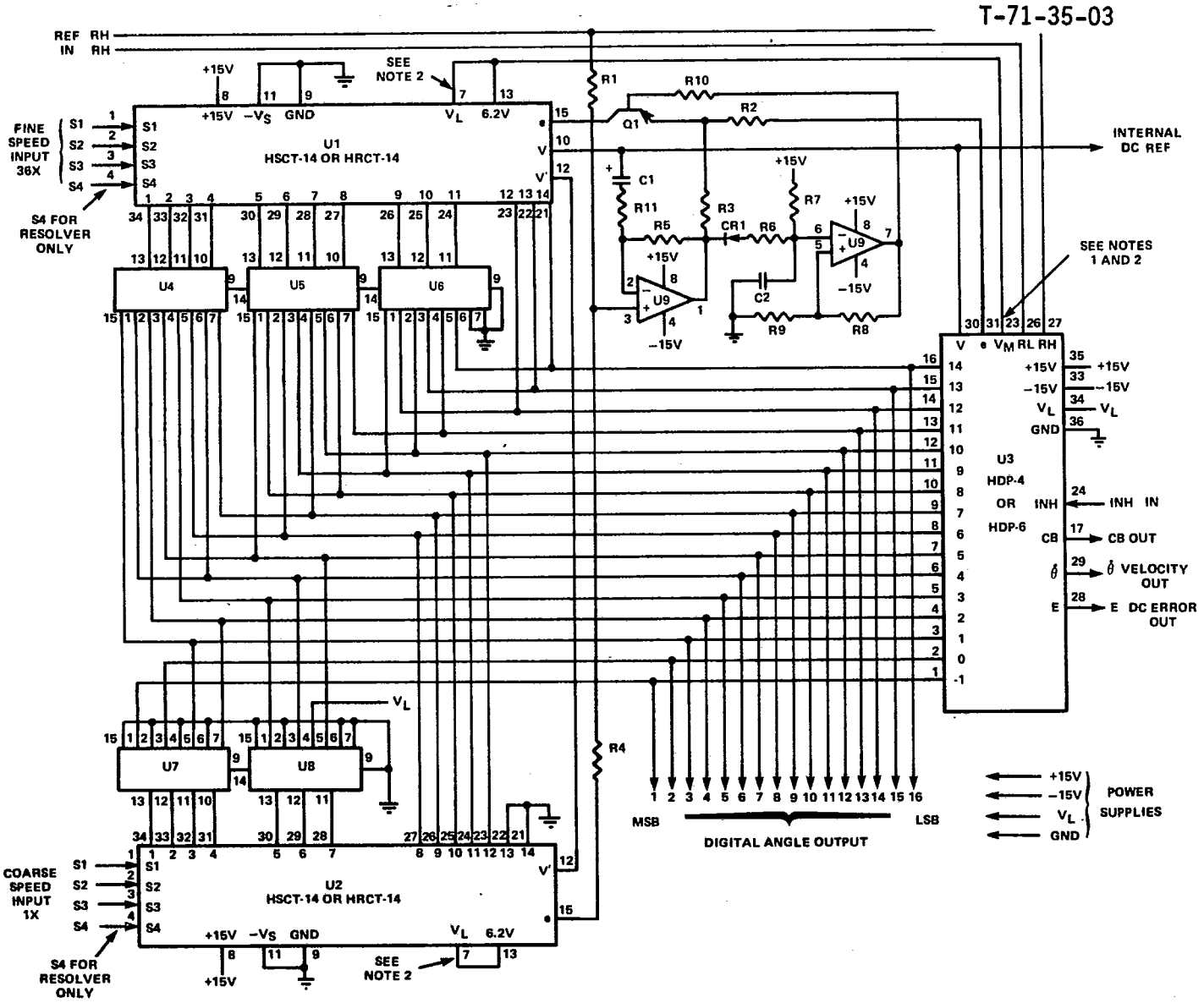
The HSDC-14 data sheet describes the characteristics of the analog outputs e, E, and $\dot{\theta}$. The only difference for the HSDC-360 is the scaling for the velocity output $\dot{\theta}$. This scaling is given in the HSDC-360 specifications table.

TIMING AND DYNAMIC PERFORMANCE

The discussion and diagrams in the HSDC-14 data sheet concerning timing and dynamic performance apply to the HSDC-360 without modification.

CIRCUIT DIAGRAM FOR 16 BIT, 1:36 SPEED CONVERTER

T-71-35-03



NOTES:

1. Digital output drive capability is normally 2 standard TTL loads. If logic supply V_L = +5V for TTL interface and 4 unit load capability is desired, disconnect pin 23 (V_M) on U3 from 6.2V and connect it to +15V. Note that the Inhibit logic 1 is referred to V_M.

2. If the external logic supply voltage V_L is greater than 6.2V, do not connect pins 7 (V_L) on U1, U2 and pin 23 (V_M) on U3 to 6.2V. Instead, connect these three pins to the external logic supply V_L.

3. If signal isolation transformers are required, use HXCT-14 for U1, U2. See Interconnection Diagram in HSDC-14 data sheet for signal and reference transformer connections.

PARTS LIST:

U1, U2 = DDC hybrid control Transformers } See ordering
U3 = DDC hybrid data processor } information
U9 = 4558, dual op-amp
R1 = Coarse speed stickoff. Value depends on reference voltage level. R1 = 22 MΩ, 5% for 115V rms ref and R1 = 5.1 MΩ, 5% for 26V ref.
U4 – U8 = 4008, CMOS 4-bit adders.
U4, U5, U6 form 36X multiplier
U7, U8 form 1X angle offset
Coarse and fine speed loop gain
1% Resistors: R2 = 80.6 KΩ; R3 = 100 KΩ, R4 = 10 KΩ; R5 = 750 KΩ; R11 = 10 KΩ
C1 = 10μF, 6V DC
Crossover Detector
5% Resistors: R6 = 1 KΩ; R7, R8 = 1 MΩ, R9 = 200 KΩ, R10 = 30 KΩ
C2 = 0.1μF ceramic; CR1 - 1N4148
Crossover Switch
Q1 = 2N2946

SPECIFICATIONS

PARAMETER	VALUE
TEMPERATURE RANGES	
Operating	
–1 option	–55°C to +125°C
–3 option	0°C to +70°C
Storage	–55°C to +135°C
POWER SUPPLIES	
Nominal Voltage	+15 VDC / –15 VDC / Logic Supply
Voltage Range	+11 to +16.5V / 0 to –16.5V / +4.5V to +15 supply
Absolute Max Voltage	+18V / –18V / +18V
Current or Impedance	70 mA max* / 20 mA max* / Z_{IN} – 10 KΩ min

*Does not include current required by 60 Hz active transformers.

PARAMETER	VALUE
PHYSICAL CHARACTERISTICS	
Converter Module and Data Processor Module	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	1 oz max (28 g)
400 Hz Transformer Modules	
Type	Encapsulated module. Signal input uses 2 modules (T1A and T2B) Ref uses 1 module (T2)
Size	0.8 x 0.6 x 0.3 inch (2 x 1.5 x 0.8 cm)
Weight	0.4 oz max (11 g)
60 Hz Transformer Modules	
Type	Encapsulated module.Signal transformer and reference transformer each consist of one such module
Size	1.125 x 1.125 x 0.42 inch (2.86 x 2.86 x 1.07 cm)
Weight	0.7 oz max (20 g)

ORDERING INFORMATION

Order two hybrid control transformers and one hybrid data processor. DDC does not supply the discrete components for the angle multiplier, angle offset, and stickoff.

1. Order two control transformers as follows. These units operate over the full 47–1000 Hz frequency range. Transformers for HXCT-14 units must be ordered separately as described below.

HSCT–14–H–1–a–883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL- STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- Accuracy:
  - Blank = ±4 minutes
  - a = ±2 minutes
- Temperature Range (Operating):
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Voltage Levels:
  1. Synchro solid state input (HSCT):
     - H = 90V L-L
     - L = 11.8V L-L
  2. Resolver solid state input (HRCT):
     - H = 90V L-L
     - M = 26V L-L
     - L = 11.8V L-L
  3. Voltage follower input (HXCT): Omit voltage level specification. One HXCT model accepts all normal voltage levels.
- Resolution = 14 Bits
- Input Type
  - HSCT = Solid state synchro
  - HRCT = Solid state resolver
  - HXCT = Voltage follower buffer. Requires external signal conditioner such as an isolation transformer.

2. Order one data processor as follows:

HDP - 4 - 1 - 883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883
  - B = Screened to MIL-STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- Temperature Range:
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Carrier Frequency Range:
  - 4 = 360–1000 Hz
  - 6 = 47–1000 Hz

3. Isolation transformers for CT modules with voltage follower buffer inputs (HXCT-14) must be ordered separately by part number.

Type	Frequency	Ref. Voltage	L-L Voltage	Part Numbers: Ref. Xfmr.	Part Numbers: Signal Xfmr.
Synchro	400 Hz	115V	90V	21049	21045*
Synchro	400 Hz	26V	11.8V	21049	21044*
Resolver	400 Hz	115V	90V	21049	21048*
Resolver	400 Hz	26V	26V	21049	21047*
Resolver	400 Hz	26V	11.8V	21049	21046*
Synchro	60 Hz	115V	90V	24133	24126*

*The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

MECHANICAL OUTLINES

Mechanical outlines, pin assignments, and schematic diagrams for the control transformer and error processor modules and for all transformers are available from the factory.

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