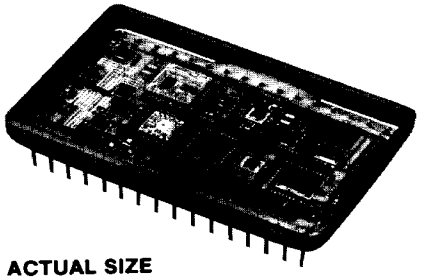
NATEL

HDR2106 = 996212

1.5 VA Output, 32-pin Hybrid. 16-bit Digital-to-Resolver Converter. Microprocessor Compatible.

Features

- **Fully protected 1.5 VA output**
  (current limiting)
  (short circuit proof)
  (thermal cutoff)
  (voltage feedback transients)
- **1 arc-minute accuracy**
- **0.03% max scale factor variation**
  (sin, cos conformance)
- **Microprocessor Compatible**
  (8 and 16-bit)
- **Double-buffered inputs**
- **Does not require +5 V power supply**
- **TTL and CMOS compatible**
- **Hi-rel MIL-STD-883B processing**
- **Priced at $495/USA price**
  (HDR2106-14S)



ACTUAL SIZE

Applications

Flight Simulation
Flight Instrumentation
Fire Control Systems
Position Control Systems
Driving CRT displays
Radar and Navigation Systems.

Description

Offering both 8- and 16-bit microprocessor compatibility, the HDR2106 is the only hybrid digital-to-resolver converter available that provides 1.5-VA output drive, 16-bit resolution and 1 arc-minute accuracy. The other outstanding features include double-buffered inputs, 0.03% vector accuracy and fully protected analog sine and cosine outputs.

Packaged in a 32-pin triple DIP, the converter does not require a +5-V logic supply. The digital inputs are TTL and CMOS compatible. Internally derived logic thresholds are 0.8 V-dc for a logic "low" and 2.4 V-dc for a logic "high." The digital input can accept a logic "high" of up to $+V_S$ (+15 V typical) without adversely affecting the performance of the converter.

All data bits (B1 through B16) are actively pulled down to ground. If the converter requires less than 16-bit resolution, the unused data bit pins may be left unconnected. Control Signals LBE, HBE and LDC are actively pulled-up to logic "high" so that the HDR2106 may be used in conventional applications without any external components or additional connections.

The output power stage can be driven by +15 V-dc power supply or pulsating supplies for higher efficiency. The output protection includes current limiting, thermal cutoff, short circuit and voltage feedback transients.

Model HDR2106 converters are available with angular accuracies of 1, 2 and 4 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring special compensation circuits. Matched thin-film resistors are used to scale the reference input as well as the sine and cosine outputs to assure excellent performance over the entire operating temperature range. All gain resistors are actively laser trimmed to achieve precise performance.

Theory of Operation

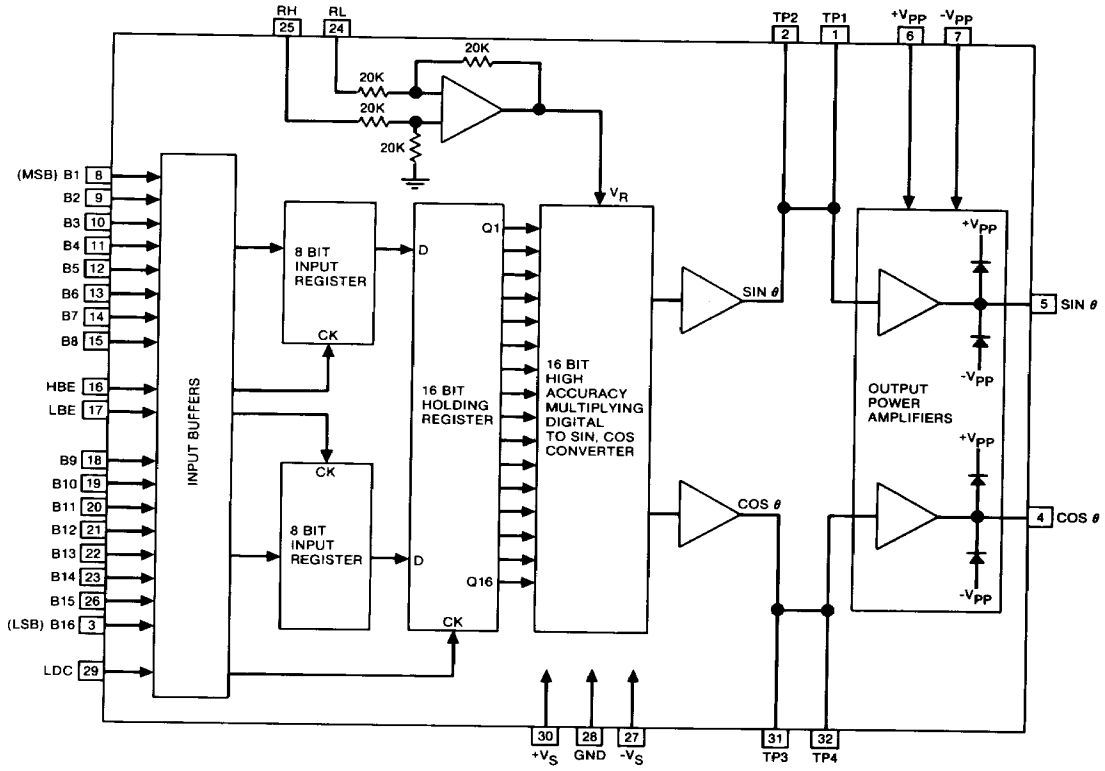


FIGURE 1 2106 Block Diagram

Operation of HDR2106 is illustrated in the functional block diagram of figure 1. The reference voltage is applied to a differential amplifier to obtain a buffered reference (V_R). The digital word representing the input angle is applied to input buffers. Two input registers accept 16-bits from the microprocessor. In conjunction with an 8-bit data bus, each input register can be separately enabled to accept the 16-bit word in two 8-bit bytes. This is accomplished by setting HBE to Logic "High" (High Byte enable), to load 8 MSBs (most significant bits). And . . . setting LBE (Low Byte enable) to Logic "High" to load 8 LSBs (least significant bits). The 16-bit data word is then parallel-loaded into a holding register and processed through a multiplying Digital-to-Sin/Cos converter.

Although not required for interfacing with a 16-bit data bus, the holding register is very important when interfacing with an 8-bit data bus. Without the 16-bit holding register, the output could hunt (go both clockwise and counterclockwise) while the digital input angle is changing in one direction only. For a continuous circular motion (most applications for digital-to-resolver converter) this hunt or jitter condition could occur 256 times in a circle i.e., every 1.4 degree.

The 16-bit holding register is enabled by setting the LDC (Load Converter) to Logic "High." When interfacing with a 16-bit data bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word.

The multiplying digital-to-sin/cos converter is made up of two function generators (sin θ and cos θ) and a quadrant-select network. The digital input code is natural binary angle. The two most significant bits (Bit 1 = 180°, Bit 2 = 90°) determine the quadrant information. Bits 3 through 16, containing angular information together with buffered reference voltage, are applied to two function generators. The operation of the function generators is very similar to a 4-quadrant multiplying DAC. Like a conventional DAC, the 2106 uses resistive ladder networks and solid-state switching to control the attenuation of the reference voltage. The ladder networks, however, are designed to attenuate the input reference proportional to the sine and cosine of the digital input angle. A unique approach is used in the design of ladder networks to obtain high accuracy in the sine and cosine generation so that they can be used as independently accurate functions. The outputs of function generators are then applied to a quadrant select network to obtain true sin θ and cos θ outputs. The sin θ and cos θ outputs are then applied to power amplifiers to obtain 1.5-VA drive capability at the analog outputs. The output amplifiers can be powered by either ±15 V-dc or a pulsating power supply for improved efficiency. The power amplifier design incorporates a safe operating area protection circuit similar to those used in voltage regulators.

Besides short-circuit protection and current limiting, the power amplifiers are designed to provide thermal shutdown, when the amplifier junction temperature reaches 165° C, thereby making them virtually indestructible. In addition both sin θ and cos θ outputs are protected against voltage feedback transients by the diode protection circuit shown in figure 1.

Specifications

PARAMETER	VALUE		REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)		MSB = 180° LSB = 0.0055°
Accuracy	±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minute (option V)		Accuracy applies over operating temp. range
Scale Factor Variation (Transformation ratio Error)	±0.03% maximum		Simultaneous amplitude variation in both outputs as a function of digital angle.
Reference Input (RH-RL)	3.4 V-rms		Differential solid state input
Frequency Range	dc to 1000 Hz dc to 5 kHz		Angular accuracy reduced
Input Impedance	Differential 40 kΩ Single Ended 20 kΩ		
Analog Outputs (Max SIN θ, COS θ)	6.8 V-rms ±0.2% Converter Gain = 2		Output voltage varies directly in proportion to reference voltage
Output Current Drive	250 mA-rms		short circuit protected
Output inpedance	<1 ohm		Operational amplifier output
Zero offset (dc)	±10 mV typical, ±25 mV maximum		
Offset drift	25μV/° C		
Output Settling Time	20 μsec maximum to accuracy of the converter		For any analog or digital step change
Digital Inputs **Logic Voltage Levels**			CMOS transient protected
Logic "0" Logic "1"	-0.3 V-dc to 0.8 V-dc +2.4 V-dc to +V_S		Does not need external logic voltage 0.1 TTL load
Input Currents			
Data Bits (B1-B16)	15 μA typical, "active" pull down to Ground (GND)		For less than 16-bits input, unused pins can be left unconnected
HBE, LBE, LDC	-15 μA typical, "active" pull up to Internal Logic Supply		When not used pins can be left unconnected
Register Controls			
HBE	Logic "1" Logic "0"		8 MSBs enter high byte input register High byte register remains unaffected
LBE	Logic "1" Logic "0"		8 LSBs enter low byte input register Low byte register remains unaffected
LDC	Logic "1" Logic "0"		Data from input registers transferred to holding register Data in holding register remains unaffected
Pulse Width	600 nsec minimum		For guaranteed data transfer
Data Set-up time	200 nsec minimum		Before data transfer
Data Hold time	200 nsec minimum		Before input data changes
Thermal Characteristics			
Junction to case thermal resistance (θ_{JC})	5° C/w typical, 7° C/w max.		without any additional Heat Sinking.
Case to ambient thermal resistance (θ_{CA})	15° C/w typical, 20° C/w max.		
Power Dissipation No Load 1.5 VA Resistive Load 1.5 VA Inductive Load 1.5 VA Typical CT Load	 2.25 watts maximum 3.6 watts maximum 5.1 watts maximum 4.6 watts maximum		
Power Supplies			
Supply Voltages	±15 V-dc	±V_{PP} (15 V peak)	±5% without output clipping.
Supply Currents No Load Currents 1.5 VA Load Currents Mean 1.5 VA Load Currents Peak Short circuits currents	 ±30 mA maximum ±30 mA maximum ±30 mA maximum ±30 mA maximum	 ±75 mA maximum ±170 mA maximum ±310 mA maximum ±500 mA maximum	
Physical Characteristics			
Type	32 PIN Triple DIP		
Size	1.14 x 1.74 x 0.18 inch (29 x 44 x 4.6mm)		
Weight	0.8 oz (23 g) max.		

The Model 2106 converter uses discrete thin-film resistors (as compared to screened thick-film resistors), thereby allowing flexibility for different gain, reference and output voltages. In addition improved dc offset, if desired, can be achieved by internal offset trims. Contact a Natel Applications Engineer or our sales department for assistance.

Pin Designations

B1 - B16 — Parallel Data Input Bits
B1 is MSB = 180 degrees
B16 is LSB = 0.0055 degree

HBE — High Byte Enable -
Data inputs B1 through B8 enter the input buffer register when HBE is set to a Logic "High." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B1-B8 pins.

LBE — Low Byte Enable -
Data inputs B9 through B16 enter the input buffer register when LBE is set to Logic "High." When LBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9-B16 pins.

LDC — Load Converter -
When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the 16-bit holding register. When LDC is set to Logic "Low," the converter is in the hold mode and is not affected by digital activity in the input registers.

Note: For continuous updating HBE, LBE and LDC may be left open. Internal active pull-up will force these functions to a Logic "High"

RH, RL — Reference Voltage Input

GND — Power Supply Ground
Digital Ground
Analog Signal Ground

$+V_S$, $-V_S$ — Supply Voltages -
Typically ±15 V-dc

TP1	1	32	TP4
TP2	2	31	TP3
B16	3	30	$+V_S$
COS θ	4	29	LDC
SIN θ	5	28	GND
$+V_{PP}$	6	27	$-V_S$
$-V_{PP}$	7	26	B15
B1	8	25	RH
B2	9	24	RL
B3	10	23	B14
B4	11	22	B13
B5	12	21	B12
B6	13	20	B11
B7	14	19	B10
B8	15	18	B9
HBE	16	17	LBE

FIGURE 2 HDR2106 Pin Assignments

+VPP, -VPP — Pulsating Power Supplies -
(For output power amplifiers)

SIN θ, COS θ — Output Analog Signals

TP1 - TP4 — Test points -
Do not connect
(Used for other applications)

Absolute Maximum Ratings

Reference Input	Twice specified Voltage
Power Supply Voltages (±VS)	±18 V-dc
Power Supply Voltages (±VPP)	±20 Vpeak
Digital Inputs	-0.3 V-dc to +VS
Storage Temperature	-65° C to +150° C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply be turned off. Decoupling capacitors are recommended on the +VS and -VS supplies. A 1μF tantalum capacitor in parallel with 0.01μF ceramic capacitor should be mounted as close to the supply pins as possible.

CAUTION:
Reversal of +VS and -VS or reversal of +VPP and -VPP power supply connections will result in permanent damage to the converter.

For applications requiring high output drive, an adequate heat sink must be provided to keep the case temperature below the maximum operating temperature. The HDR2106 converter has been designed with a flat metal base to allow the addition of heat sinking material.

Digital Interface

The double buffered input registers of the HDR2106 offer the user an easily implemented interface with 8 or 16-bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing his own interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Asynchronous data inputs up to 16-bits can be accommodated. Memory mapped I/O with an 8080 microprocessor is described in our data sheet HDSC2016.

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 3. Inputs LBE; HBE and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs B1-B16 is continuously converted to $\sin\theta$ and $\cos\theta$ at the analog outputs. For applications requiring less than 16-bit resolution, unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B1-B16.

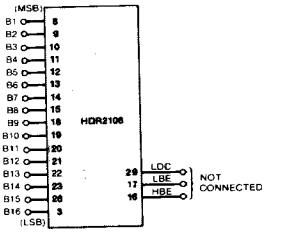


FIGURE 3 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 4. As shown in figure 5 timing diagram, the 8 LSBs (B9-B16) are transferred to the low-byte input register when LBE is a logic "1." LBE can be "High" when data bits are changing, but must remain "High" for a minimum of 800 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE goes "Low." Bits B1-B8 are transferred to the high-byte input register when HBE is a logic "1." The timing requirements are the same as those for LBE. Data are transferred from the two input registers to the holding register when LDC (load converter) is at logic "1." If LDC is at logic "0," the contents of the holding register are latched and remain at their previous values unaffected by changes at the data inputs or input registers.

Note that LBE, HBE and LDC are level-actuated functions.

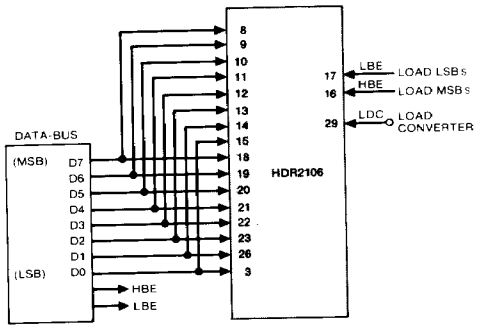


FIGURE 4 Digital Connections for Two-Byte Loading

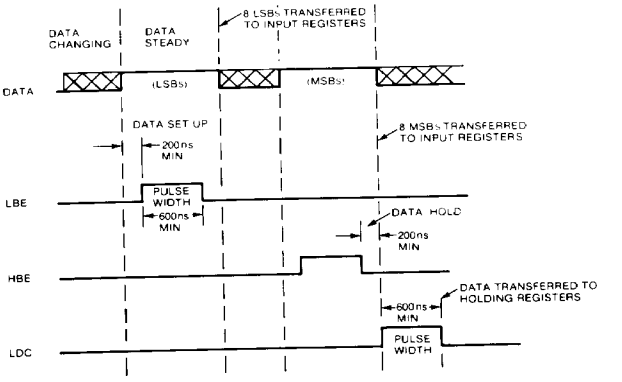


FIGURE 5 Two-Byte Loading

Single Byte Loading

Single 16-bit byte loading is illustrated in figure 6. As shown in the timing diagram (figure 7), 200 nsec after the data is stable, the input angular information is transferred to the holding register when LDC is at a logic "1." LDC is a level-actuated function and must remain high for the times specified in the timing diagram.

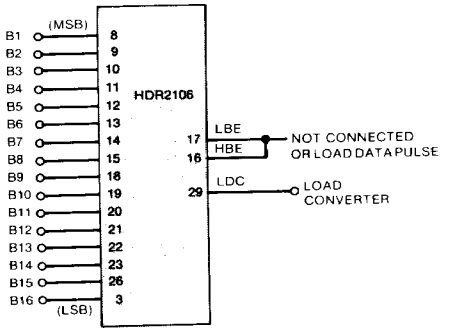


FIGURE 6 Digital Connections for One Byte (16 bits) Loading

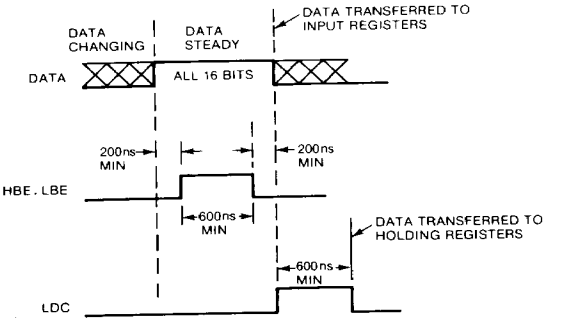


FIGURE 7 Single-Byte Loading

Power Supply for Output Amplifiers

Although a ±15 V-dc supply can be used for ±VPP, for high efficiency and low heat dissipation, a pulsating power supply is highly recommended. As shown in figure 8, the ac reference voltage is used to produce two unfiltered full wave rectified positive and negative voltages. These voltages, being in phase with the reference, are always in phase with sin θ and cos θ outputs. Therefore, the amplitude of the pulsating supply voltage need only be a few volts (4 volts) greater than the maximum output voltage. Small filter capacitors are used to provide enough dc voltage for biasing the power amplifiers. Since heat dissipation in a power amplifier is proportional to the difference between power supply voltage and output voltage, the pulsating power supply (due to its waveform tracking the output waveform) offers almost 2 to 1 improvement (for typical CT load) over the dc supply. In addition, as the output varies with the reference, the pulsating power supply varies proportionally, thereby providing further improvement in power and thermal efficiency.

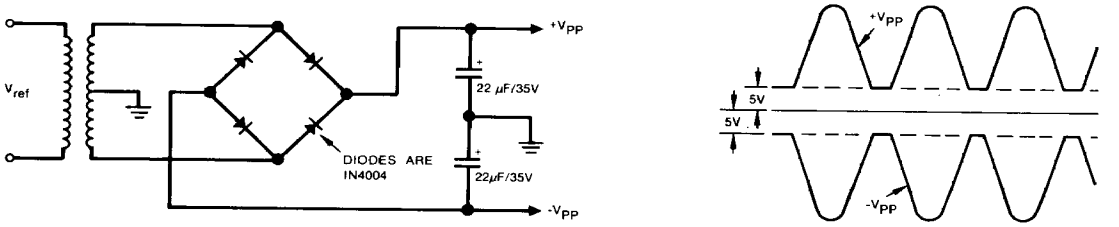


FIGURE 8 Pulsating Power Supply

Analog Output Adjustment and Phasing

Operation of the HDR2106 is very similar to that of a multiplying digital-to-analog converter. The sin and cosine ouputs are directly proportional to and have the same waveform as the reference voltage. Any distortion or harmonics present at the reference will appear at the output lines. Higher or lower output voltages can be obtained by varying the reference voltage. But, with ±15-V supply voltages, clipping of the output waveform will occur if the reference amplitude exceeds the specified valve by more than 10%.

The input circuit for a differential reference amplifier is shown in figure 9. To obtain lower output voltages or to operate the HDR2106 with a higher reference voltage, two external resistors would be required. Figure 10 shows the output phasing and mathematical relationship between the reference voltage and the output analog signals as functions of the digital angle θ and converter gain K (nominally 2). Discrete thin film resistors are used in the reference amplifier circuit. If non-standard reference voltage or different output voltage is required in your application, it can easily be accomplished at no additional cost. Contact the Natel sales department.

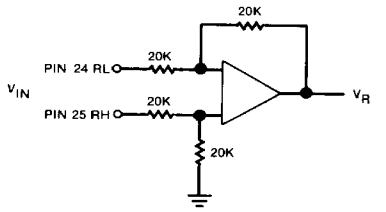


FIGURE 9 Reference Input Circuit

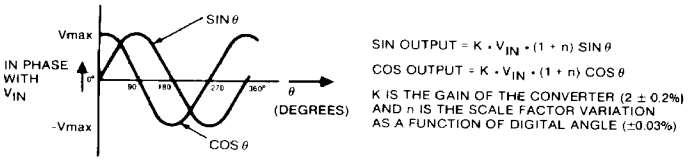


FIGURE 10 Output Phasing

Applications using HDR2106:

Figures 11 and 12 show simple schematics for transformer-isolated digital-to-resolver and digital-to-synchro converters. The Model HDR2106 with its output drive of 1.5 VA can drive control transformers (CT) directly, by the addition of output transformers only. This allows the user flexibility and ease of interfacing with different voltages and frequencies by changing only the transformers.

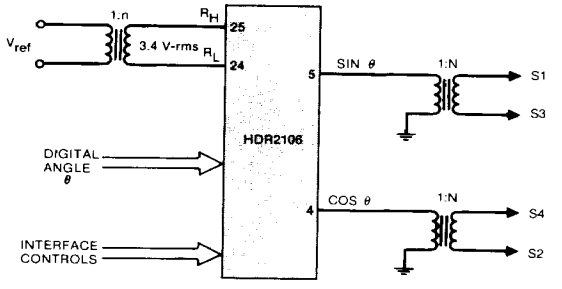


FIGURE 11 Digital-to-Resolver Converter

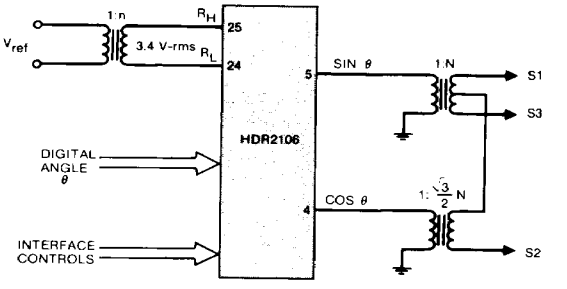


FIGURE 12 Digital-to-Synchro Converter

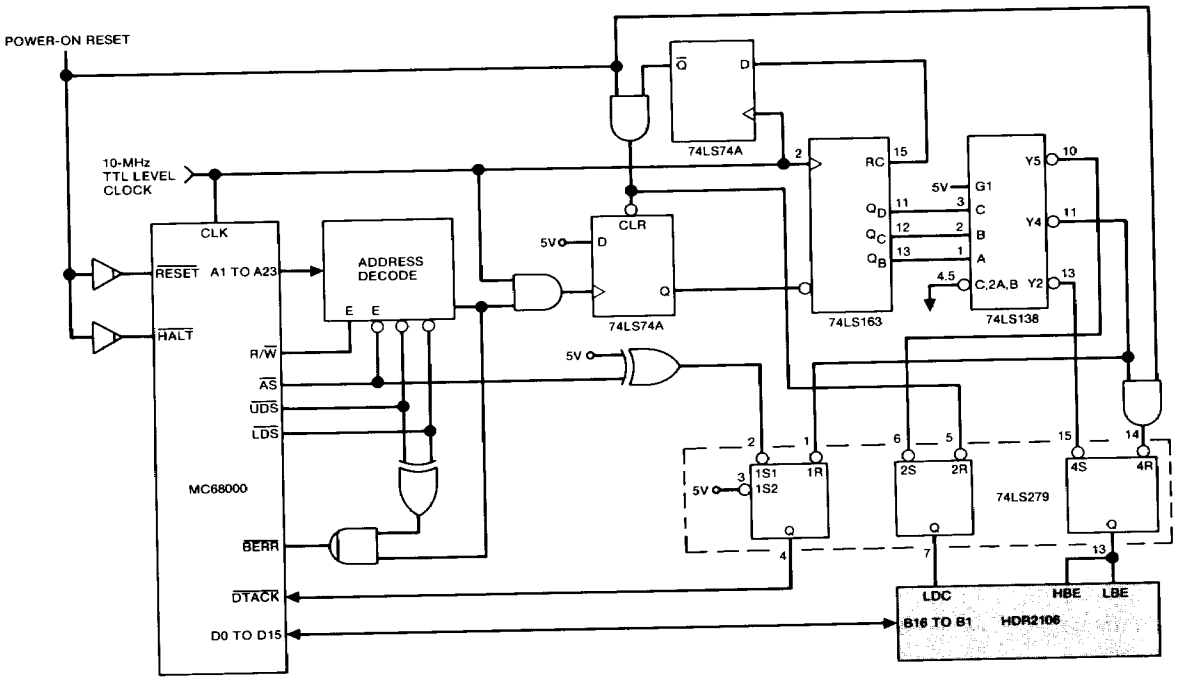
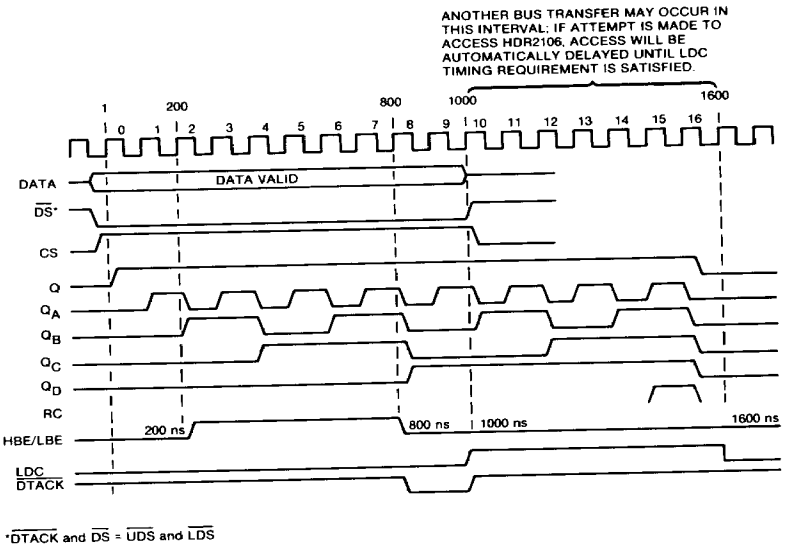


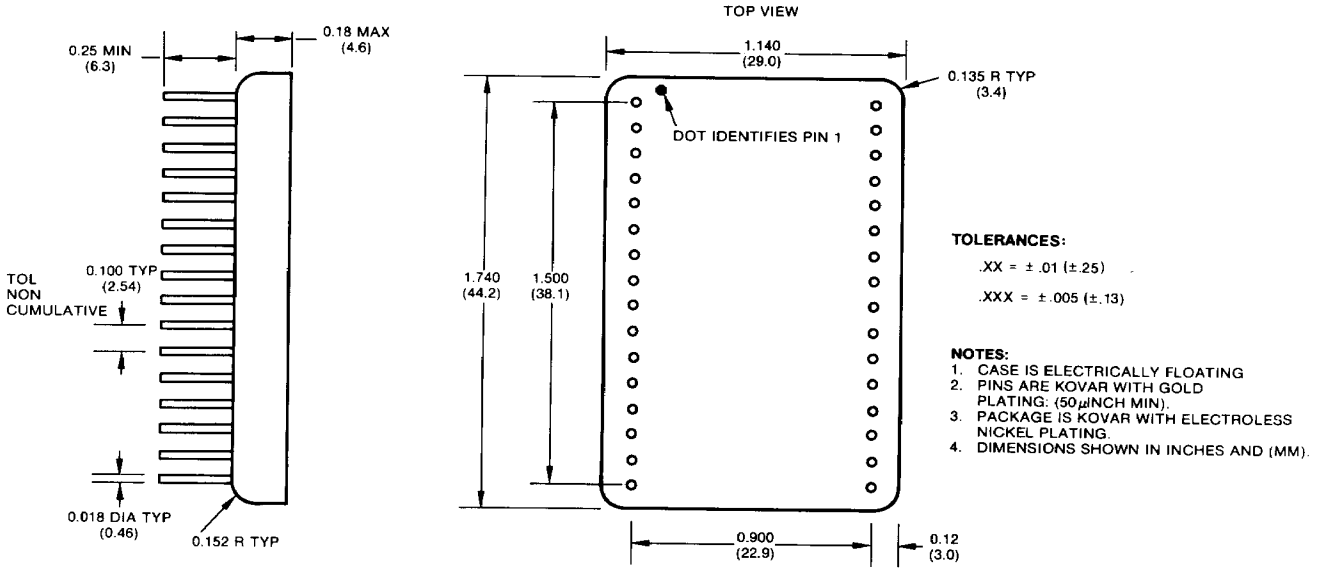
FIGURE 13 Interfacing Digital To Resolver Converter With 16-Bit Microprocessor.

The interface between a digital-to-resolver converter and an 8-bit microprocessor is described in the Natel data sheet for HDSC2016. Figure 13 shows the interface for a digital-to-resolver converter with a 16-bit microprocessor. Interface timing is shown in figure 14. To simplify the interface, a counter-driven controller sequences the converter's control lines. Whenever the microprocessor performs a 16-bit word write, the 74LS163 counter is enabled. Outputs of the counter drive a 74LS138, which generates the strobes to sequence HBE/LBE, $\overline{\text{DTACK}}$, and LDC. If the microprocessor attempts to do a byte write (only one data strobe active), then a bus error ($\overline{\text{BERR}}$) is generated. $\overline{\text{BERR}}$ terminates the bus cycle and automatically generates an exception call to the operating system. To move a 16-bit word from a memory location or microprocessor register, the instruction MOVE. W EA, HDR2106 could be used.



*$\overline{\text{DTACK}}$ and $\overline{\text{DS}}$ = $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$

FIGURE 14 16-Bit Microprocessor Interface Timing



MECHANICAL OUTLINE (32 PIN TRIPLE DIP)

Ordering Information

HDR 2106 - T F A

Temperature Range
1 = 0° C to +70° C
2 = -25° C to +85° C
3 = -55° C to +125° C

Frequency Range
4 = dc to 1000 Hz
5 = dc to 5 kHz

Accuracy
S = ±4 arc-minutes
H = ±2 arc-minutes
V = ±1 arc-minute

As a standard practice, all converters are built in accordance with the requirements of MIL-STD-883B, including 168 hours of active burn-in.

Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10 to 16-bit resolutions (1000 series)
- Hybrid (36-pin DDIP size) Digital-to-Synchro (Resolver) converters with 14 and 16-bit resolutions (2000 series)
- Two-speed Synchro (Resolver)-to-Digital converters with 16 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412).
- Multiplexed Synchro (Resolver)-to-Digital converters.
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.
- High Power synchro/resolver drivers
- Code-converters.

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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