NATEL
HDR2406 996215

One-Inch Square Package. 16-bit Digital-to-Resolver Converter. Microprocessor Compatible.

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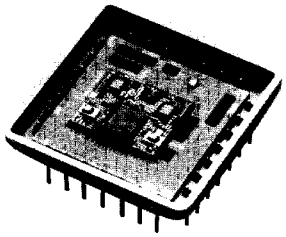
006389
6389 NTL

Features

- **28-pin Square package**
- **1 arc-minute accuracy**
- **0.03% radius accuracy**
- **Microprocessor compatible** (8 and 16-bit)
- **Double buffered inputs**
- **Pin-programmable reference input** (for 26 and 115 V-rms)
- **dc-coupled reference and outputs**
- **Requires only ±15-V power supplies**
- **TTL and CMOS compatible**
- **Hi rel MIL-STD-883B processing**
- **Priced at $230/USA single unit price** (HDR2406-14L)



ACTUAL SIZE

Applications

Digital Remote positioner
Axis rotation
Vector resolution
Resolver computing circuits
Digital-to-resolver (synchro) converter
Low frequency oscillator
Radar and navigational systems
Flight instrumentation

HDR2406

Description

Designed primarily for use within a resolver of size 15 or larger, the Model HDR2406 is contained in a 1-inch square hermetically-sealed package. Offering both 8- and 16-bit microprocessor compatibility the converter accepts a digital input of 16-bits (CMOS/TTL) as angle θ and a reference voltage of either 115 V-rms or 26 V-rms to generate the resolver outputs of 6.8 Sin θ and 6.8 Cos θ.

Model 2406 does not require a +5-V logic supply. The digital inputs are TTL and 5-V CMOS compatible. Internally derived logic thresholds are 0.8 V-dc for a logic "low" and 2.4 V-dc for a logic "high."

All data bits (B1 through B16) are actively pulled down to ground. If the converter requires less than 16-bit resolution, the unused data bit pins may be left unconnected. Control Signals LBE, HBE, and LDC are actively pulled-up to logic "high." When not required by your application, these pins may also be left open.

Although designed to interface with most microprocessors, the HDR2406 may be used in conventional appications without any external components or additional connections.

Model HDR2406 converters are available with angular accuracies of 1, 2, 4 and 8 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring special compensation circuits.

Matched thin film resistors are used to generate the sine and cosine outputs to assure excellent angular accuracy over the entire operating temperature range. All gain resistors are actively laser trimmed to achieve precise performance.

Theory of Operation

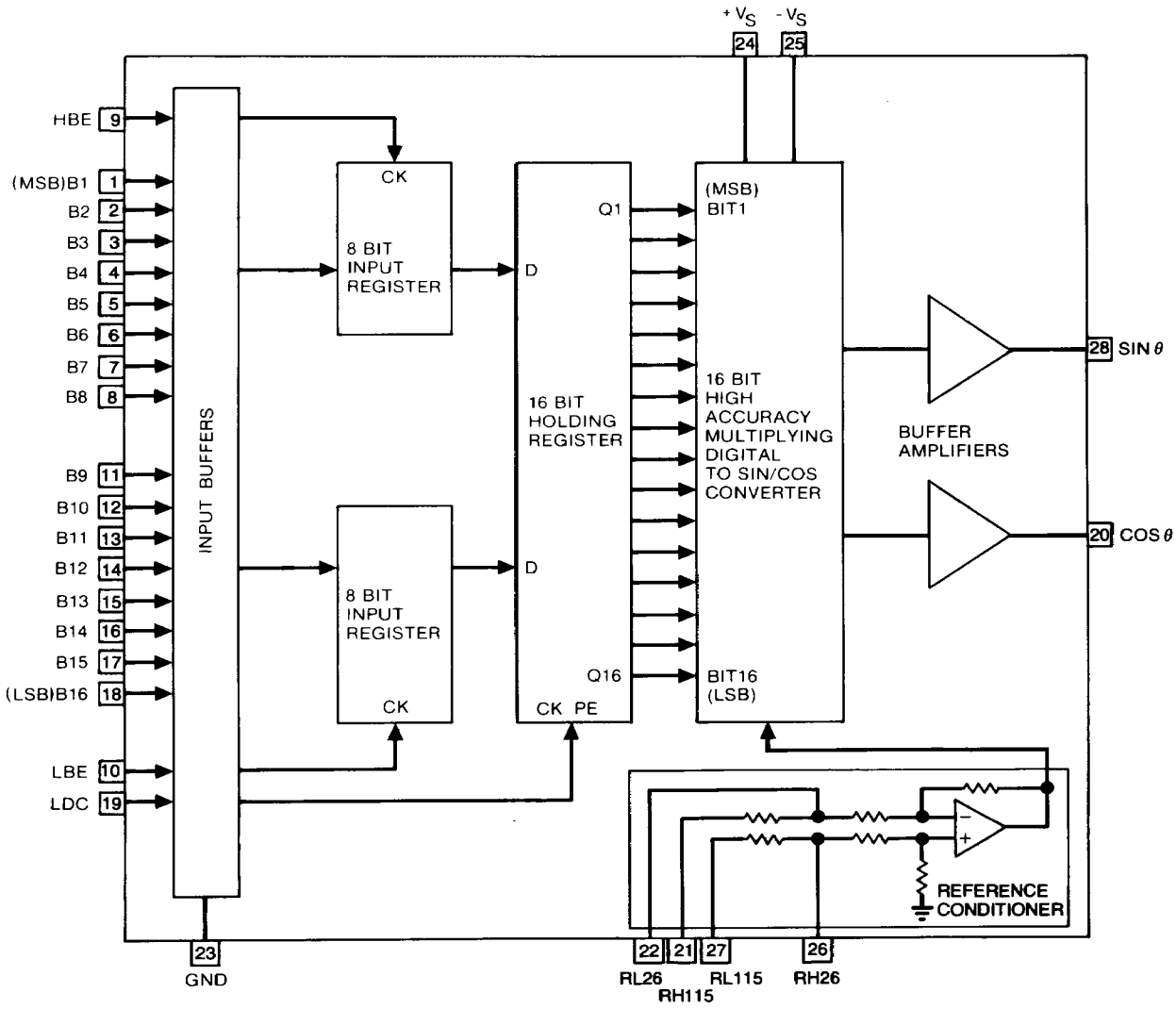


FIGURE 1 2406 Block Diagram

The operation of the Model 2406 is illustrated in the functional block diagram of figure 1. The reference voltage is applied to a differential operational ampliier in the reference conditioner. The digital word representing the input angle is applied to input buffers . Two input registers accept 16-bits from the microprocessor. In conjunction with an 8-bit data bus, each input register can be independently enabled to accept the 16-bit word in two 8-bit bytes. When interfacing with 16-bit data bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word. The 16-bit data word is then parallel-loaded into holding register and processed through a Multiplying Digital-to-Sin/Cos converter.

The multiplying digital-to-sin/cos converter is made up of two function generators (sin θ and cos θ) and quadrant select network. The digital input code is natural binary angle. The two most significant bits (Bit 1 = 180°, Bit 2 = 90°) determine the quadrant information. Bits 3 through 16, containing angular information together with buffered reference voltage, are applied to two function generators. The operation of the function generators is very similar to a 4-quadrant multiplying DAC. Like a conventional DAC, the 2406 uses resistive ladder networks and solid state switching to control the attenuation of the reference voltage. The ladder networks, however, are designed to attenuate the input reference proportional to the sine and cosine of the digital input angle. A unique approach is used in the design of ladder networks to obtain high accuracy in the sine and cosine generation so that they can be used as independently accurate functions. The outputs of function generators are then applied to a quadrant select network to obtain true sin θ and cos θ outputs.

Specifications

PARAMETER	VALUE	REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)	MSB = 180° LSB = 0.0055°
Accuracy	±8 arc-minutes (option L) ±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minute (option V)	Accuracy applies over operating temp. range
Scale Factor Variation (Transformation ratio Error)	±0.03% maximum	Simultaneous amplitude variation in both outputs as a function of digital angle.
Reference Input (RH-RL)	115 V-rms or 26 V-rms	Differential solid state input
Frequency Range	dc to 1000 Hz (option 4) dc to 5 kHz (option 5)	
Input Impedance	Differential 230kΩ Differential 52kΩ	For 115 V-rms reference For 26 V-rms reference
Analog Outputs (Max SIN θ, COS θ)	6.8 V-rms ±1%	Output voltage varies directly in proportion to reference voltage
Output Current	2mA-rms	short circuit protected
Output inpedance	<1 ohm	Operational amplifier output
Zero offset (dc)	±10 mV typical, ±25 mV maximum	Improved offset available by internal offset trimming
Offset drift	25μV/°C typical, 50μV/ °C maximum	
Output Settling Time	50 μsec maximum to accuracy of the converter	For any analog or digital step change
Digital Inputs Logic Voltage Levels		CMOS transient protected
Logic "0" Logic "1"	-0.3 V-dc to 0.8 V-dc +2.4 V-dc to 5.5 V-dc	Does not need external logic voltage 0.1 TTL load
Input Currents		
Data Bits (B1-B16)	15 μA typical, "active" pull down to Ground (GND)	For less than 16-bits input, unused pins can be left unconnected
HBE, LBE, LDC	-15 μA typical, "active" pull up to Internal Logic Supply	When not used pins can be left unconnected
Register Controls		
HBE	Logic "1" Logic "0"	8 MSBs enter high byte input register High byte register remains unaffected
LBE	Logic "1" Logic "0"	8 LSBs enter low byte input register Low byte register remains unaffected
LDC	Logic "1" Logic "0"	Data from input registers transferred to holding register Data in holding register remains unaffected
Pulse Width	600 nsec minimum	For guaranteed data transfer
Data Set-up time	200 nsec minimum	Before data transfer
Data Hold time	200 nsec minimum	Before input data changes
Power Supplies		
Supply voltages (±V_S) Supply Currents Supply Rejection	±15 V-dc ± 10% ±20 mA maximum 80 dB typical	Without output clipping
Physical Characteristics		
Type	28 Pin Square	
Size	1.0×1.0×0.21 inch (25×25×5.3mm)	
Weight	0.6 oz (17 g) max	

Absolute Maximum Ratings

Reference Input ..... Twice Normal Voltage
Power Supply Voltages (±Vs) ..... ±18 V-dc
Digital Inputs ..... −0.3 V-dc to 6.5 V-dc
Storage Temperature ..... −65°C to +135°C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply be turned off. Decoupling capacitors are recommended on the $+V_S$ and $-V_S$ supplies. A 1μF tantalum capacitor in parallel with 0.01 μF ceramic capacitor should be mounted as close to the supply pins as possible.

Pin Designations

GND — Power Supply Ground
Digital Ground
Analog Signal Ground

B1-B16 — Parallel Data Input Bits
B1 is MSB = 180 degrees
B16 is LSB = 0.0055 degree

HBE — High Byte Enable —
Data inputs B1 through B8 enter the input buffer register when HBE is set to a Logic "high." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B1-B8 pins.

LBE — Low Byte Enable —
Data inputs B9 through B16 enter the input buffer register when LBE is set to Logic "High." When LBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9-B16 pins.

LDC — Load Converter —
When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the 16-bit holding register. When LDC is set to Logic "Low," the converter is in the hold mode and is not affected by digital activity in the input registers.

Note: For continuous updating HBE, LBE and LDC may be left open. Internal active pull-up will force these functions to a Logic "High"

+Vs, −Vs — Supply Voltage —
Typically ±15 V-dc

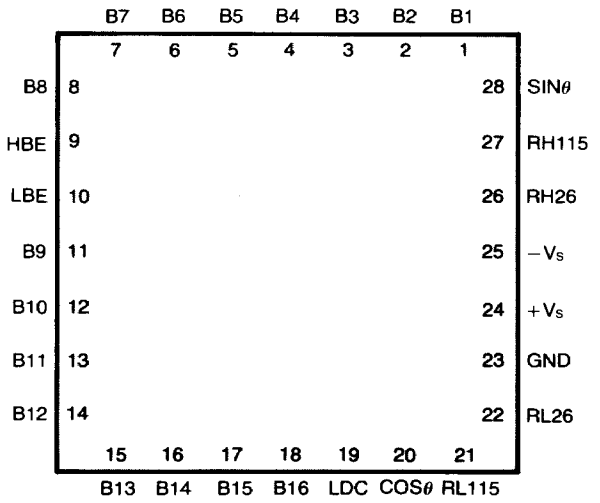


FIGURE 2 HDR2406 Pin Assignments

SIN θ, COS θ — Output Analog Signals

RH115, RL115 — Reference Voltage Input for 115 V-rms reference

RH26, RL26 — Reference Voltage Input for 26 V-rms reference

Caution: Reversal of +Vs and −Vs power supply connections will result in permanent damage to the converter.

Digital Remote Positioner Using HDR2406

Using the HDR2406, a self-contained digital remote positioner can be constructed as shown in figure 3. The remote digital angular input θ, together with an ac reference is applied to HDR2406. The output of the HDR2406 is connected to a resolver that produces an analog error signal which is then demodulated and amplified and applied to a dc torque motor. With the direct drive construction (motor armature and resolver rotor on the same shaft), they will turn together without any additional error or change in position normally caused by gearing. If the digital input is continuously up-dated, the digital remote positioner shaft will rotate continuously.

Although model HDR2406 is specified for reference voltages of 115 and 26 V-rms, other reference voltages can be accommodated. Contact the Natel Application or Sales Department for your specific requirements.

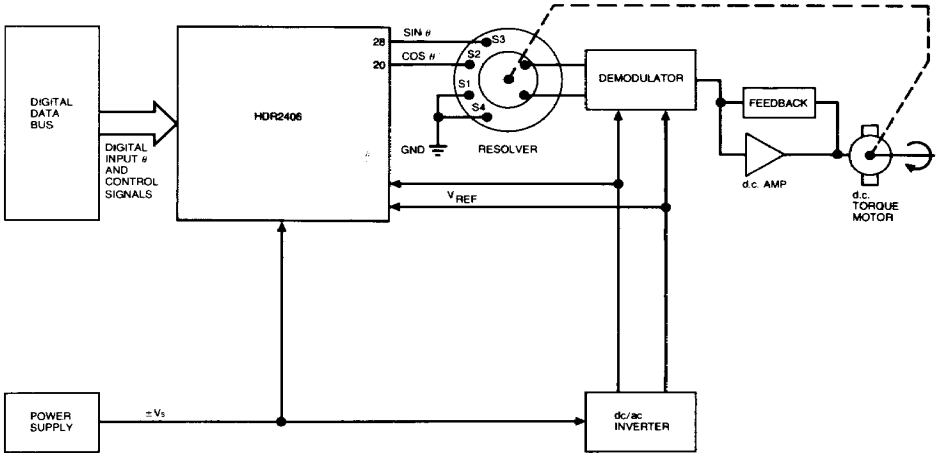


FIGURE 3 Digital Remote Positioner

Digital Interface

The double buffered input registers of the HDR2406 offer the user an easily implemented interface with 8-or 16-bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing his own interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Asynchronous data inputs up to 16 bits can be accommodated.

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 5. Inputs LBE; HBE and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs B1-B16 is continuously converted to $\sin\theta$ and $\cos\theta$ at the analog outputs. For applications requiring less than 16-bit resolution, unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B1-B16.

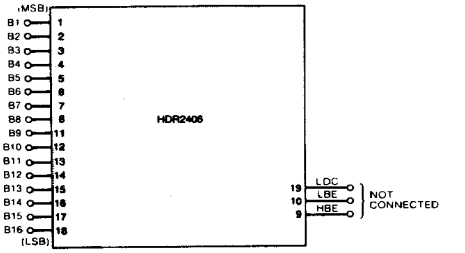


FIGURE 5 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 6. As shown in figure 7 timing diagram, the 8 LSBs (B9-B16) are transferred to the low-byte input register when LBE is a logic "1". LBE can be "High" when data bits are changing, but must remain "High" for a minimum of 800 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE goes "Low." Bits B1-B8 are transferred to the high-byte input register when HBE is a logic "1." The timing requirements are the same as those for LBE. Data are transferred from the two input registers to the holding register when LDC (load converter) is at logic "1." If LDC is at logic "0," the contents of the holding register are latched and remain at their previous values unaffected by changes at the data inputs or input registers.

Note that LBE,HBE and LDC are level-actuated functions.

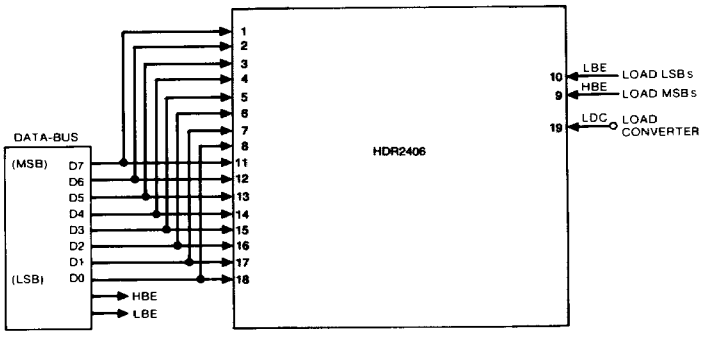


FIGURE 6 Digital Connections for Two-Byte Loading

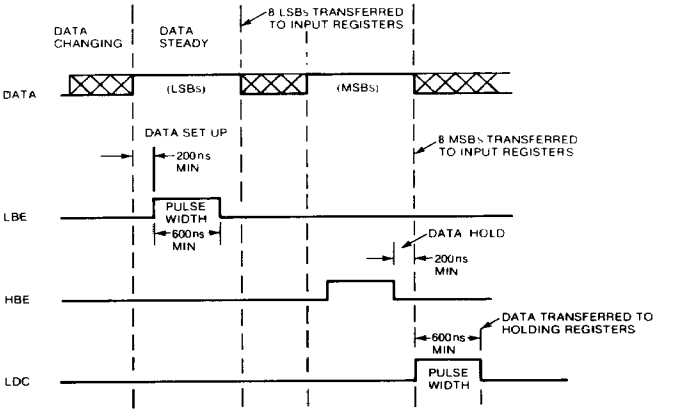


FIGURE 7 Two-Byte Loading

Single Byte Loading

Single 16-bit byte loading is illustrated in figure 8. As shown in the timing diagram (figure 9), 200 nsec after the data is stable, the input angular information is transferred to the holding register when LDC is at a logic "1". LDC is a level-actuated function and must remain high for the times specified in the timing diagram.

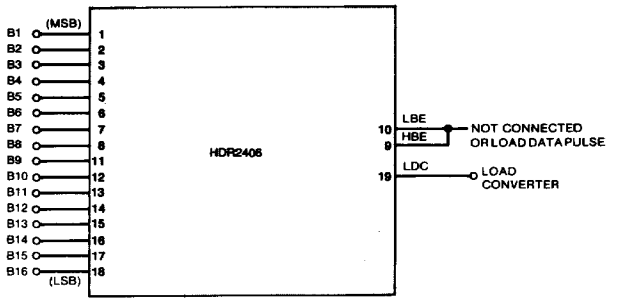


FIGURE 8 Digital Connections for One Byte (16 bits) Loading

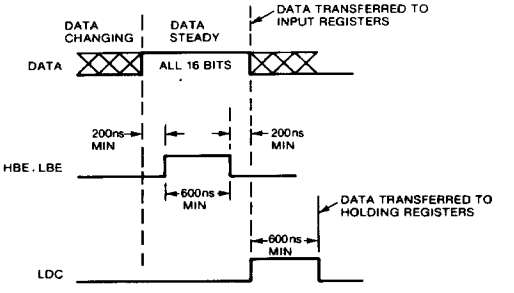


FIGURE 9 Single-Byte Loading

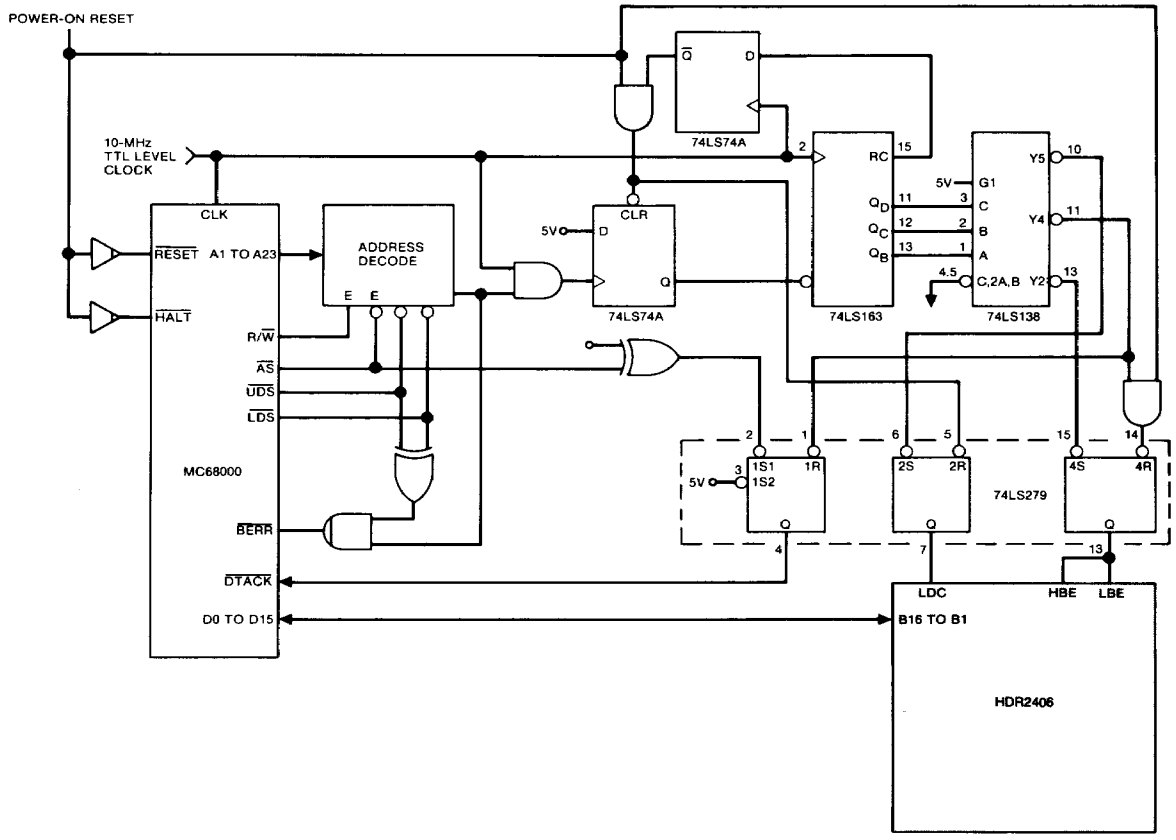
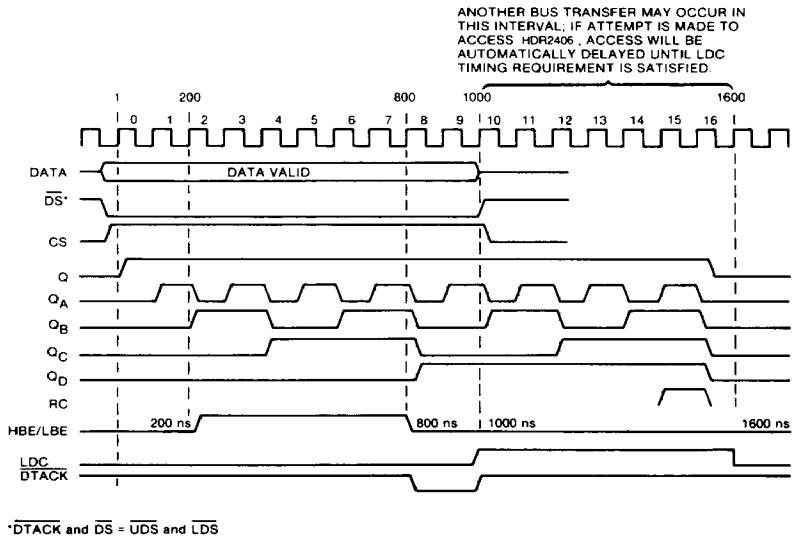


FIGURE 10 Interfacing Digital To Resolver Converter With 16-Bit Microprocessor.

Figure 10 shows the interface for a digital-to-resolver converter with a 16-bit microprocessor. Interface timing is shown in figure 11. To simplify the interface, a counter-driven controller sequences the converter's control lines. Whenever the microprocessor performs a 16-bit word write, the 74LS163 counter is enabled. Outputs of the counter drive a 74LS138, which generates the strobes to sequence HBE/LBE, $\overline{\text{DTACK}}$, and LDC. If the microprocessor attempts to do a byte write (only one data strobe active), then a bus error ($\overline{\text{BERR}}$) is generated. $\overline{\text{BERR}}$ terminates the bus cycle and automatically generates an exception call to the operating system. To move a 16-bit word from a memory location or microprocessor register, the instruction MOVE. W EA, HDR2406 could be used.



*$\overline{\text{DTACK}}$ and $\overline{\text{DS}}$ = $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$

FIGURE 11 16-Bit Microprocessor Interface Timing

Memory-Mapped I/O With 8080 Microprocessor

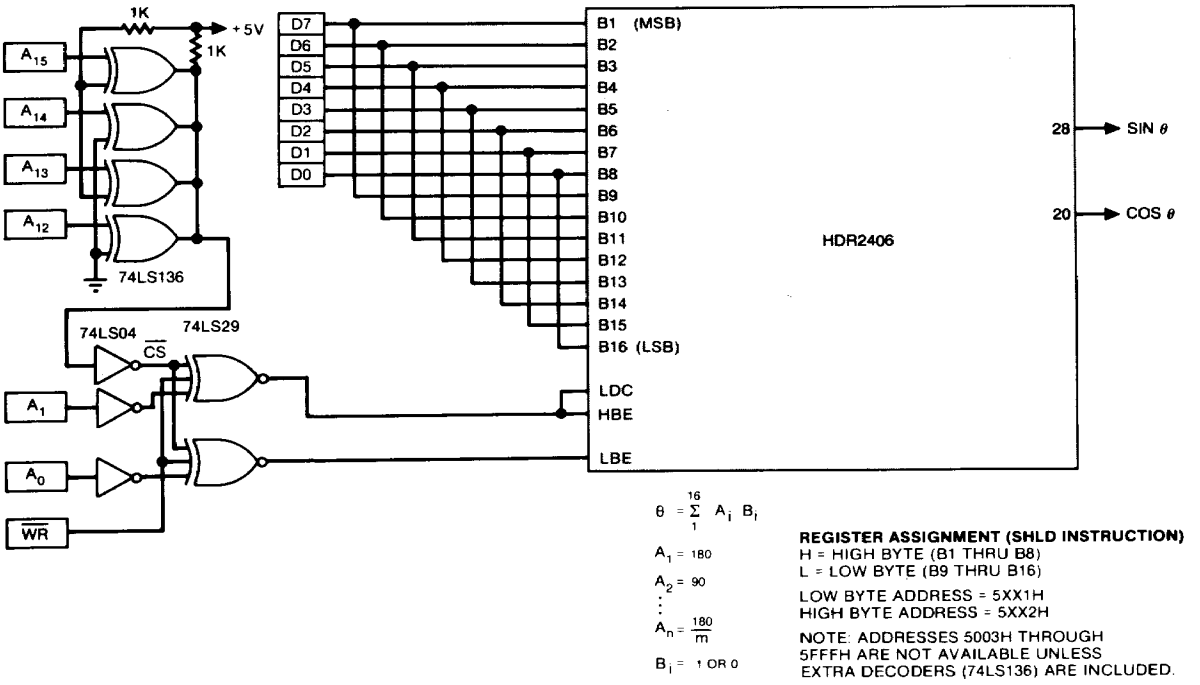


FIGURE 12 8080μP-HDR2406 Memory– Mapped Interface Connection Diagram

A typical example of a microprocessor interface using memory mapping and an 8080-type 8-bit μP is shown in figure 12. Memory-mapped I/O enables the HDR2406 to receive data from the μP using the same instructions that are required to transfer data to and from memory locations. This means that, in addition to the accumulator, any of the internal registers can be used to transfer data to the converter. This is a particularly attractive feature, since the use of the SHLD instruction permits transfer of a 16-bit output to the HDR2406 with a single instruction.

As is shown in figure 12, the control signals necessary to operate the converter are provided by the external gating structure. The CS signal (Chip Select) is generated by decoding the address bus with the 74LS136 exclusive-or gates, hard-wired to the selected address. In the example, only the upper 4 address lines are decoded. When the address 5XXXH is decoded, CS goes low enabling the 74LS29 control gates. When the selected address is 5XX1H and the $\overline{WR}$ line goes low, D0-D7 are transferred to the low-byte input register. When $\overline{WR}$ returns to high, LBE goes low, latching the data. Using the SHLD instruction, the next processor cycle will increment the address to 5XX2H and output the next byte of data. When $\overline{WR}$ again goes low, HBE and LDC go high, transferring both data bytes to the converter's 16-bit holding register, at which time the conversion takes place. The data format for loading the H and L registers is shown below:

H Registers -- High Byte

B1	B2	B3	B4	B5	B6	B7	B8
D7	D6	D5	D4	D3	D2	D1	D0

(MSB)

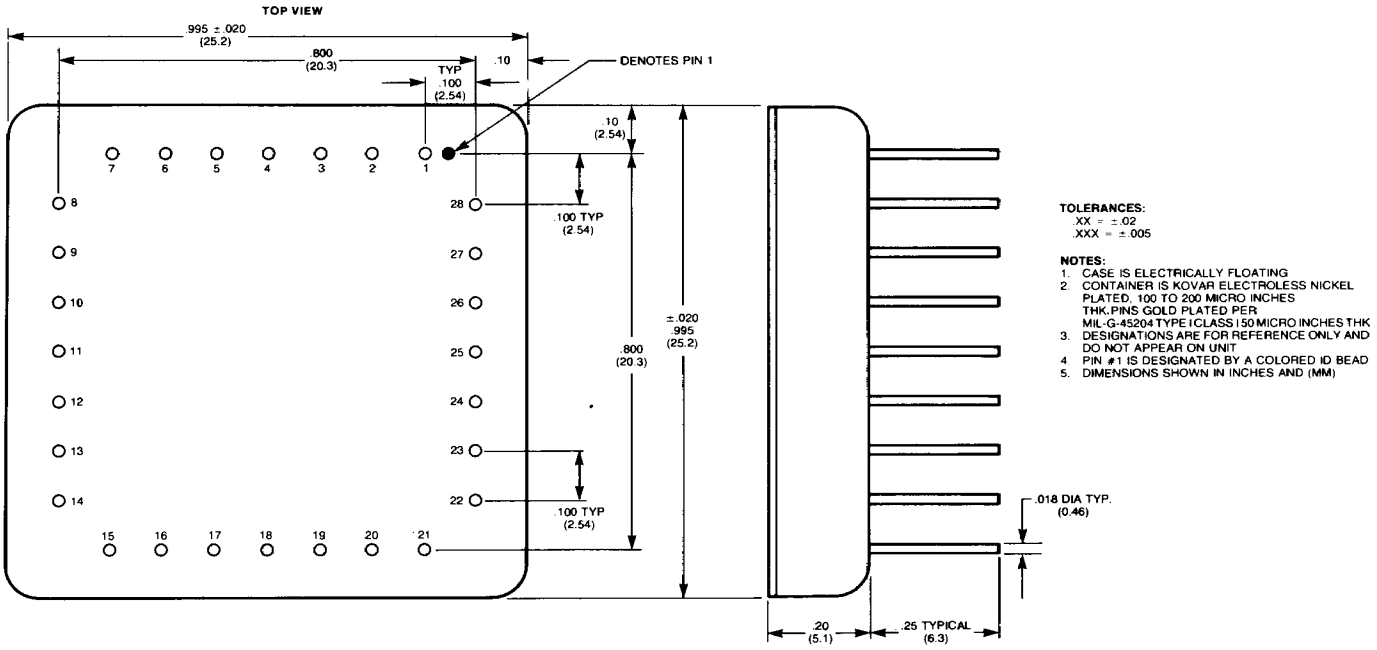
L Registers -- Low Byte

B9	B10	B11	B12	B13	B14	B15	B16
D7	D6	D5	D4	D3	D2	D1	D0

(LSB)

Other Synchro Conversion products available from NATEL

- Two-speed logic combiner with 20-bit, 3-state output, in a 1.3 x 2.6 x .35 inch size (TSL1x36)
- 14 and 16-bit Digital to Synchro/Resolver converters, with internal power amplifiers (5012, 5112, 5116)
- High power Synchro/Resolver Drivers
- 10 to 20-bit single-speed Synchro-to-Digital converters
- Hybrid synchro converters - see page 8
- Low profile Digital-to-Synchro/Resolver converters
- Two-speed Synchro (Resolver)-to-Digital converters with 16 and 20-bit resolutions in a single package. (Models 2SD402 and 2SD412).
- Solid State control transformers (SSCT) and differential transmitters (SCDX).
- Angle position indicators and synchro instrumentation for one-speed and multi-speed applications.



MECHANICAL OUTLINE

Ordering Information

HDR 2406 - T F A

Temperature Range
1 = 0°C to +70°C
2 = -25°C to +85°C
3 = -55°C to +125°C

Accuracy
L = ±8 arc-minutes
S = ±4 arc-minutes
H = ±2 arc-minutes
V = ±1 arc-minute

Frequency Range
4 = dc to 1000 Hz
5 = dc to 5 kHz

As a standard practice, all converters are built in accordance with the requirements of MIL-STD-883B, including 168 hours of active burn-in.

Other Hybrid products

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)
- 16-bit microprocessor-compatible digital to synchro/resolver converter with double buffered inputs and 1 arc-minute accuracy (HDSR2006).
- 14-bit synchro(resolver)-to-digital converters pin-compatible with existing designs, but with superior performance (HSD/HRD1014)
- 10-bit synchro (resolver)-to-digital converters that are pin compatible with existing designs (HSD/HRD1510)
- 14/16-bit synchro (resolver) control transformer with 1 arc minute accuracy (HSCT/HRCT3006)
- 14-bit Digital-to-Synchro/Resolver converter that is pin-compatible with existing designs, with transformation and angular accuracy improvement of a factor of 2 to 4 (HDSR2504).

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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