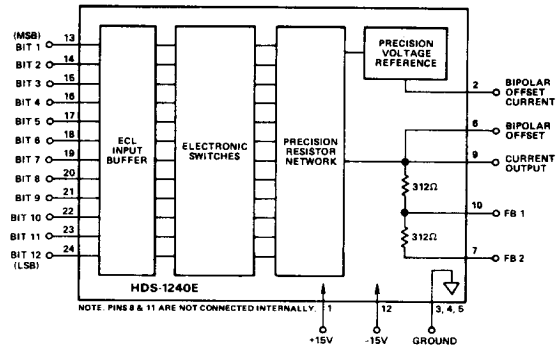
Ultra High Speed ECL Hybrid D/A Converter

HDS-1240E

FEATURES
12-Bit Settling Time to 40ns
Low Glitch Energy
ECL Compatible
Replacement for ADH-030, DA-4000, DAC397

APPLICATIONS
Graphic Displays - Random Scan
Digital VCO's
Waveform Generation
High-Speed ADC's

HDS-1240E FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The HDS-1240E is a 12-bit high current output hybrid IC D/A converter which has an output settling time of 40ns. Its inputs are compatible with standard ECL (emitter coupled logic), and it features an actively trimmed resistor ladder network for high accuracy. The HDS-1240E can be operated connection. For voltage output applications, the feedback resistors required for use with an external op-amp are built in to allow various voltage ranges without the need for external components. Additionally, the HDS-1240E features practically glitch-free operation without the need for external adjustments, and it operates on standard ±15 volt power supplies.

PIN DESIGNATIONS
HDS-1240E

PIN	FUNCTION	PIN	FUNCTION
1	+15 VOLTS	13	BIT 1 (MSB) INPUT
2	BIPOLAR OFFSET CURRENT	14	BIT 2 INPUT
3	GROUND	15	BIT 3 INPUT
4	GROUND	16	BIT 4 INPUT
5	GROUND	17	BIT 5 INPUT
6	BIPOLAR OFFSET	18	BIT 6 INPUT
7	FB 2	19	BIT 7 INPUT
8	N.C.	20	BIT 8 INPUT
9	OUTPUT	21	BIT 9 INPUT
10	FB 1	22	BIT 10 INPUT
11	N.C.	23	BIT 11 INPUT
12	-15 VOLTS	24	BIT 12 (LSB) INPUT

SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

Model	Units	HDS-1240E
RESOLUTION FS = Full Scale	Bits	12
LSB WEIGHT	μA	3.9
ACCURACY (Relative to FS)		
Linearity	% FS	±0.0125 max
Differential Linearity	% FS	±0.0125 max
Gain	% FS	±0.05 max
Zero Offset - Unipolar	μA	1
Zero Offset - Bipolar	μA	4
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C	±3 typ; ±5 max
Differential Linearity	ppm/°C	±3 typ; ±5 max
Gain	ppm/°C	25
Zero Offset	ppm/°C	10
DATA INPUTS		
Logic Compatibility		
Logic "1"		
Voltage Range (Operating)	V	-0.81 to -0.96
Voltage Range (Absolute max)	V	0
Current	mA	10 max
Logic "0"		
Voltage Range (Operating)	V	-1.65 to -1.85
Voltage Range (Absolute min)	V	-6
Current	μA	1 max
Coding		Complementary Binary (CBN) for Unipolar; Complementary Offset Binary (COB) for Unipolar
OUTPUT		
Current - Unipolar	mA	0 to -16
Current - Bipolar	mA	±8
Compliance	V	+0.5V to -1.1V
Impedance	Ω	200
Capacitance	pF	25
SPEED PERFORMANCE		
Settling Time[1]		
For FS Input Change		
to 1% of FS	ns	20 typ; 30 max
to 0.1% of FS	ns	35 typ; 50 max
to 0.0125% of FS	ns	40 typ
For 1LSB Change from		
011...11 to 100...00 to 0.0125%	ns	30 typ; 35 max
Internal Skewing Time	ps	400 typ; 800 max
Output Time Constant	ps	3 into 100Ω load
Glitch Energy (with 100Ω Load)	pV-s	150
	mA-ns	2.5
POWER REQUIREMENTS		
Voltage - Operating	V	+15 ±10%; -15 ±10%
Voltage - Absolute Limit	V	+18, -18
Current	mA	20 typ; 30 max; 60 typ; 80 max
Rejection Ratio	%/V	0.02 max
TEMPERATURE RANGE (Case)		
Operating		
HDS-1240E	°C	0 to +70
HDS-1240EM, HDS-1240EMB	°C	-55 to +100
Storage	°C	-55 to +125
THERMAL RESISTANCE[2]		
Junction to Air, θja (free air)		
HDS-1240E	°C/W	38
HDS-1240EM, HDS-1240EMB	°C/W	45
Junction to Case, θjc		
HDS-1240E	°C/W	15
HDS-1240EM, HDS-1240EMB	°C/W	12
MTBF[3]		
Mean Time Between Failure		
Calculated Using MIL Handbook-217	hours	$>1.356 \times 10^6$
PACKAGE OPTIONS[4]		HY24E, HY24G

NOTES
[1] Measured with output loaded with 100Ω.
[2] Maximum junction temperature is 150°C.
Specifications subject to change without notice.
[3] HDS-1240EMB calculated using MIL Handbook-217 Ground: Fixed Temperature Case = 60°C.
[4] See Section 19 for package outline information.

APPLICATIONS

The HDS-1240E is a current output D/A converter which is input compatible with standard ECL (emitter coupled logic). Each digital input controls an internal switch, which through a precision binary weighted resistor network, sets the output current of the device. Starting with the most significant bit (MSB) and proceeding toward the least significant bit (LSB), each lesser bit controls one-half the current value of the preceeding bit. Therefore, the MSB (Bit 1) controls 8mA, Bit 2 controls 4mA, and so on until the LSB is reached which has a weight of 3.9μA. Thus, the output of the D/A varies from 0 with all digital inputs at a logic "1" state to -16mA with all inputs at a logic "0" state. This operating condition is called unipolar. For bipolar operation, an 8mA current source is provided. When this current source is connected to the output, it will then swing from -8mA to +8mA. See Figures 1 and 2 for this hook-up.

Transfer Characteristics

With the DAC hooked-up as shown in Figure 1, the output will be 0 to -16mA. Since the output compliance is +0.5V to -1.1V, care must be taken not to let the output voltage exceed these limits. The input/output relationships are shown in the table below.

Analog Output		Digital Input Code
Unipolar	Bipolar	
0	+FS	111...11
-1/2LSB	+FS -1LSB	111...10
-1/4FS	+1/2 FS	100...00
-1/2 FS +1LSB	+1LSB	100...00
-1/2FS	0	011...11
-1/2 FS -1LSB	-1LSB	011...10
-3/4 FS	-1/2LSB	001...11
-FS +1LSB	-FS -1LSB	000...00

Table I. Coding Table

ANALOG OUTPUT

A. Normal Operation Without Amplification

The HDS-1240E is a current output D/A converter. However, the wide voltage compliance of +0.5V to -1.1V allows it to be used to generate an output voltage within this range which is proportional to the digital input code and the load impedance. When the DAC is operated in this mode the following formulae apply:

$$V_O = -0.016\ [R_t]$$

$$R_t = \frac{R_i \times R_L}{R_i + R_L} = \frac{200\ (R_L)}{200 + R_L}$$

Where: R_i = the internal resistance of the DAC (200Ω)
R_L = the external load resistance loading the DAC
R_t = the total resistance seen by the DAC output current, i.e., R_i in parallel with R_L.

In general, the output voltage of DAC is limited to 1V p-p. In this instance, from the above formulae, it can be determined that the maximum external load resistance will be about 90Ω. Since the bipolar offsetting provision is a true current source, this calculation does not differ even when the DAC is used in the bipolar mode. Full-scale gain may be adjusted by varying R_L (see Figure 4).

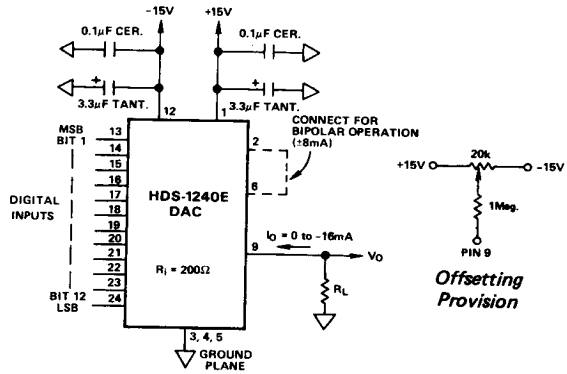

Figure 1. Current Output Operation

B. Operation with Voltage Amplification

There are certain applications that require more than the 1V p-p that is directly obtainable with the DAC output. In these circumstances, the use of an ultra-high speed operational amplifier is required. Figure 2 shows such an application utilizing the ADI Model HOS-050 op amp. The HDS-1240E DAC has built-in feedback resistors which are actively laser trimmed, and which eliminate the need for extra components. A variety of connections of these resistors allows various output voltages as shown in the table below. Care should be taken to keep all leads as short as possible, as the bandwidths encountered in these type circuits are quite high, and parasitics can be a very real problem. The power supply bypassing arrangement shown in Figure 1 should be used.

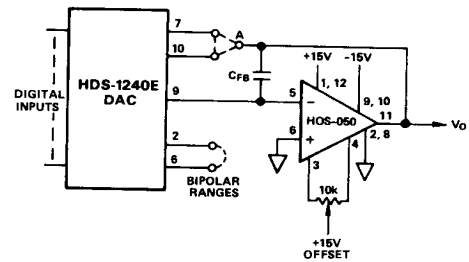

Figure 2. Voltage Output Operation

Voltage Range	Jumper Connections
±1.25V	7 to 9, 10 to A, 2 to 6
±2.5V	10 to A, 2 to 6
±5V	7 to A, 2 to 6
0 to +2.5V	7 to 9, 10 to A
0 to +5V	10 to A
0 to +10V	7 to A

Table II. Output Voltage Connections

NOTE: The value of Cfb should be optimized for best settling time without overshoot. If absolute accuracy of gain is required, a large value of resistance can be introduced in parallel with Pins 7 and 9 of the DAC.

High-Speed Low-Glitch Operation Suggestions

The HDS-1240E D/A offers the highest available speed. However, with this speed performance, certain precautions and operating conditions should be considered. You are now in the RF world.

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with 1μF (or larger) tantalum capacitors mounted between the ±15V supply lines and ground near the D/A (see Figure 1).
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 1 and 12 to ground (see Figure 1).
4. The D/A converter should be driven with ECL registers as physically close to the D/A as possible. The 10176 HEX "D" Master-slave flip-flop is recommended. The six most significant bits should come from the same package as shown in Figure 4. The six least significant bits should come from a second package.
5. Each digital input should be terminated with a 510Ω resistor connected between the input and -5.2V (see Figure 4).
6. If required, variable capacitors can be added to "deskew" the most significant bits for lowest glitch—although this is not usually required in many applications. These capacitors are added as shown in Figure 4 (C1-4), and are adjusted for minimum glitch energy.
7. Standard 24-pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/A's should be soldered directly into the printed circuit board without sockets.

ULTRA-LOW GLITCH OPERATION

For extremely low glitch requirements (<50 - 100pV-s), an HTS-0025 Track-and-Hold is recommended as a deglitcher (see Figure 3). The duration of the HDS-1240E D/A glitch is approximately 10ns. The hold time of the HTS-0025 should be at least 15ns to "mask out" the glitch.

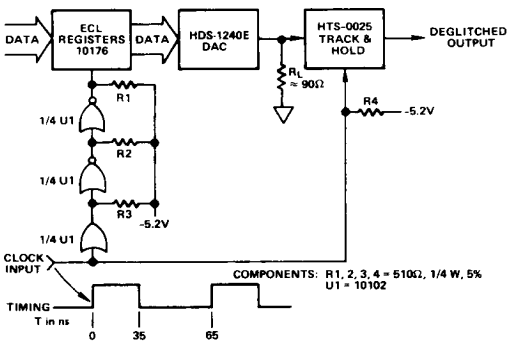

Figure 3. HTS-0025 Track & Hold Used with HDS-1240E D/A as Deglitcher @ 20MHz Update Rate

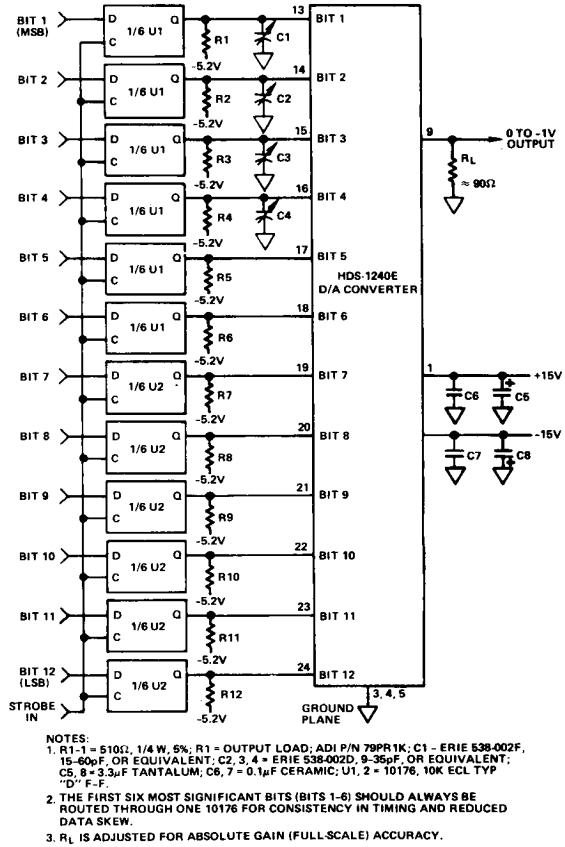

Figure 4. HDS-1240E — Typical Hook-Up and Test Circuit

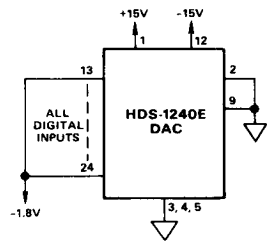

Figure 5. Recommended Burn-In Circuit

ORDERING INFORMATION

For commercial environment applications (0 to +70°C), order HDS-1240E. For extreme environment applications (-55°C to +100°C), order HDS-1240EM.