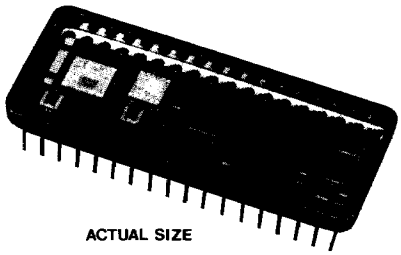
NATEL HDSR2006

Digital-to-Synchro/Resolver Converter Microprocessor Compatible 16-bit Hybrid

Features

- **Single 36-pin hybrid DDIP package**
- **1 arc-minute accuracy**
- **0.05% max scale factor variation (sin, cos conformance)**
- **4-quadrant digital-to-sin/cos conversion**
- **Microprocessor compatible (8 or 16 bit)**
- **Double buffered inputs**
- **Pin-programmable synchro or resolver output**
- **Pin-programmable reference input**
- **Pin-programmable set-up and test mode**
- **Requires only ±15-V power supplies**
- **TTL and CMOS compatible**
- **Hi rel MIL-STD-883B processing**
- **Priced at $495/USA price (HDSR2006-14S)**



ACTUAL SIZE

255 orig

006381

6381 NTL

HDSR2006

Applications

Polar to rectangular coordinate conversion
Missile and fire control systems
Flight instrumentation
Simulation systems
Digital phase shifting
Rotating PPI sweep
Radar and navigational systems
Axis rotation

Description

Offering both 8- and 16-bit microprocessor compatibility, the HDSR2006 is the world's first 16-bit hybrid digital-to-synchro/resolver converter. The HDSR2006 is, in effect, a versatile 4-quadrant multiplying digital-to-sin/cos converter.

With an accuracy of ±1 arc-minute and a scale factor variation of only ±0.05%, a wide range of applications become appropriate for this product. The most obvious is that of driving synchros or resolvers in radar systems (external power amplifier required). The very low scale factor variation and dc coupling on the outputs of the converter mean that distortion-free PPI (plan position indicator) displays can be developed without using any external correction modules.

Packaged in a standard 36-pin DDIP, the converter requires only ±15-V power supplies. The inputs are double-buffered, and the converter is TTL, standard CMOS and high-level CMOS compatible. The two programmable input registers (buffers) permit the converter to interface with a microprocessor data bus. Although designed to work with either 8- or 16-bit microprocessors, the converter may be used in conventional applications without any external components or additional connections. Multilayered hybrid construction allows a high level of circuit density in a very small package.

Reference voltages of either 115, 26 or 1.3 volts are selected by pin programming, without any requirement for external resistors.

Two self test functions are provided for test and/or calibration in different applications. The test mode is implemented digitally without disconnecting any inputs or disturbing the normal operation of the converter.

Microprocessor Compatibility

Two programmable input registers accept 16-bits from the microprocessor. Used in conjunction with an 8-bit data bus, each input register can be separately enabled to accept the 16-bit word in two 8-bit bytes. This is accomplished by setting HBE to Logic "High" (High Byte enable), to load 8 MSBs (most significant bits). And...setting LBE (Low Bytes enable) to Logic "High" to load 8 LSBs (least significant bits). The 16-bit data word is then parallel loaded into a holding register and processed through a multiplying Digital-to-Sin/Cos converter. Without the holding register, output transients would occur due to the two-byte loading scheme. The holding register is enabled by setting LDC (Load Converter) to Logic "High." When interfacing with a 16-bit data bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word.

For other applications: LDC, HBE and LBE can be controlled by system timing or left open to allow continuous updating. Internal active pullups allow HBE, LBE and LDC to be left open when the converter is being used in the continuous updating mode.

Logic Voltage and Digital Inputs

All digital inputs are TTL and CMOS compatible. For a +5 V-dc logic supply, the low threshold is 0.8 V-dc and the high threshold is 2.4 V-dc, thereby making it unnecessary to connect the logic supply to V_L (pin 36). For logic voltages between +5 V-dc and +15 V-dc, the switching thresholds can be increased by connecting the logic supply to V_L. When the logic supply is connected to V_L, the logic "0" threshold is $0.2V_L$, and the logic "1" threshold is $0.8V_L$. All data bits (B1 through B16) are actively pulled-down to ground. If the converter requires less than 16-bit resolution, the unused pins of data bits may be left open. Control signals LBE, HBE, LDC and Self Test Functions $\overline{STO}$ and $\overline{ST90}$ are actively pulled-up to the V_L supply voltage. When not required by your application, these pins may also be left open.

Transformation Ratio (Sin/Cos Conformity)

One of the outstanding features of the HDSR2006 is its very low transformation error of less than ±0.05%. Until recently, most converters had typical transformation ratio variations of from ±1% to ±7%. A few designs, including Natel's model 5112, had reduced this error to ±0.1%. In many synchro/servo systems this error is not critical, provided that the ratio of sine to cosine outputs is correct. However, in certain closed-loop control systems and other applications requiring independent sine and cosine accuracy, this variation is unacceptable. Coordinate transformation and PPI (sweep) display are examples of applications where the HDSR2006 would be an ideal choice.

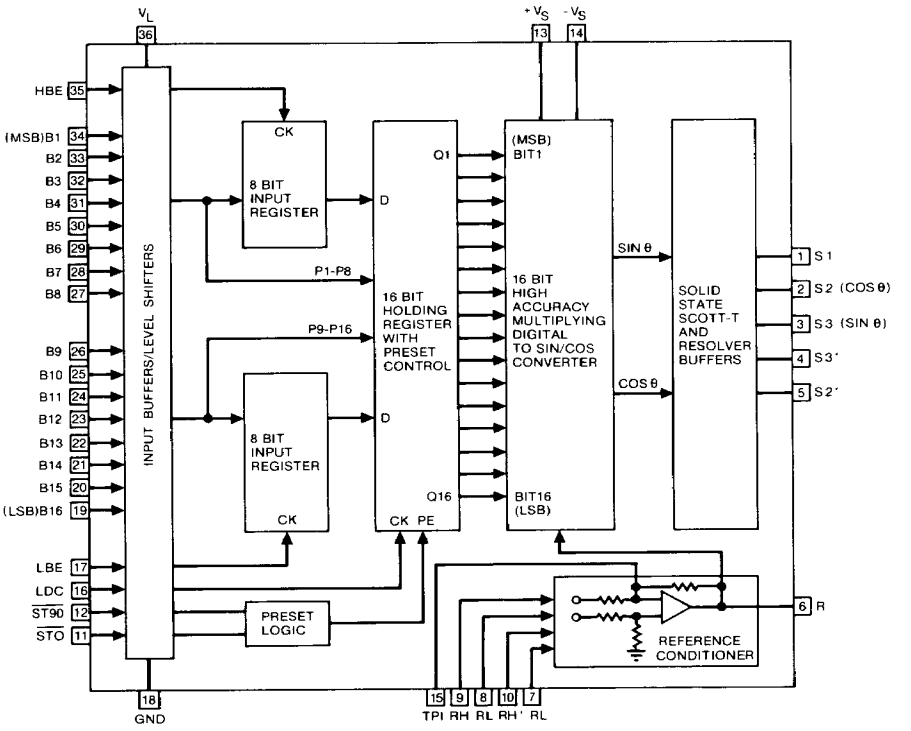


FIGURE 1

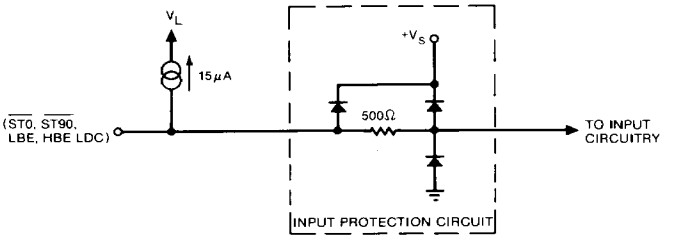


FIGURE 2 Active Pull-Up Circuit

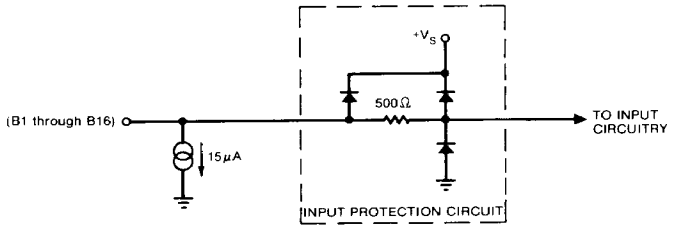


FIGURE 3 Active Pull-Down Circuit

Accuracy

Model HDSR2006 converters are available with angular accuracies of 1, 2 and 4 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring special compensation circuits.

Matched thin film resistors are used at the Reference input and the Synchro and Resolver outputs to assure excellent performance over the operating temperature range. All gain resistors are actively laser trimmed to achieve precise performance.

Specifications

PARAMETER	VALUE	REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)	MSB = 180°, LSB = 0.0055°
Accuracy	±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minute (option V)	Accuracy applies over operating temp. range
Scale factor Variation (Transformation ratio Error)	±0.05% maximum	Simultaneous amplitude variation in all output lines as a function of digital angle.
Output Settling time	20μsec maximum to accuracy of the converter	For any digital step change
Reference Input		
Internal Resistors	Pin-programmable for 1.3, 26 and 115 V-rms (±10%)	Differential Solid State Input
External Resistors	Programmable for voltages 1.3 to 115 V-rms by adding two external resistors	See Reference level adjustment
Frequency Range	dc to 1000 Hz dc to 10 kHz	Reduced accuracy
Input Impedance		
RH - RL	Differential 200 k Ω±0.25% Single Ended 100 k Ω±0.25%	
RH' - RL'	Differential 10 k Ω±0.25% Single Ended 5 k Ω±0.25%	
Common Mode Voltage Range		
26 V-rms (RH-RL)	±80 V peak maximum	RH', RL' unterminated
115 V-rms (RH-RL)	±200 V peak maximum	RH', RL' connected to GND
1.3 V-rms (RH'-RL')	±4 V peak maximum	RH, RL Unterminated
Common Mode Rejection Ratio	50dB minimum	
Analog Outputs		Using Internal Resistors
Synchro Format	11.8 V-rms line-to-line ±0.2%	S1, S2, S3 outputs
Resolver Format	6.81 V-rms ±0.2%	Sin, Cos output
"R" Output	2.27 V-rms Nominal	
Output Current	2 mA-rms maximum	Short circuit proof
DC Offset		
Synchro/Resolver	±50 mV maximum	Offset is specified with respect to GND
"R" output	±10 mV maximum	
Digital Inputs		CMOS tansient protected
Logic Voltage Levels		
Logic "0"	-0.3 V-dc to 0.8 V-dc	Does not need external logic voltage (Pin 36 not connected)
Logic "1"	+2.4 V-dc to $+V_S$	
Logic "0"	-0.3 V-dc to 0.2 V_L	Using External V_L (Pin 36)
Logic "1"	0.8 V_L to V_L	$6 \leqslant V_L \leqslant +V_S$ @ 1 mA
Input Currents		
Data Bits (B1-B16)	15 μA typical, "active" pull down to Ground (GND)	For less than 16-bits input, unused pins can be left unconnected
Control Signals (HBE, LBE, LDC, $\overline{ST0}$, $\overline{ST90}$)	-15 μA typical, "active" pull up to Logic Supply (V_L)	When not used pins can be left unconnected
Register Controls		
HBE	Logic "1"	8 MSBs enter high byte input register
	Logic "0"	High byte register remains unaffected
LBE	Logic "1"	8 LSBs enter low byte input register
	Logic "0"	Low byte register remains unaffected
LDC	Logic "1"	Data from two input registers is transferred to holding register
	Logic "0"	Data in holding register remains unaffected
Pulse Width	600 nsec minimum	For guaranteed data transfer
Data Set-up time	200 nsec minimum	Before data transfer
Data Hold time	200 nsec minimum	Before input data changes
Power Supplies		
Supply voltages ($\pm V_S$)	±15 V-dc ± 5%	Without output clipping for nominal ac voltages
Supply Currents	±30 mA maximum	
Supply Rejection	80 dB typical	
Physical Characteristics		
Type	36 PIN Double DIP	3 standoffs are added to the package to insulate it from printed circuit board traces. (Standoffs included in 0.21-inch height dimension).
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	
Weight	0.6 oz (17 g) max	

Pin Designations

V_L	Logic Supply Voltage (may be left open for 5 V-dc logic)
GND	Power Supply Ground Digital Ground Analog Signal Ground
B1 - B16	Parallel Data Input Bits B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree
HBE	High Byte Enable - Data inputs B1 through B8 enter the input buffer register when HBE is set to a Logic "High." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected ty digital activity at the input data bits B1 - B8 pins.
LBE	Low Byte Enable - Data inputs B9 through B16 enter the input buffer register when LBE is set to Logic "High." When LBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9 - B16 pins.
LDC	Load Converter - When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the 16-bit holding register. When LDC is set to Logic "Low," the converter is in the hold mode and is not affected by digital activity in the input registers.
Note:	For continuous updating HBE, LBE and LDC may be left open. Internal active pull-up will force these functions to a Logic "High"
TP1	Test Point - Leave this pin open (no external power should be applied to this pin)
$+V_S$, $-V_S$	Supply Voltages - Typically ±15 V-dc
$\overline{ST0}$, $\overline{ST90}$	Self Test function - For normal operation leave these pins open. (See text for their use in self test mode)
RH, RL, RH', RL'	Reference Voltage Input - Pin programmable for 1.3, 26 and 115 V-rms inputs (See text for connections)
R	Buffered Reference Voltage - Nominal output 2.27 V-rms for standard input reference voltages
S1, S2, S3, S2', S3'	Output Analog Signal Pin programmable for Synchro or Resolver output (See text for connections)

S1	1	36	V_L
(COS) S2	2	35	HBE
(SIN) S3	3	34	B1
S3'	4	33	B2
S2'	5	32	B3
R	6	31	B4
RL'	7	30	B5
RL	8	29	B6
RH	9	28	B7
RH'	10	27	B8
$\overline{STO}$	11	26	B9
$\overline{ST90}$	12	25	B10
$+V_S$	13	24	B11
$-V_S$	14	23	B12
TPI	15	22	B13
LDC	16	21	B14
LBE	17	20	B15
GND	18	19	B16

Fig. 4 HDSR2006 Pin Assignments

Absolute Maximum Ratings

Reference Input ..... Twice specified Voltage
Power Supply Voltages ($\pm V_S$) ..... ±18 V-dc
Logic Voltage (V_L) ..... 4.5 V-dc to $+V_S$
Digital Inputs ..... -0.3 V-dc to V_L
Storage Temperature ..... -65° C to +135° C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply be turned off. Decoupling capacitors are recommended on the $+V_S$ and $-V_S$ supplies. A 1 μF tantalum capacitor in parallel with 0.01 μF ceramic capacitor should be mounted as close to the supply pins as possible.

Caution: Reversal of $+V_S$ and $-V_S$ power supply connections will result in permanent damage to the converter.

Reference Level Adjustment

Operation of the HDSR2006 is very similar to that of a multiplying digital-to-analog converter. The sine and cosine outputs are directly proportional to and have the same waveform as the reference voltage. Any distortion or harmonics present at the reference will appear at the output lines.

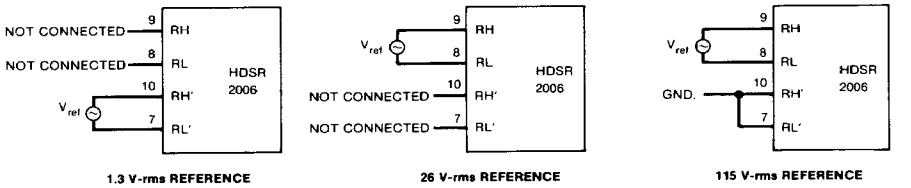
Internal resistors permit pin-programming for three standard reference voltages with the normal analog output (6.81 V-rms for Resolvers and 11.8 V-rms for Synchros). The connections for the three reference voltages -- 1.3 V-rms, 26 V-rms and 115 V-rms -- are shown in figure 5. Proportionally higher or lower voltages will be obtained for analog outputs when higher or lower reference voltages are used.

With ±15-V supply voltages, clipping of the output waveform will occur if the reference amplitude exceeds the specified value by more than 10%.

To obtain nominal analog output with non-standard reference voltages, two external resistors are required. The input resistance for RH and RL is 100 kΩ. RH' and RL' are each 5 kΩ. The circuit configuration for reference voltages other than nominal is shown in figure 6.

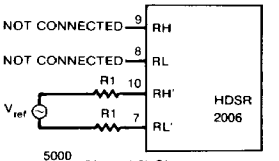
For high reference voltages (26 to 115 V-rms), the resistor values for R1 might become too large to be practical. In those situations the external resistor should be connected as shown in figure 7.

The value of R2 in figure 7 is a nonlinear function of V_{ref}. Contact the factory for application notes.



1.3 V-rms REFERENCE | 26 V-rms REFERENCE | 115 V-rms REFERENCE

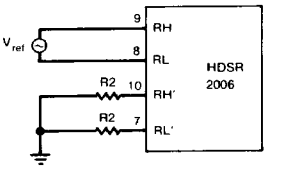
FIGURE 5



$R1 = \frac{5000}{1.3}(V_{ref} - 1.3)$ Ohms

V_{ref} = 1.3 V-rms to 26 V-rms

FIGURE 6



V_{ref} = 26 V-rms to 115 V-rms

FIGURE 7

$E_{S3-S1} = K_1 V_{ref} (1 + n) \sin\theta$

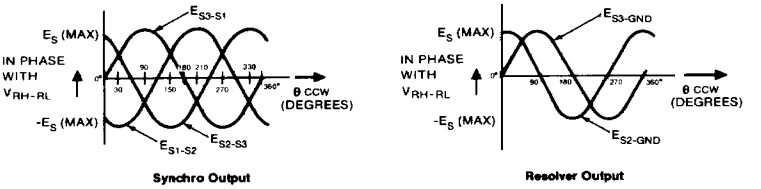
$E_{S2-S3} = K_1 V_{ref} (1 + n) \sin(\theta + 120°)$

$E_{S1-S2} = K_1 V_{ref} (1 + n) \sin(\theta + 240°)$

$E_{S3-GND} = K_2 V_{ref} (1 + n) \sin\theta$

$E_{S2-GND} = K_2 V_{ref} (1 + n) \cos\theta$

K is the gain of the converter and n is the scale factor variation as a function of digital angle. (± 0.05%)



Synchro Output | Resolver Output

FIGURE 8 Synchro/Resolver Outputs

Synchro/Resolver Connections — Output Phasing and Gain

The connections for synchro and resolver outputs are shown in figure 8. For standard reference voltages, the gain of the converter is factory adjusted to provide voltages of 6.81 V-rms for maximum sine and cosine outputs in the resolver configuration and 11.8 V-rms in the synchro configuration. The gain accuracy using internal resistors is ±0.2%. Applications requiring exact gain can be accommodated by using external resistors (see Reference Adjustment). Contact factory for gain accuracies of better than ±0.2%, if it is not practical to use external resistors.

Self-test Functions $\overline{ST0}$ and $\overline{ST90}$

Another of the unique features of the HDSR2006 is the inclusion of two built-in test functions, $\overline{ST0}$ and $\overline{ST90}$. Using these two test functions it is possible to preset two test angles of 0° and 90°, independent of the digital inputs.

There are 4 modes of operation controlled by $\overline{ST0}$ and $\overline{ST90}$. These modes are indicated by the Truth Table for Self Test Functions, (See table on page 6) and are defined as follows:

Normal Mode ($\overline{ST0}$ = 1, $\overline{ST90}$ = 1). This is the normal operating mode of the converter, with the input registers controlled by HBE and LBE and the holding register controlled by LDC.

Test 0° Mode ($\overline{ST0}$ = 0, $\overline{ST90}$ = 1). This condition presets the 0° test angle in the holding register. Input register contents and operation remain unaffected.

Test 90° Mode ($\overline{ST0}$ = 1, $\overline{ST90}$ = 0). This condition presets the 90° test angle in the holding register. Input register contents and operation remain unaffected.

Continuous Conversion Mode ($\overline{ST0}$ = 0, $\overline{ST90}$ = 0). This condition enables the holding register for inputs B1 through B16, i.e. the analog outputs follow digital input continuously. Input register contents previously latched are unaffected. Restoration of the normal mode, followed by an LDC pulse, transfers the previously latched data from the input registers to the holding register.

Truth Table for Self Test Functions

$\overline{ST0}$	$\overline{ST90}$	Mode	Remarks
1	1	Normal	Normal operation
0	1	Test 0°	Holding register preset to 0°, input register operation unaffected
1	0	Test 90°	Holding register preset to 90°, input register operation unaffected
0	0	Continuous conversion	Holding register preset to inputs B1-B16, input register operation unaffected

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 9. Inputs LBE, HBE and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs B1-B16 is continuously converted to Synchro or Resolver at the analog outputs. For applications requiring less than 16-bit resolution, unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B1-B16.

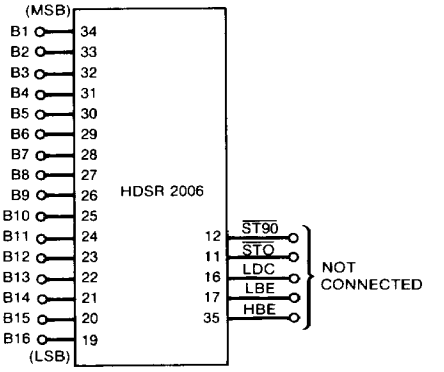


FIGURE 9 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 10. As shown in the figure 11 timing diagram, the 8 LSBs (B9-B16) are transferred to the low-byte input register when LBE is a logic "1". LBE can be "High" when data bits are changing, but must remain "High" for a minimum of 800 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE goes "Low". Bits B1-B8 are transferred to the high-byte input register when HBE is a logic "1". The timing requirements are the same as those for LBE. Data are transferred from the two input registers to the holding register when LDC (load converter) is at logic "1". If LDC is at logic "0", the contents of the holding register are latched and remain at their previous values, unaffected by changes at the data inputs or input registers.

Note that LBE, HBE and LDC are level-actuated functions. Note also that the converter can accept reverse order of loading high-byte followed by low-byte.

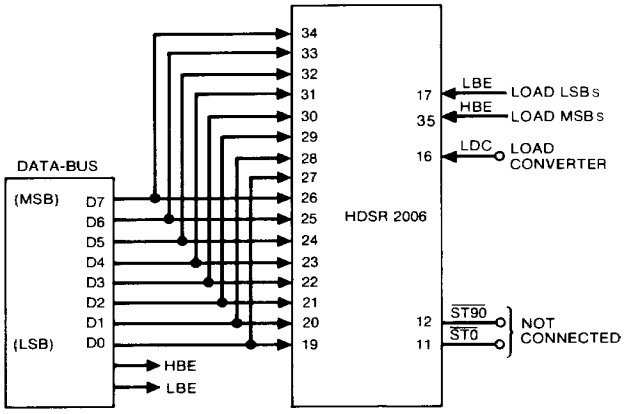


FIGURE 10 Digital Connections for Two-Byte Loading

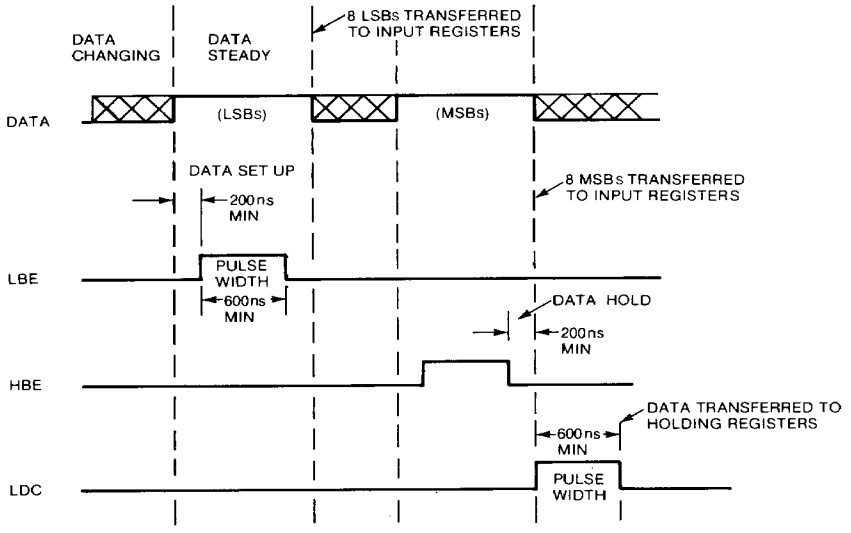


FIGURE 11 Two-Byte Loading

Single Byte Loading

Single 16-bit byte loading is illustrated in figure 12. As shown in the timing diagram (figure 13), 200 nsec after the data is stable, the input angular information is transferred to the holding register when LDC is at a logic "1". LDC is a level-actuated function and must remain high for the times specified in the timing diagram.

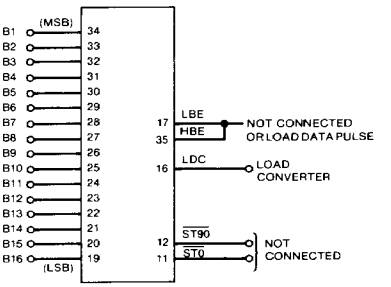


FIGURE 12 Digital Connections for One Byte (16 bits) Loading

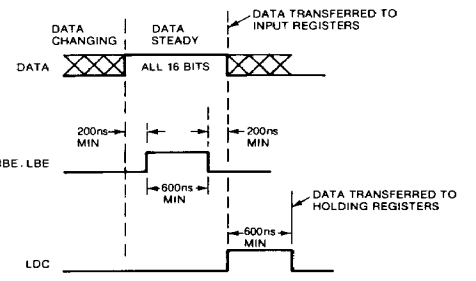


FIGURE 13 Single-Byte Loading

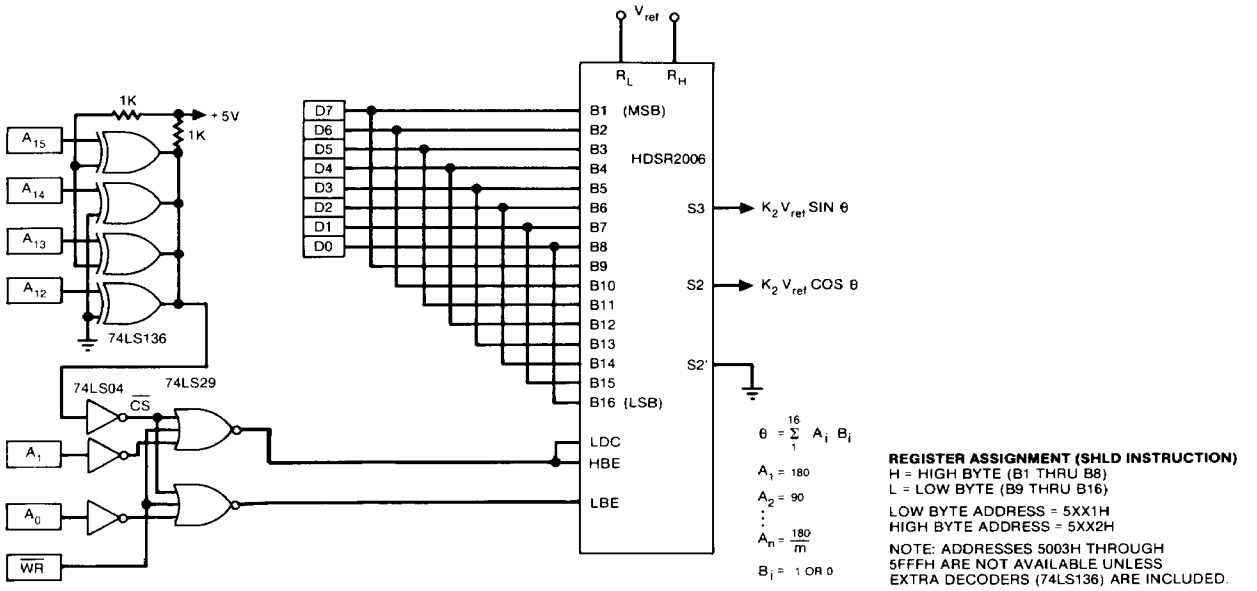
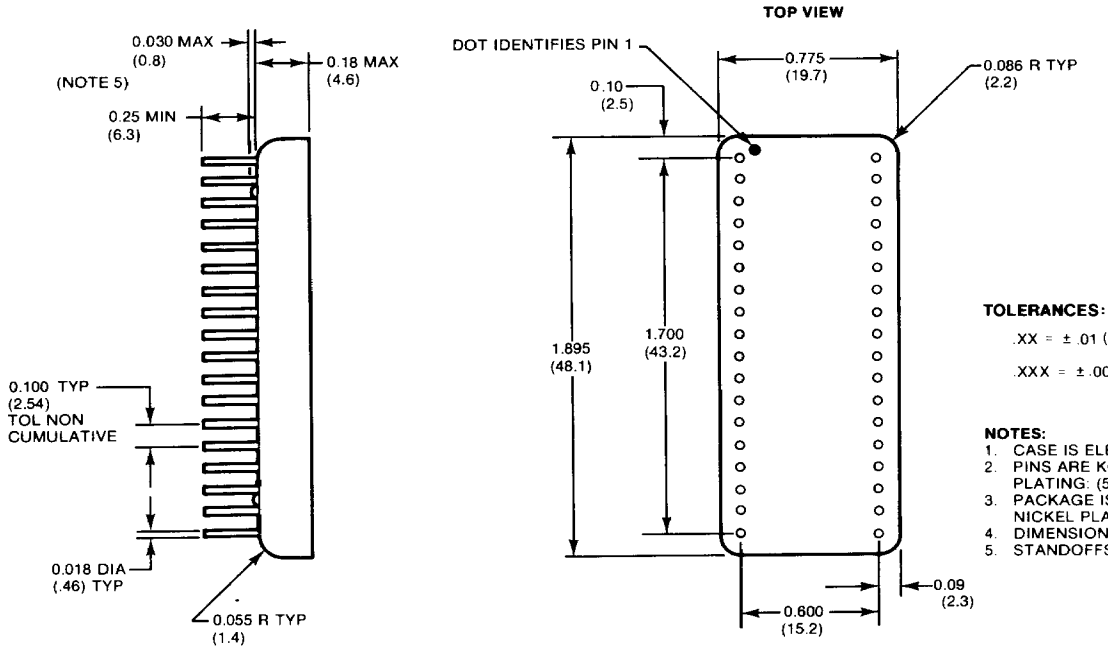


FIGURE 14 8080μP–HDSR2006 Memory Mapped Interface Connection Diagram

Memory Mapped I/O With 8080 Microprocessor

A typical example of a microprocessor interface using memory mapping and an 8080-type 8-bit μP is shown in figure 14. Memory-mapped I/O enables the HDSR2006 to receive data from the μP using the same instructions that are required to transfer data to and from memory locations. This means that, in addition to the accumulator, any of the internal registers can be used to transfer data to the converter. This is a particularly attractive feature, since the use of the SHLD instruction permits transfer of a 16-bit output to the HDSR2006 with a single instruction.

As is shown in figure 14, the control signals necessary to operate the converter are provided by the external gating structure. The CS signal (Chip Select) is generated by decoding the address bus with the 74LS136 exclusive-or gates, hard-wired to the selected address. In the example, only the upper 4 address lines are decoded. When the address 5XXXH is decoded, CS goes low enabling the 74LS29 control gates. When the selected address is 5XX1H and the $\overline{WR}$ line goes low, D0-D7 are transferred to the low-byte input register. When $\overline{WR}$ returns to high, LBE goes low, latching the data. Using the SHLD instruction, the next processor cycle will increment the address to 5XX2H and output the next byte of data. When $\overline{WR}$ again goes low, HBE and LDC go high, transferring both data bytes to the converter's 16-bit holding register, at which time the conversion takes place. The data format for loading the H and L registers is shown below:



MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HDSR2006 - T F A

Temperature Range
1 = 0° C to +70° C
2 = -25° C to +85° C
3 = -55° C to +125° C

Frequency Range
4 = dc to 1000 Hz
5 = dc to 10 kHz

Accuracy
S = ±4 arc-minutes
H = ±2 arc-minutes
V = ±1 arc-minute

As a standard practice, all converters are built in accordance with the requirements of MIL-STD-883B, including 168 hours of active burn-in.

Other Hybrid products now in 36 pin DDIP size:

- 16-bit microprocessor-compatible synchro/resolver-to-digital converter, with 3 state output, operating from a single +5-V power supply (HSRD1006)

Other Hybrid products to be introduced in the next six months:

- 14-bit synchro/resolver-to-digital converters pin-compatible with existing designs, but with superior performance
- 14/16-bit multiplexed synchro/resolver-to-digital converters
- 14/16-bit SSCT with high accuracy

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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