# ECL GATE ARRAY

# HE2000

## PRODUCT DESCRIPTION

The HE2000 Gate Array (Figure 1) is a 300 picosecond, 2000 equivalent gate density Very Large Scale Integration (VLSI) monolithic integrated circuit built using Honeywell's ADB-II™ fabrication process. The array is composed of an uncommitted array of Current-Mode-Logic gates (Figure 2) and ECL 10K/KH compatible I/O cells. Up to 2000 gates are autoroutable, to provide the advantages of both VLSI and proprietary design.

Designing with the HE2000 is easy and fast, requiring only conventional logic design, logic simulation, and test pattern generation. The computer-aided-design and autorouting methodologies are similar to those used for printed circuit boards.

Logic functions are predefined by Honeywell and are implemented by automatically interconnecting the macrocells, using two layers of metal routing. A third layer of metal is used for power and ground bus distribution. Both cell intraconnection and routing of power buses are invisible to the user. For external interface, up to 140 ECL 10K/KH I/O buffers can be specified. Sixty-four buffers are dedicated ECL 10K/KH drivers.

The basic circuit technique used to implement logic functions is a two-level series gated CML structure. This technique gives maximum flexibility and performance in implementing a given function. Macrocells such as adders, decoders, latches, and flip flops are built using only one layer of metal within a cell. This eliminates many interconnects normally done in the routing channels of a gate array, simplifying the autorouting task.

Compared to ECL internal gate arrays, the use of the HE2000 with its lower power, higher component density and more efficiently built macrocells results in substantial performance improvement (circuit speed), and the increased use of on-chip components reduces system costs.

The ultra high packing density of the HE2000 offers up to a 110-to-1 reduction in system component count when compared with similar systems built using conventional SSI/MSI ECL logic functions. The user obtains a degree of optimization like that of a full custom design and the quick turnaround time of a semicustom part.

## FEATURES

- **Customer programmable VLSI**
- **2000 equivalent (OR/NOR) gates**
- **140 ECL 10K/KH compatible I/O cells**
- **Input buffer delay: 0.3 ns typical**
- **Internal gate delay: 0.3 ns typical**
- **Output buffer delay: 1.0 ns typical**
- **Commercial operating temperature range**
- **Power dissipation: 3.5 watts typical**
- **Series gated CML internal logic functions**
- **Ceramic 173-pin-grid array package**

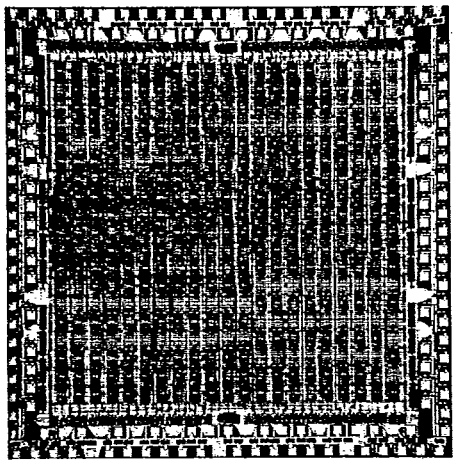

*Figure 1. HE2000 Gate Array*

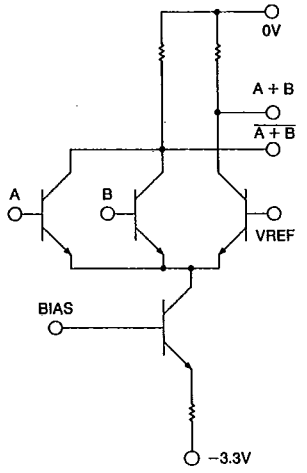


*Figure 2. CML Two-Input OR/NOR Gate*



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## COMPUTER-AIDED-DESIGN SYSTEM

Honeywell's Software Toolkit™ for VLSI gate array design is built around industry standard software programs. Most importantly, a standardized design language, Mentor SIM™, is available for logic simulation. This language is used hierarchically to define complex logic functions in a computer readable data base. The data is then accessed by other software programs for simulation, analysis, autorouting, and array fabrication.

In addition to Mentor SIM, the Software Toolkit contains programs for schematic entry, netlist generation, timing verification, design statistic analysis, loading/fanout analysis, media delay feedback/analysis, and test program compilation. Industry standard programs are also available for automatic placement, automatic routing, and interactive graphics editing.

Honeywell supports the Software Toolkit for customers with a variety of in-house design automation capabilities. A set of tools hosted on popular workstations provides complete schematic-through-PG tape capability in the hands of the system designer. Customers can use the Software Toolkit at Honeywell's Colorado Springs Design Center or in their own facility.

## FOR CUSTOMERS WITH MENTOR GRAPHICS ENGINEERING WORKSTATIONS

Mentor Graphics provides the following IDEA 1000™ programs as part of the Software Toolkit:

SYMED™ Mentor symbol generation package used with Honeywell-developed macrocell symbols. User may create new macrocell symbols using the macrocell library provided.

NETED™ Mentor schematic entry package used with Honeywell developed macrocells. User calls symbols from a library and interconnects them to implement his design.

SIM™ Mentor logic simulation package used with Honeywell developed macrocells. User provides input patterns to functionally debug the design.

EXPAND™ Mentor design expansion package used with Honeywell developed macrocells. Used for removing design hierarchy (nesting of macrocells) from design file prior to autoplacement.

Honeywell provides the following programs as part of the Software Toolkit:

LOADS™ Honeywell developed logic rules check and load modeling program. Informs the user of illegal loading or electrical violations. Also modifies macrocell propagation delays based on junction temperature, fanout, and power supply voltage.

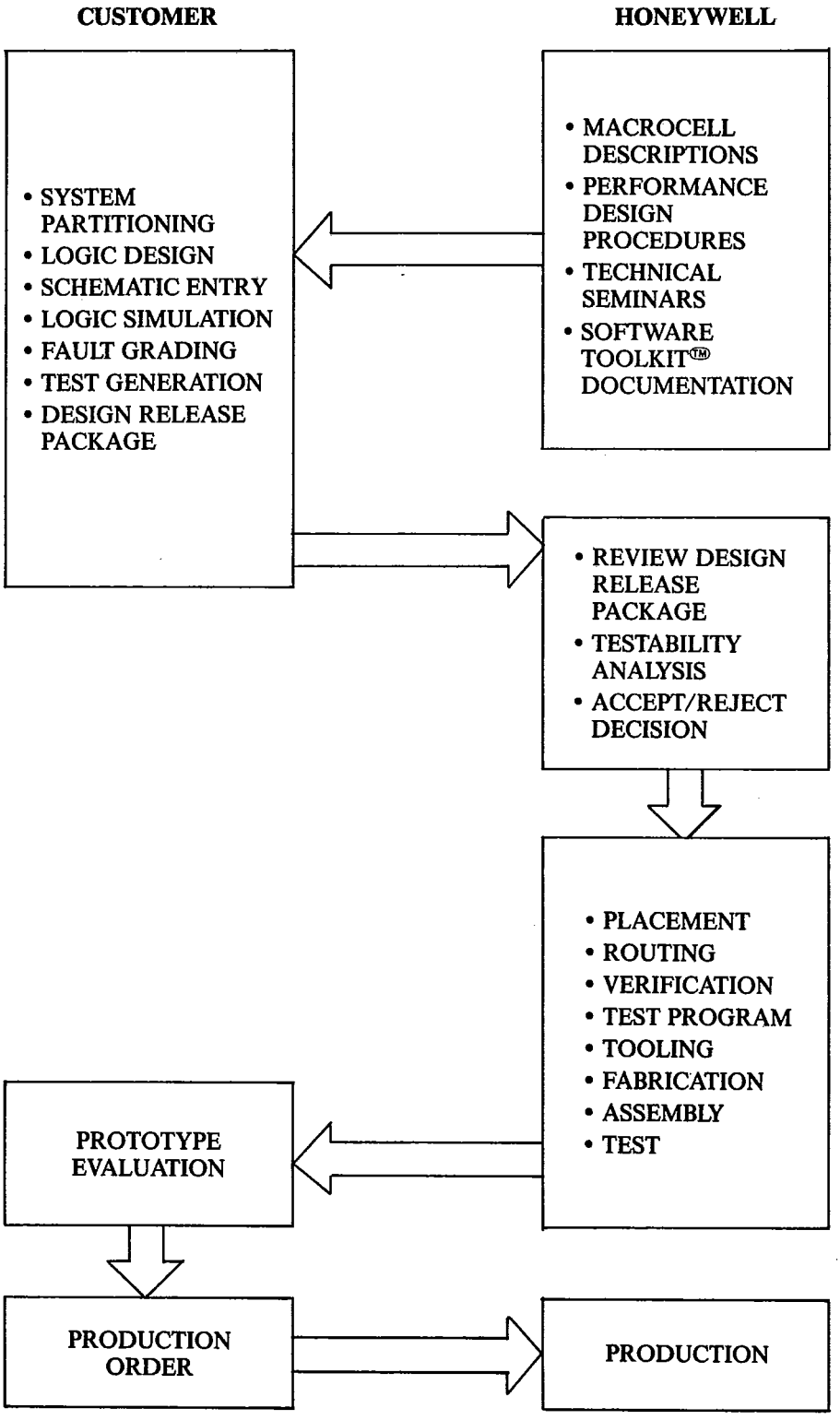
STATS™ Honeywell developed design statistics report. Lists chip power, cell count and utilization. Informs user of either cell count or I/O count exceed maximums for the specific gate array.

WIRES™ Honeywell developed wire delay calculation program. Lists all nets by line length and delay with error reporting for nets exceeding specified limits. Recomputes user design files with user specified temperature and actual wire delays.

TESTS™ Honeywell developed automatic test program compilation software. Takes functional test vectors from logic simulation and parametric test requirements to generate Series 20 compatible test tapes.

Ask your local Honeywell sales representative for further information on the Software Toolkit.

## GATE ARRAY DEVELOPMENT FLOW



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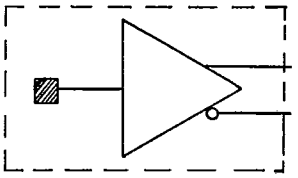
## INPUT/OUTPUT CELLS

All signals within the array interface to external pins through I/O buffers located around the device perimeter. A description plus the logic and schematic representations for each I/O cell are shown in Figure 3.

**INPUT BUFFERS** **(I01)**

**DESCRIPTION:** ECL compatible input buffer with CML ouputs.

**LOGIC:**

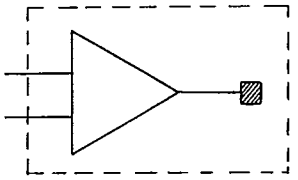


(I01)

**OUTPUT BUFFERS**

**DESCRIPTION:** 50 Ω ECL output buffer with non-inverting output.

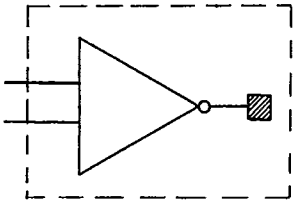
**LOGIC:**



(O01)

**DESCRIPTION:** 50 Ω ECL output buffer with inverting output.

**LOGIC:**

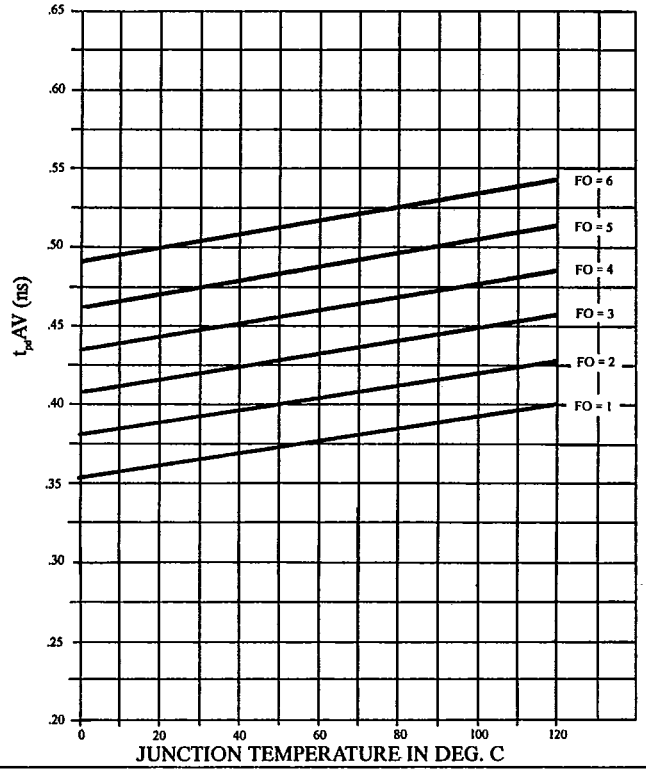


(O02)

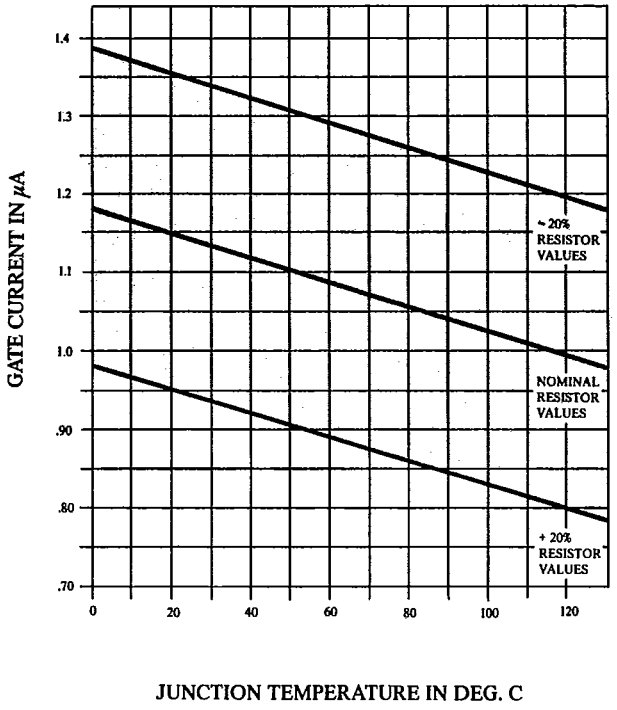
*Figure 3. I/O cells*

## TYPICAL PERFORMANCE CHARACTERISTICS

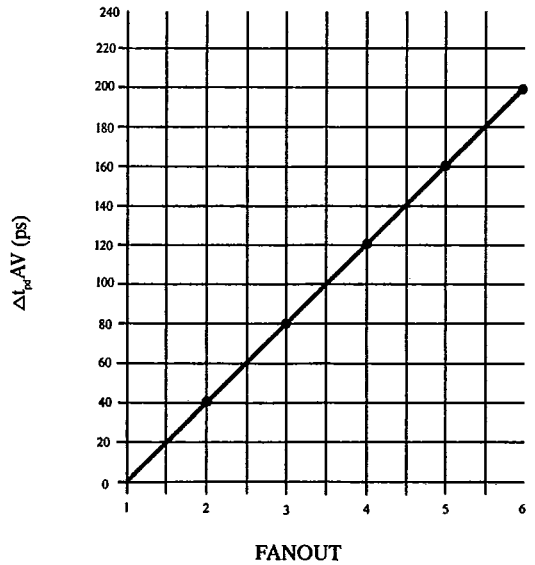
### HE2000 P02 GATE DELAY VS. TEMPERATURE



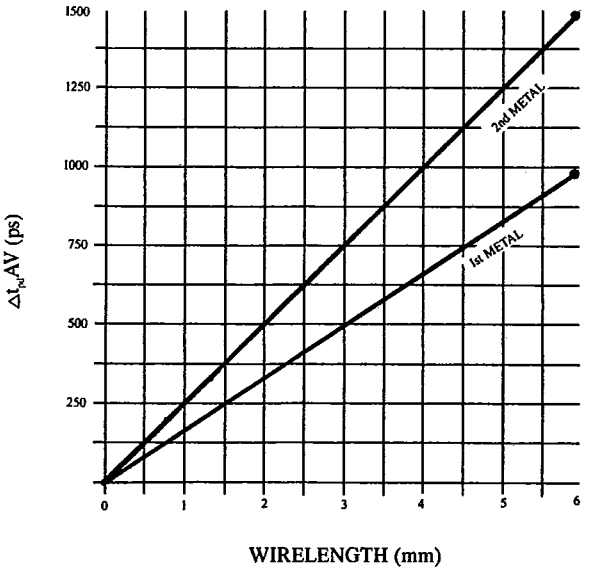

### P02 (TWO INPUT OR/NOR GATE CURRENT VS. TEMPERATURE




### P02 $\triangle t_{pd}$AV VS. FANOUT (T = 25° C)




### P02 $\triangle t_{pd}$AV VS. WIRELENGTHS (T = 25° C)



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## POWER DISSIPATION

The typical power dissipation of the HE2000 Gate Array is given by the following equation.

Typical Power (mW) = 3.3 x number of CML current sources
+ 294 mW for reference generators
+ 16.5 x number of 50 ohm drivers
+ 4.3 x number of input buffers

Power dissipated in the output emitter-follower transistor and termination resistor must be calculated separately.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CC1}$ | ECL ground | | 0 | | V |
| $V_{CC2}$ | CML ground | | 0 | | V |
| $V_{EE}$ | CML power supply | –3.450 | –3.300 | –3.150 | V |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |
| $F_{MAXT}$ | Maximum Internal Flip Flop Toggle Frequency | | | 500 | MHz |
| $F_{IN}$ | Maximum Input Frequency At Package Pin[1] | | | 300 | MHz |

[1]Package selection will determine the maximum input frequency. Consult Honeywell.

## ABSOLUTE MAXIMUM RATINGS[2]

| PARAMETER | DESCRIPTION | RATING | UNIT | PARAMETER | DESCRIPTION | RATING | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC1}$ | ECL ground | 0.0 | V | $V_{OH}$ | Output "1" voltage | –.700 | V |
| $V_{CC2}$ | CML ground | 0.0 | V | $V_{OL}$ | Output "0" voltage | –1.615 | V |
| $V_{EE}$ | CML power supply | –8.000 | V | $T_A$ | Ambient operating temperature | +85 | °C |
| $V_{IH}$ | Input "1" voltage | –.700 | V | $T_J$ | Junction operating temperature | +120 | °C |
| $V_{IL}$ | Input "0" voltage | –1.440 | V | | | | |

[2]COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions

| PARAMETER | | TEST CONDITIONS | LIMITS (COMMERCIAL) | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **CML GATE (Internal)** | | | | | | |
| $I_{CC2/G}$ | Power supply current per current source[3] | $V_{EE}$ = –3.3V, $V_{CC2}$ = 0.0V | .800 | 1.100 | 1.400 | mA |
| ILF | Input load factor | | | 1 | | Unit load |
| FO | Fanout | | | | 6 | Unit load |
| $t_{pdAV}$ | Average propagation delay (Inverter) | $V_{EE}$ = –3.3V, $V_{CC2}$ = 0.0V, fanout = 2 CML Inverters | — | .380 | .450 | ns |

[3]Typical applications estimate 2.5 gates/current source.

## DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions

| PARAMETER | | TEST CONDITIONS | COMMERCIAL LIMITS MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT BUFFER** | | | | | | **(I01)** |
| $I_{EE}$ | Power supply current | $V_{EE}$ = –3.3V ± 5% | 1.05 | 1.30 | 1.55 | mA |
| $I_{INH}$ | Input high current | $V_{EE}$ = –3.3V ± 5%, $V_{IH}$ = Max | | | 50 | μA |
| $I_{INL}$ | Input low current | $V_{EE}$ = –3.3 V ± 5%, $V_{IL}$ = Min | | | 0.5 | μA |
| $t_{PDLH}$ | Propagation delay, low-to-high. Fanout = 1 CML load | (See Figure 4a) | | .330 | .470 | ns |
| $t_{PDHL}$ | Propagation delay, high-to-low. Fanout = 1 CML load | (See Figure 4a) | | .260 | .370 | ns |
| $t_{PDLH}$ | Propagation delay, low-to-high. Fanout = 4 CML loads | (See Figure 4a) | | .490 | .580 | ns |
| $t_{PDHL}$ | Propagation delay, high-to-low. Fanout = 4 CML loads | (See Figure 4a) | | .490 | .580 | ns |
| FO | Fanout | | | | 6 | Unit load |

| PARAMETER | | TEST CONDITIONS | TEMPERATURE $T_A$ = 0°C MIN. | $T_A$ = 0°C MAX. | $T_A$ = 25°C MIN. | $T_A$ = 25°C MAX. | $T_A$ = 70°C MIN. | $T_A$ = 70°C MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **INPUT BUFFER** | | | | | | | | | **(101)** |
| $V_{IH}$ | Input high voltage | $V_{EE}$ = –3.3V ± 5% | –1.17 | | –1.13 | | –1.07 | | V |
| $V_{IL}$ | Input low voltage | $V_{EE}$ = –3.3V ± 5% | | –1.48 | | –1.48 | | –1.48 | V |

## DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions

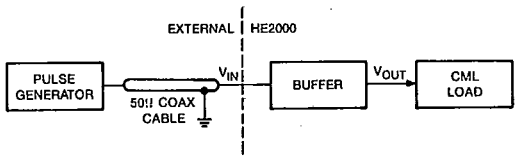
| PARAMETER | | TEST CONDITIONS | COMMERCIAL LIMITS MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OUTPUT BUFFERS—50 Driver** | | | | | | **(O01, O02)** |
| $I_{EE}$ | Power supply current | $V_{EE}$ = –3.3V ± 5%, $V_{CC2}$ = 0.0V | 4.0 | 5.0 | 6.0 | mA |
| $t_{PDHL}$ | Propagation delay, high-to-low output | (See Figure 4) | | 1.000 | 1.400 | ns |
| $t_{PDLH}$ | Propagation delay, low-to-high output | | | 1.000 | 1.400 | ns |
| $V_{TT}$ | Terminating voltage | — | | –2.0 | | V |

| PARAMETER | | TEST CONDITIONS | TEMPERATURE $T_A$ = 0° MIN. | MAX. | $T_A$ = 25° MIN. | MAX. | $T_A$ = 70° MIN. | MAX. | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **OUTPUT BUFFERS—50 Driver** | | | | | | | | | **(O01, O02)** |
| $V_{OH}$ | Output high voltage | $V_{EE}$ = –3.3V ± 5% | –1.02 | –0.84 | –0.98 | –0.81 | –0.92 | –0.74 | V |
| $V_{OL}$ | Output low voltage | $V_{EE}$ = –3.3V ± 5% | –1.95 | –1.63 | –1.95 | –1.63 | –1.95 | –1.63 | V |

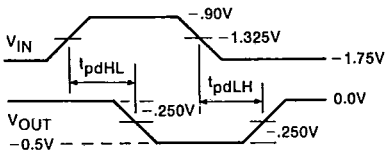
# ECL GATE ARRAY

# HE2000

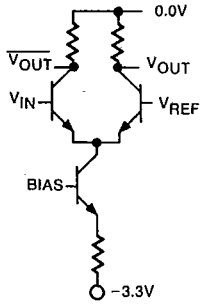
TEST SETUP:




WAVEFORMS:

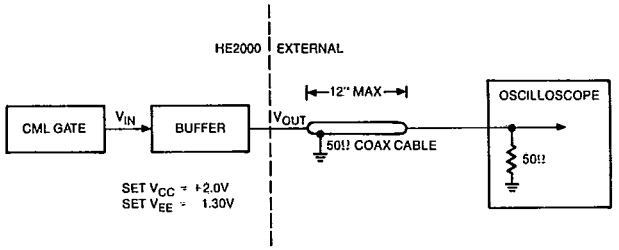



EQUIVALENT CIRCUIT OF CML UNIT LOAD:

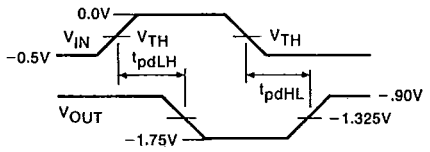



A. INPUT BUFFER

TEST SETUP:




WAVEFORMS:




SPECIFIED DELAY DOES NOT INCLUDE DELAY DUE TO COAX CABLE.

B. OUTPUT BUFFER—50 OHM DRIVER

## TESTING ECL COMPATIBLE OUTPUTS

To obtain results correlating with Honeywell specifications, specific testing techniques must be used.

All power leads and signal leads must be kept as short as possible. Equal length coaxial cables must be used between the test set and the scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended. Interconnect fittings should be 50-ohm GR, BNC, Selectro Conhex, or equivalent. Wire length should be less than ¼ inch from TPin to input and TPout to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times. In addition, the positive supply ($V_{CC}$) should be decoupled from the test board by an RF type 25 $\mu$F capacitor to -3.3V. $V_{CC}$ should be set to +2.0V and $V_{EE}$ set to -1.3V. With this setup, the termination resistors may be connected to GND.

*Figure 4. Test Configurations*

## UNDERSTANDING CURRENT MODE LOGIC

From the earliest days of bipolar technology, circuit designers noted that current switches are faster than their voltage counterparts. A logic family based on steering currents, without altering their values, is intrinsically faster than one based on voltage-switching techniques. That is the reason ECL and CML circuits are generally faster than TTL.

Both ECL and CML use a differential pair of NPN transistors for switching current. Circuit diagrams of the basic gates look similar (Figure 5), but they differ in operation.

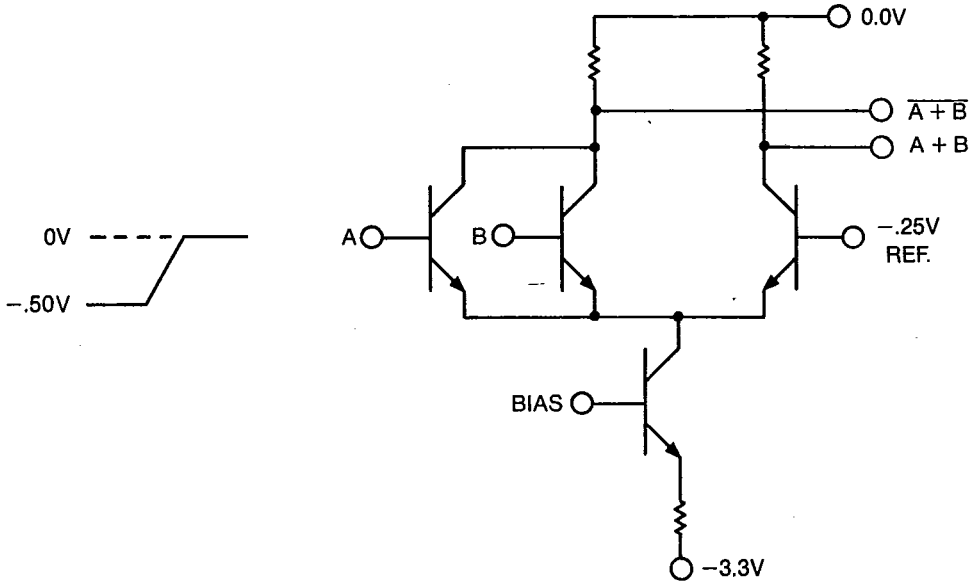
The reference voltages represent the center point of the logic swing. In ECL, with a –1.29 volt reference and a nominal collector voltage swing of .85 volt, the collector-base junction on the signal input side goes to 0 volts under worst case conditions. On the reference side, that junction always remains reverse-biased by .44 volt. Thus, the transistors never saturate. However, the emitter-follower is always on, increasing power consumption. The use of the emitter-follower output dictates the ECL operating levels. Rather than rising all the way to the positive power supply voltage, the ECL output high level stays a diode drop below.

In contrast, CML employs a reference voltage of .25 volt below the positive supply and a signal swing of .5 volt. The collector-base junction of the input transistor then becomes forward-biased by .5 volt at most, a condition termed soft saturation because negligible forward injection across the junction takes place. With almost no excess charge stored in the base in soft saturation, switching speed is comparable with that of ECL. At the same time, an off transistor cuts off completely. Because they are not used, the additional power of ECL emitter-follower drivers is eliminated.

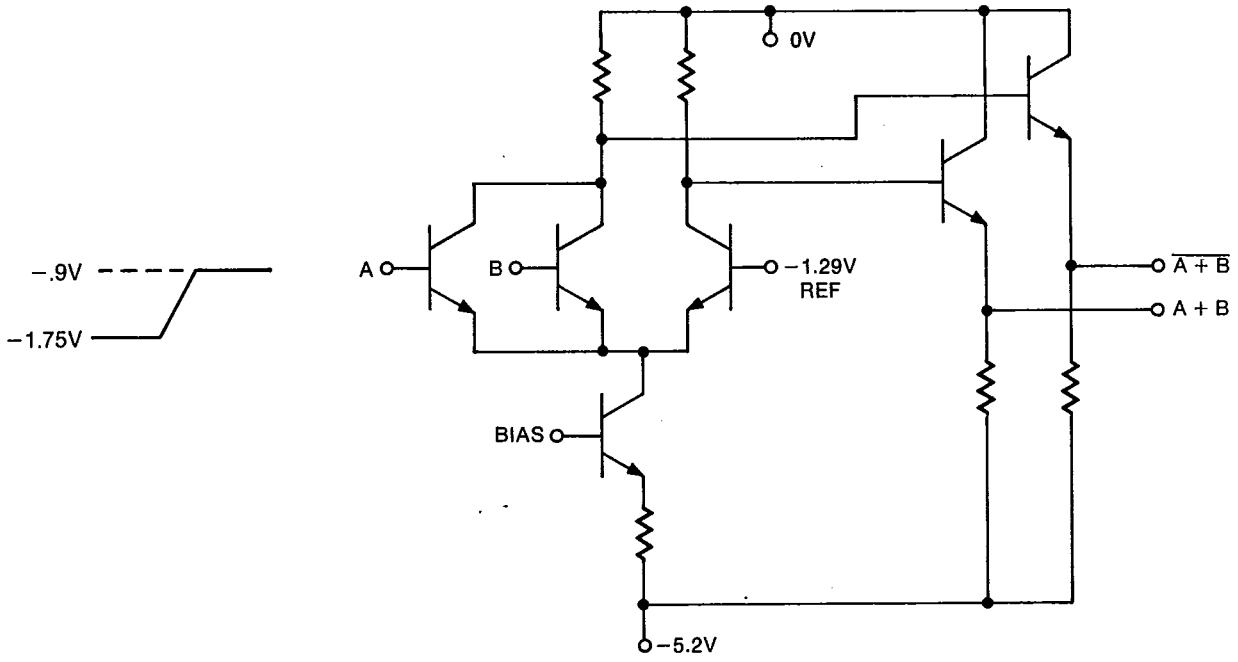
The single differential pair of a CML gate drives following gates directly from either collector. Both true and complement outputs are available with nearly equal speed. Gate delays are essentially a single transistor delay because most logic functions are implemented with a single differential pair as the primary switch. Series gating generates many useful logic functions with few logic-gate delays, as in the Master Slave D Flip Flop shown in Figure 6. The –3.3V supply is the minimum voltage that supports the series-gating logic structure, so CML power consumption is at an absolute minimum without sacrificing any speed.

In CML circuits intended for gate array or VLSI custom chip use, currents are set on chip by a voltage and temperature compensated reference regulator. Reliable operation over commercial and extended temperature ranges is achieved.

For further information, ask your Honeywell representative for the article reprints entitled, "Honeywell High Speed Digital Technology."




(A) BASIC CML OR/NOR LOGIC GATE




(B) BASIC ECL OR/NOR LOGIC GATE

*Figure 5. Basic Gates*

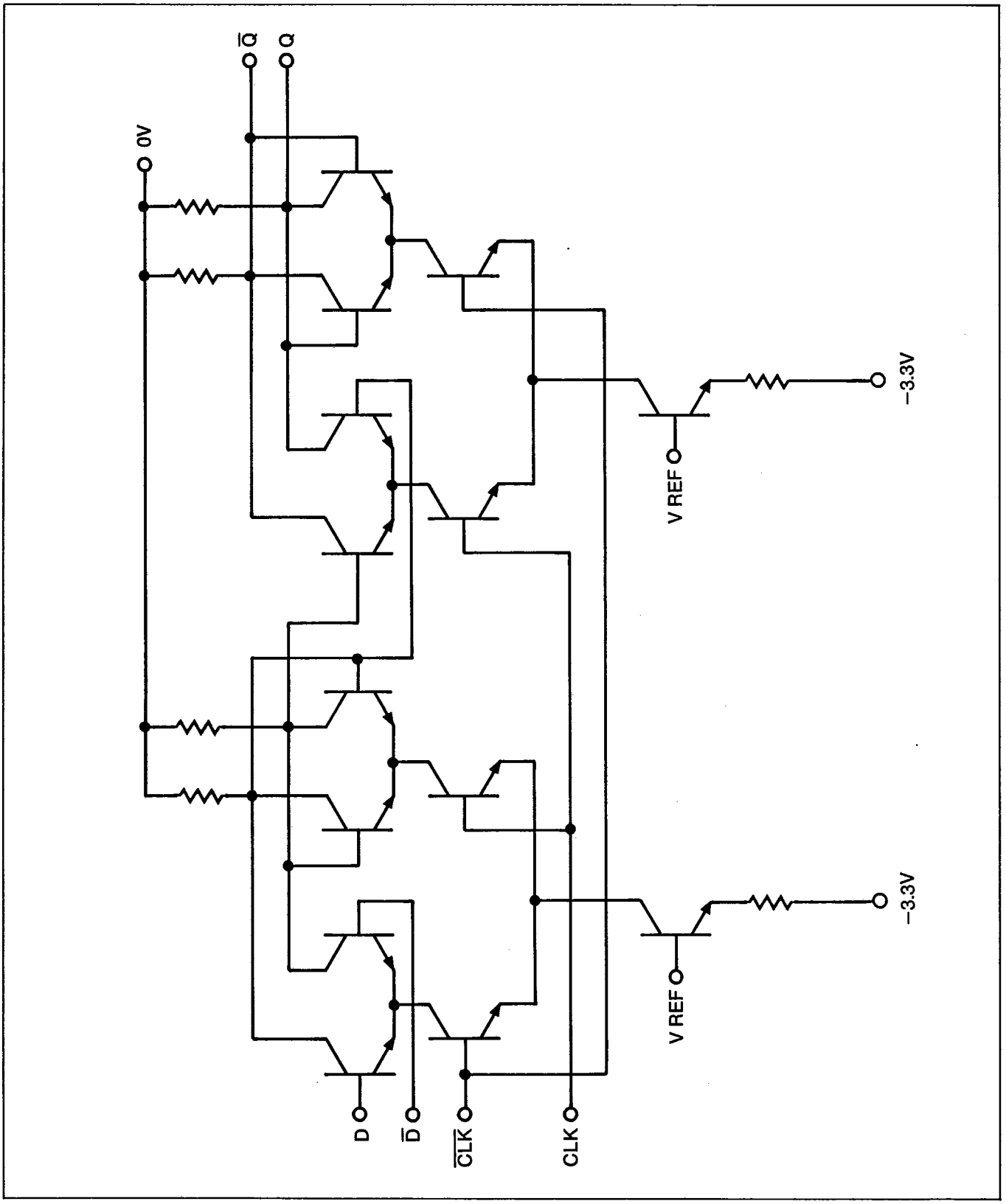



*Figure 6. CML Master Slave D Flip Flop*

# ECL GATE ARRAY HE2000

## PACKAGING

The HE2000 Gate Array is offered in a 173-pin-grid package. The PGAC package is pictured in Figure 7.

Figure 8 shows that separate power and signal metallization layers are provided to minimize lead resistance and inductance. The die is mounted cavity down to provide an elevated primary heat conducting surface ideally suited to forced air-cooling. The central die cavity is square to provide matched lead lengths and voltage drops. Hermeticity is provided with a solder-sealed lid.

The package has 140 I/O pins, 32 $V_{CC}$ and $V_{EE}$ pins, and one orientation pin. All pins are positioned in a uniform rectangular grid on 100 mil centers. The HE2000 is die attached to the ceramic substrate using a preform to provide a low thermal resistance path.

## HEAT SINKING

The HE2000 Gate Array was designed to be used in forced-air cooled systems. Maximum junction temperatures of 110 degrees C are allowed. Junction to case thermal resistance is typically less than 1 degree C/watt, while the junction to ambient thermal resistance is a function of heat sink mounting technique, air flow, and surrounding electronics. See Figure 9.

HE2000 Application Note #2 entitled "Packaging and Thermal Considerations", describes how to calculate thermal resistance and which heat sinks are appropriate.

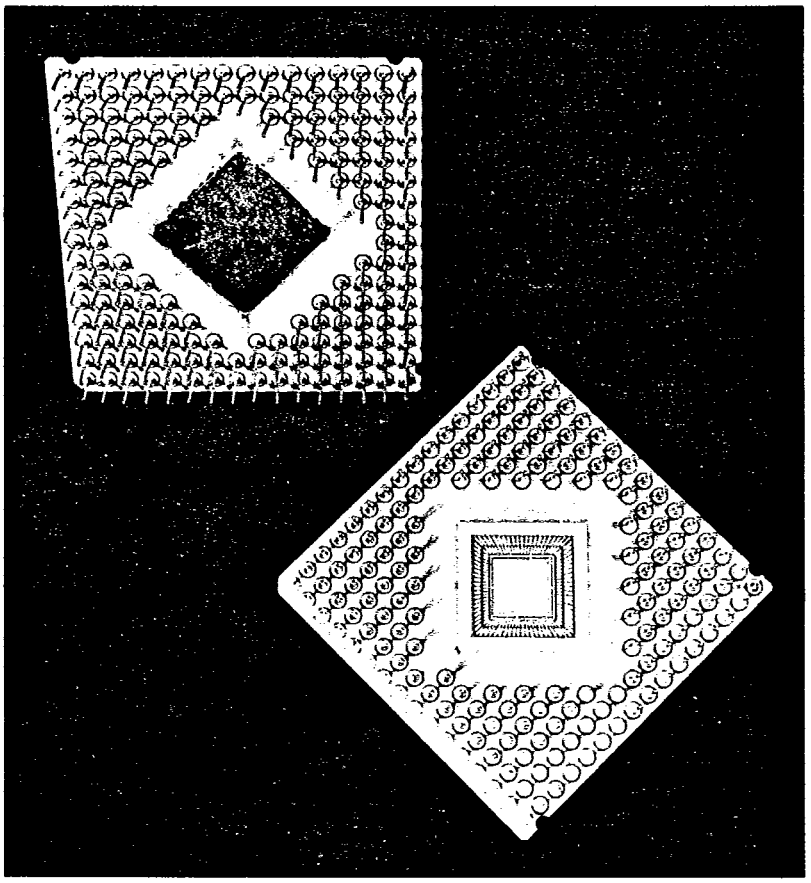


*Figure 7. HE2000 PGAC Package*

# ECL GATE ARRAY

# HE2000

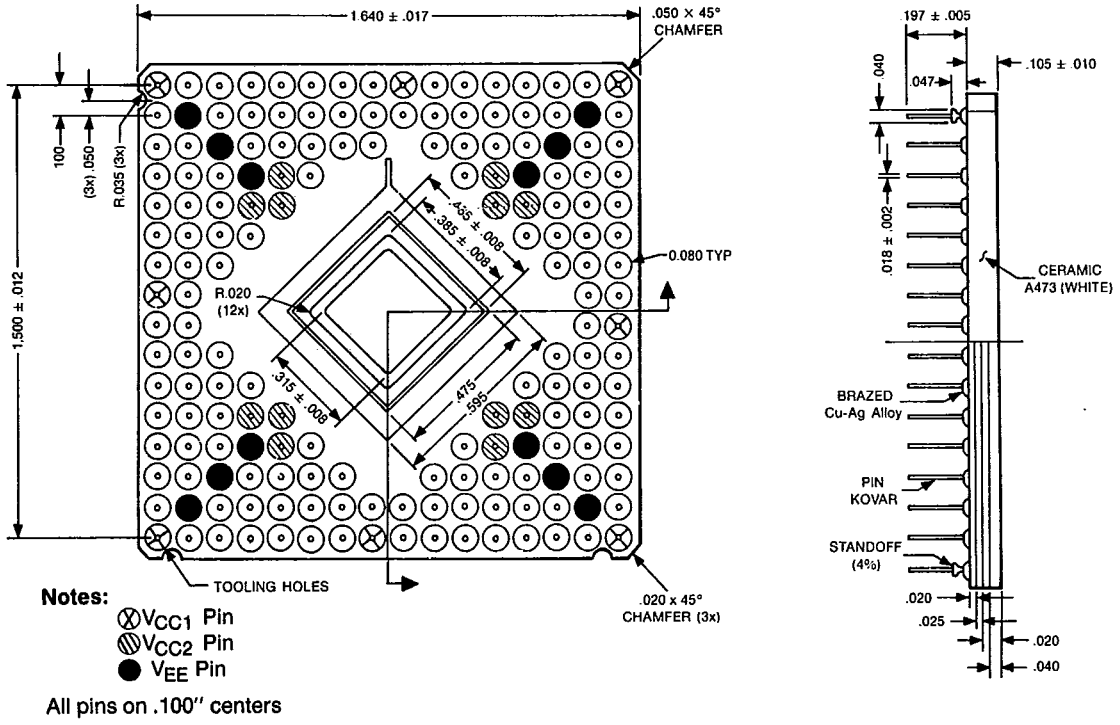



*Figure 8. PGAC Package Dimensions*

Order Code: GD

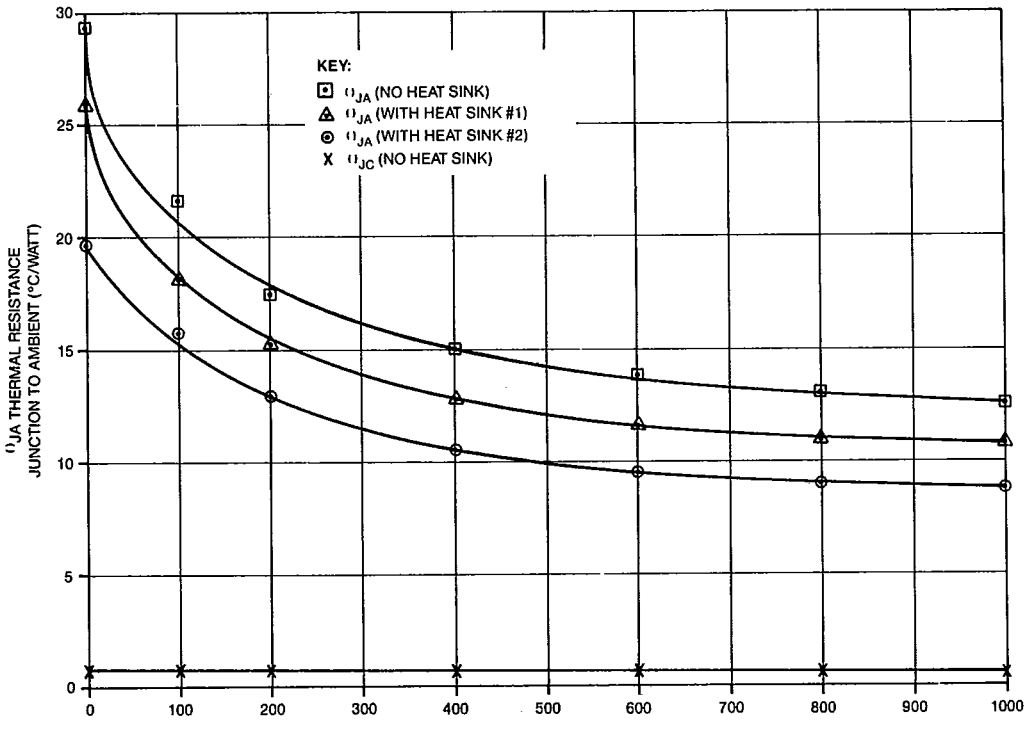



*Figure 9. Thermal Characteristics of PGAC Package*



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