QUADRUPLE BILATERAL SWITCHES

The HEF4016B has four independent analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition). Current through a switch will not cause additional V_{DD} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{DD} \geqslant (V_Y, V_Z) \geqslant V_{SS}$. Inputs Y and Z are electrically equivalent terminals.

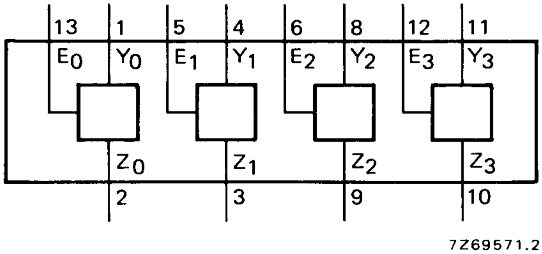


Fig. 1 Functional diagram.

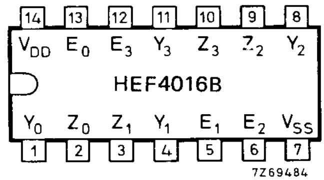


Fig. 2 Pinning diagram.

HEF4016BP : 14-lead DIL; plastic (SOT-27).
HEF4016BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4016BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

PINNING

E_0 to E_3 enable inputs
Y_0 to Y_3 input/output terminals
Z_0 to Z_3 input/output terminals

APPLICATION INFORMATION

Some examples of applications for the HEF4016B are:

- Signal gating
- Modulation
- Demodulation
- Chopper

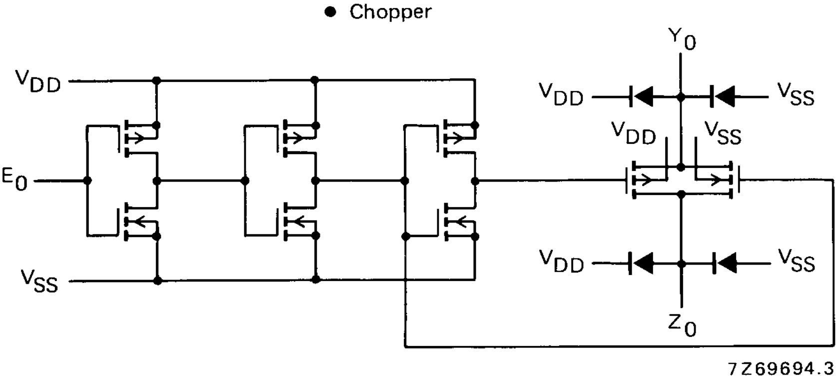


Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch   P   max.   100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C; V_{SS} = 0 V (unless otherwise specified)

parameter	V_{DD} V	symbol	typ.	max.	unit	conditions
ON resistance	5	R_{ON}	8000	–	Ω	E_n at V_{IH}
	10		230	690	Ω	V_{is} = 0 to V_{DD}
	15		115	350	Ω	see Fig. 4
ON resistance	5	R_{ON}	140	425	Ω	E_n at V_{IH}
	10		65	195	Ω	V_{is} = V_{SS}
	15		50	145	Ω	see Fig. 4
ON resistance	5	R_{ON}	170	515	Ω	E_n at V_{IH}
	10		95	285	Ω	V_{is} = V_{DD}
	15		75	220	Ω	see Fig. 4
'Δ' ON resistance between any two channels	5	ΔR_{ON}	200	–	Ω	E_n at V_{IH}
	10		15	–	Ω	V_{is} = 0 to V_{DD}
	15		10	–	Ω	see Fig. 4

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	unit	condition
Quiescent device current	5	I_{DD}	–	1,0	–	1,0	–	7,5	μA	V_{SS} = 0; all valid input combinations; V_I = V_{SS} or V_{DD}
	10		–	2,0	–	2,0	–	15,0	μA	
	15		–	4,0	–	4,0	–	30,0	μA	
Input leakage current at E_n	15	$\pm I_{IN}$	–	–	–	300	–	1000	nA	E_n at V_{SS} or V_{DD}
OFF-state leakage current, any channel OFF	5	I_{OZ}	–	–	–	–	–	–	nA	E_n at V_{IL}; V_{is} = V_{SS} or V_{DD}; V_{os} = V_{DD} or V_{SS}
	10		–	–	–	–	–	–	nA	
	15		–	–	–	200	–	–	nA	
E_n input voltage LOW	5	V_{IL}	–	1,5	–	1,5	–	1,5	V	switch OFF; see Fig. 9 for I_{OZ}
	10		–	3,0	–	3,0	–	3,0	V	
	15		–	4,0	–	4,0	–	4,0	V	
E_n input voltage HIGH	5	V_{IH}	3,5	–	3,5	–	3,5	–	V	low-impedance between Y and Z (ON condition) see R_{ON} switch
	10		7,0	–	7,0	–	7,0	–	V	
	15		11,0	–	11,0	–	11,0	–	V	

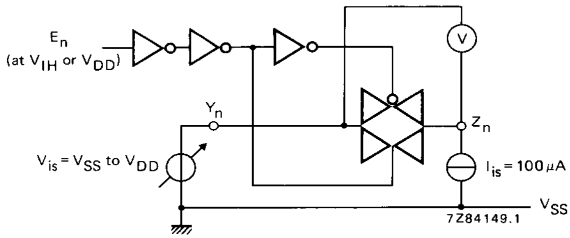


Fig. 4 Test set-up for measuring R_{ON}.

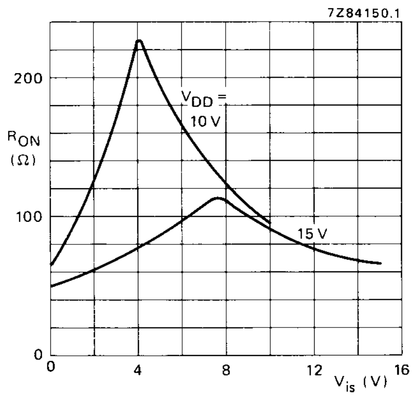


Fig. 5 Typical R_{ON} as a function of input voltage.

$E_n > V_{IH}$
$I_{is} = 100\ \mu A$
$V_{SS} = 0\ V$

A.C. CHARACTERISTICS V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		25	50	ns	
HIGH to LOW	10	t_{PHL}	10	20	ns	note 1
	15		5	10	ns	
	5		20	40	ns	
LOW to HIGH	10	t_{PLH}	10	20	ns	note 1
	15		5	10	ns	
Output disable times						
$E_n \rightarrow V_{os}$	5		90	130	ns	
HIGH	10	t_{PHZ}	80	110	ns	note 2
	15		75	100	ns	
	5		85	120	ns	
LOW	10	t_{PLZ}	75	100	ns	note 2
	15		75	100	ns	
Output enable times						
$E_n \rightarrow V_{os}$	5		40	80	ns	
HIGH	10	t_{PZH}	20	40	ns	note 2
	15		15	30	ns	
	5		40	80	ns	
LOW	10	t_{PZL}	20	40	ns	note 2
	15		15	30	ns	
Distortion, sine-wave	5		–		%	
response	10		0,08		%	note 3
	15		0,04		%	
Crosstalk between	5		–		MHz	
any two channels	10		1		MHz	note 4
	15		–		MHz	
Crosstalk; enable	5		–		mV	
input to output	10		50		mV	note 5
	15		–		mV	
OFF-state	5		–		MHz	
feed-through	10		1		MHz	note 6
	15		–		MHz	
ON-state frequency	5		–		MHz	
response	10		90		MHz	note 7
	15		–		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)*	5	$550\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz)
	10	$2\,600\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs
	15	$6\,500\,f_i + \Sigma(f_oC_L) \times V_{DD}^2$	V_{DD} = supply voltage (V)

* All enable inputs switching.

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n = V_{DD}; V_{is} = V_{DD} (square-wave); see Figs 6 and 10.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Figs 6 and 11.
3. R_L = 10 kΩ; C_L = 15 pF; E_n = V_{DD}; V_{is} = ½$V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½V_{DD});
   f_{is} = 1 kHz; see Fig. 7.
4. R_L = 1 kΩ; V_{is} = ½$V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½V_{DD});
   $20 \log \frac{V_{os}\ (B)}{V_{is}\ (A)} = -50$ dB; E_n (A) = V_{SS}; E_n (B) = V_{DD}; see Fig. 8.
5. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value);
   see Fig. 6.
6. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{SS}; V_{is} = ½$V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 7.
7. R_L = 1 kΩ; C_L = 5 pF; E_n = V_{DD}; V_{is} = ½$V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 7.

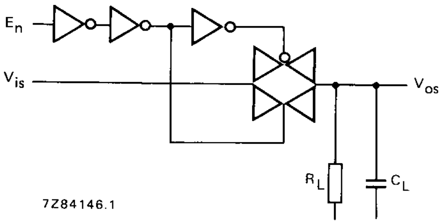


Fig. 6.

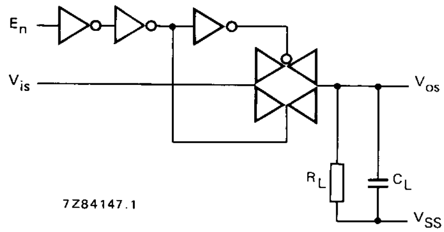
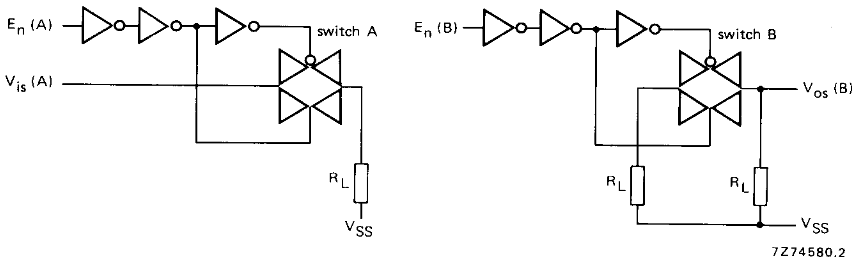


Fig. 7.



(a)

(b)

Fig. 8.

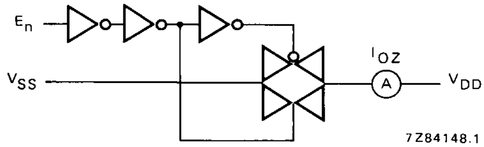


Fig. 9.

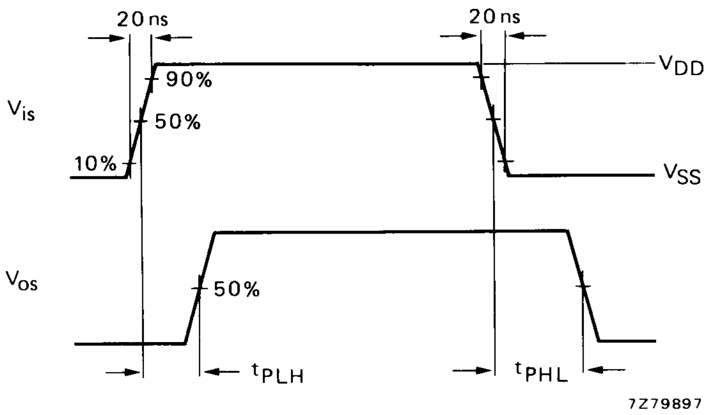
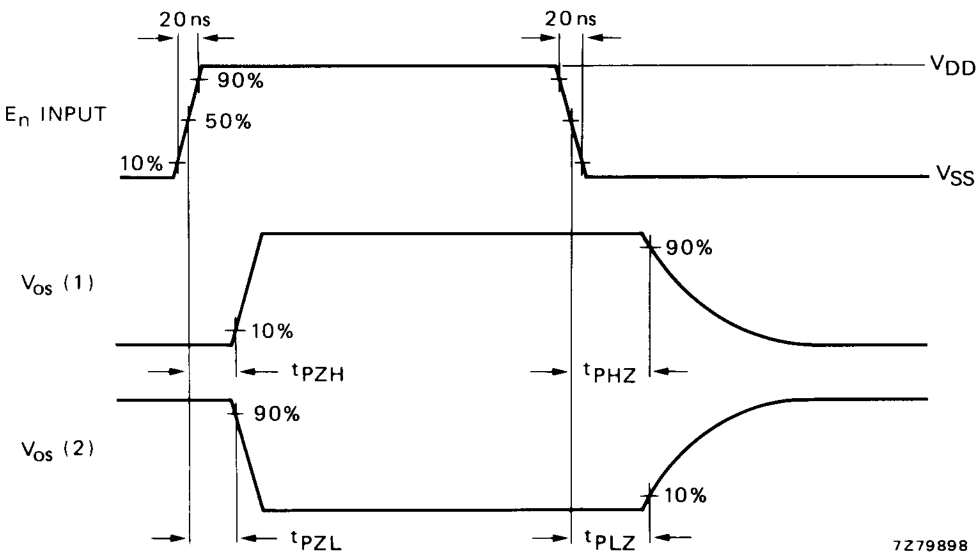


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os}.



(1) V_{is} at V_{DD}; (2) V_{is} at V_{SS}.

Fig. 11 Waveforms showing output disable and enable times.