4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

The HEF4022B is a 4-stage divide-by-8 Johnson counter with eight spike-free decoded active HIGH outputs (O_0 to O_7), an active LOW output from the most significant flip-flop ($\overline{O}_{4-7}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table). Either CP_0 or $\overline{CP}_1$ may be used as clock input to the counter and the other clock input may be used as a clock enable input. When cascading counters, the $\overline{O}_{4-7}$ output, which is LOW while the counter is in states, 4, 5, 6 and 7, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{4-7}$ = HIGH; O_1 to O_7 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit, following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

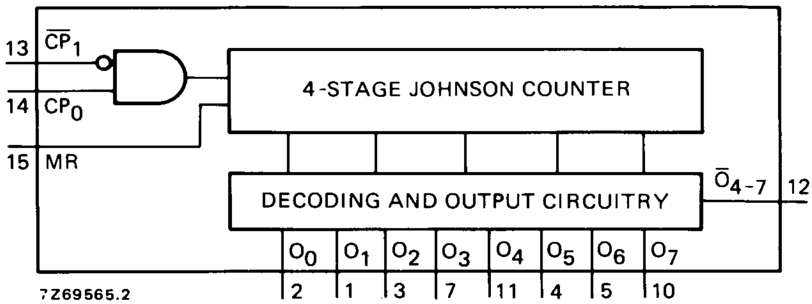

Fig. 1 Functional diagram.

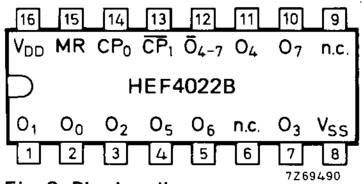

Fig. 2 Pinning diagram.

HEF4022BP : 16-lead DIL; plastic (SOT-38Z).
HEF4022BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4022BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_0	clock input (LOW to HIGH; edge-triggered)
$\overline{CP}_1$	clock input (HIGH to LOW; edge-triggered)
MR	master reset input
O_0 to O_7	decoded outputs
$\overline{O}_{4-7}$	carry output (active LOW)

FAMILY DATA
I_{DD} LIMITS category MSI
} see Family Specifications

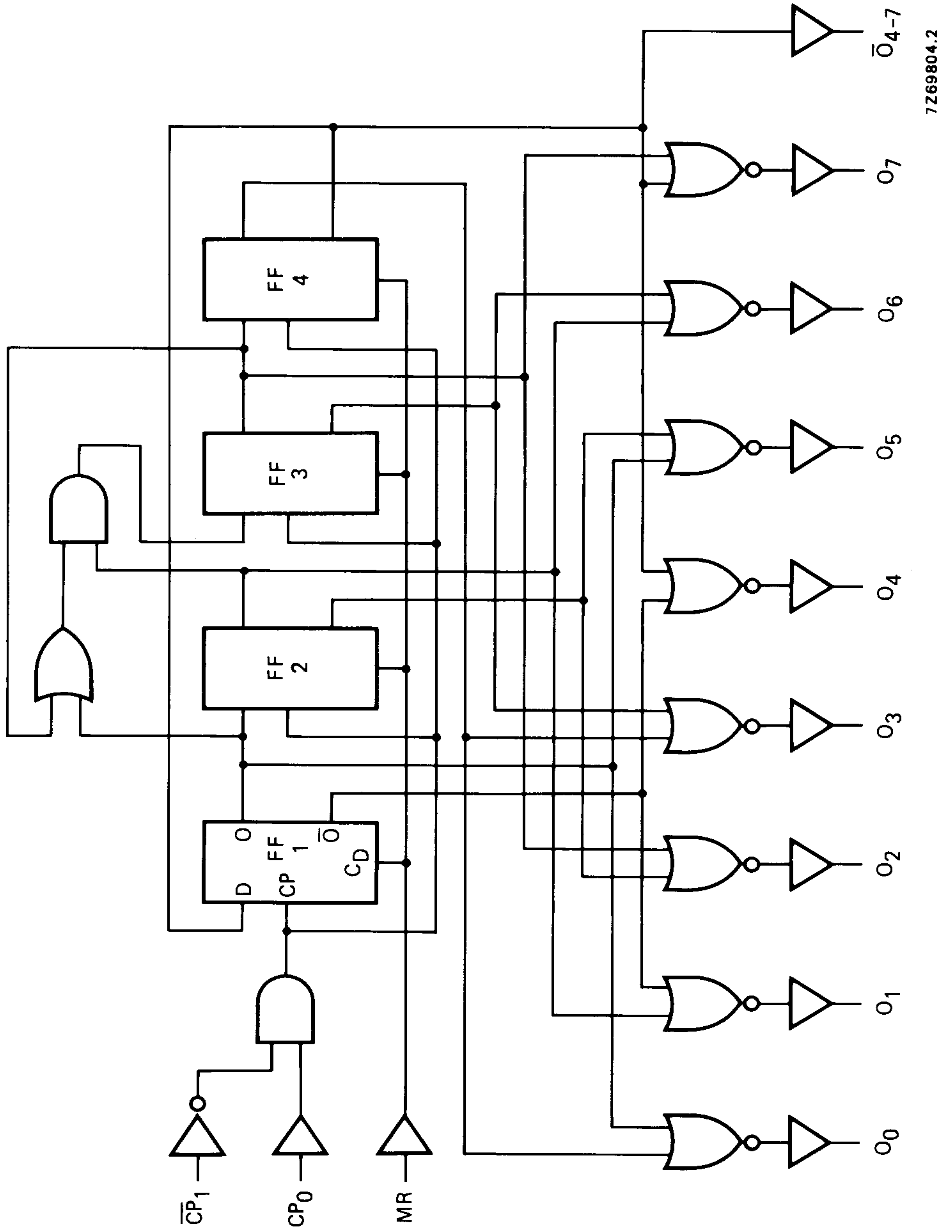

Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	operation
H	X	X	$O_0 = \overline{O}_{4\text{-}7}$ = H; O_1 to O_7 = L
L	H	╲	Counter advances
L	╱	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	╱	No change
L	╲	L	No change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
╱ = positive-going transition
╲ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			195	390	ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	145	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			245	485	ns	218 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	195	ns	84 ns + (0,23 ns/pF) C_L
	15			60	125	ns	52 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1$ → $\overline{O}_{4\text{-}7}$	5			245	485	ns	218 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	185	ns	79 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	145	ns	64 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
MR → O_1 to O_7	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
MR → O_0	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
MR → $\overline{O}_{4\text{-}7}$	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		
Hold times $CP_0 \rightarrow \overline{CP}_1$	5		140	70		ns	see also waveforms Figs 4 and 5
	10	t_{hold}	50	25		ns	
	15		30	15		ns	
$\overline{CP}_1 \rightarrow CP_0$	5		170	85		ns	
	10	t_{hold}	60	30		ns	
	15		40	20		ns	
Minimum clock pulse width	5		75	35		ns	
	10	t_{WCP}	30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5		70	35		ns	
	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time for MR	5		30	10		ns	
	10	t_{RMR}	15	5		ns	
	15		10	5		ns	
Maximum clock pulse frequency	5		3	6		MHz	
	10	f_{max}	8	16		MHz	
	15		12	24		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$2400\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz); C_L = load capacitance (pF)
	15	$6700\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	$\Sigma(f_oC_L)$ = sum of outputs; V_{DD} = supply voltage (V)

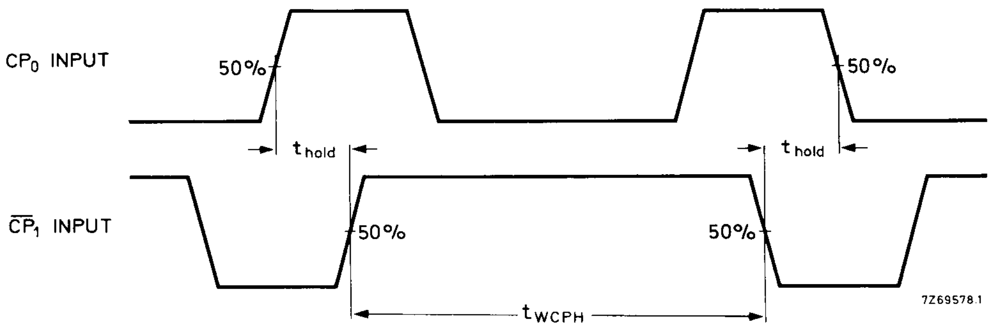

Fig. 4 Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.
Hold times are shown as positive values, but may be specified as negative values.

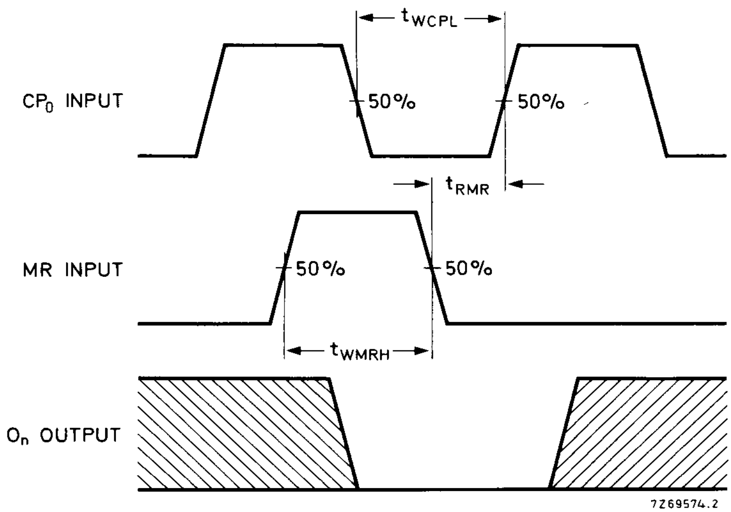

Fig. 5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

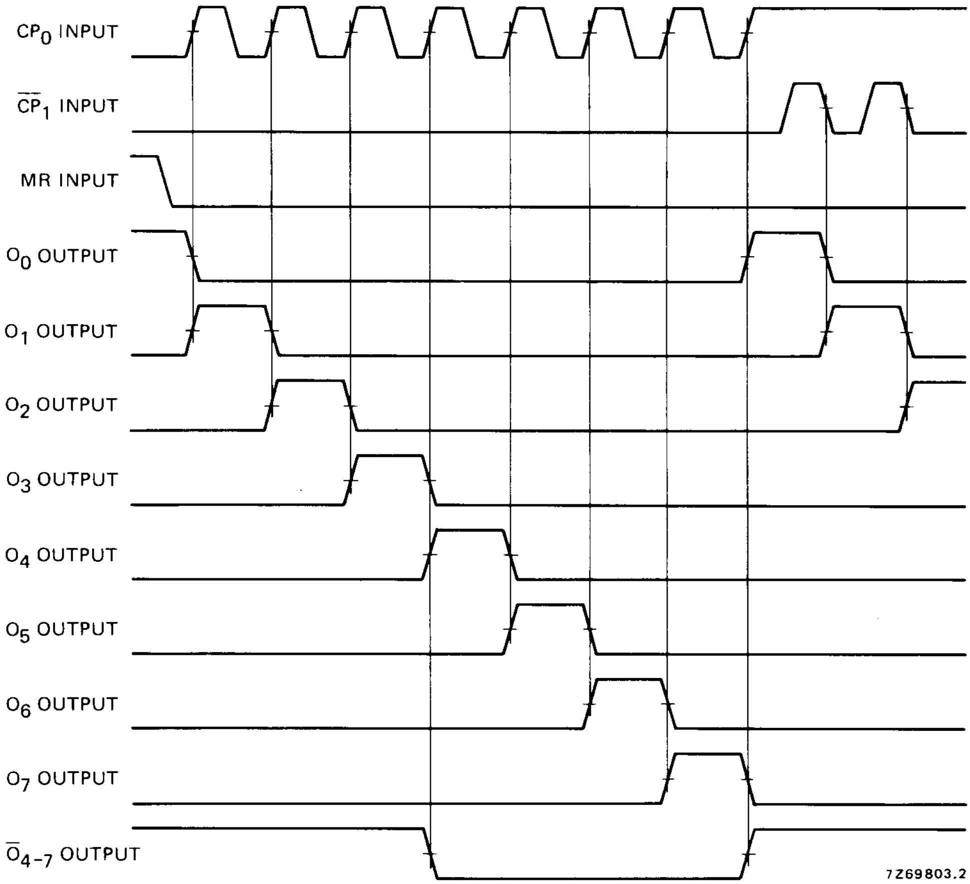

Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some of the features of the HEF4022B are:

- High speed
- Spike-free decoded outputs
- Carry output for cascading

Figure 7 shows a technique for extending the number of decoded output states for the HEF4022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

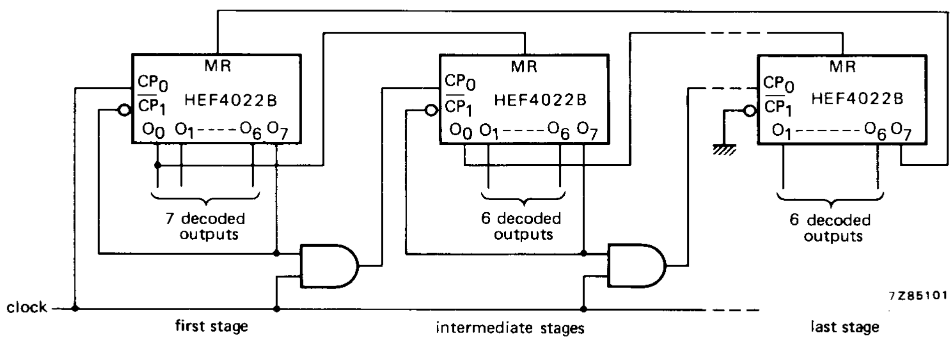

Fig. 7 Counter expansion.