DUAL JK FLIP-FLOP

The HEF4027B is a dual JK flip-flop which is edge-triggered and features indepedent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs (O,$\overline{O}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

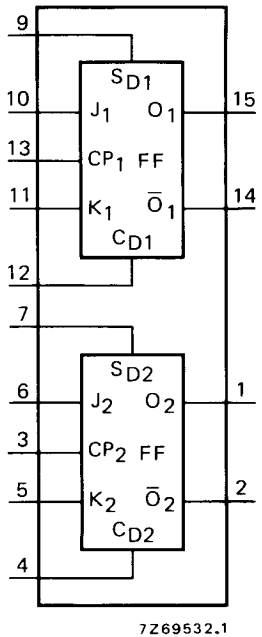

Fig. 1 Functional diagram.

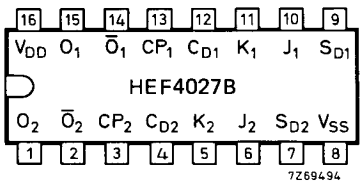

Fig. 2 Pinning diagram.

FUNCTION TABLES

inputs					outputs	
S_D	C_D	CP	J	K	O	$\overline{O}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

inputs					outputs	
S_D	C_D	CP	J	K	O_{n+1}	$\overline{O}_{n+1}$
L	L	∫	L	L	no change	
L	L	∫	H	L	H	L
L	L	∫	L	H	L	H
L	L	∫	H	H	$\overline{O}_n$	O_n

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transition

PINNING

J,K synchronous inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\overline{O}$ complement output

HEF4027BP : 16-lead DIL; plastic (SOT-38Z).
HEF4027BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4027BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category FLIP-FLOPS

} see Family Specifications

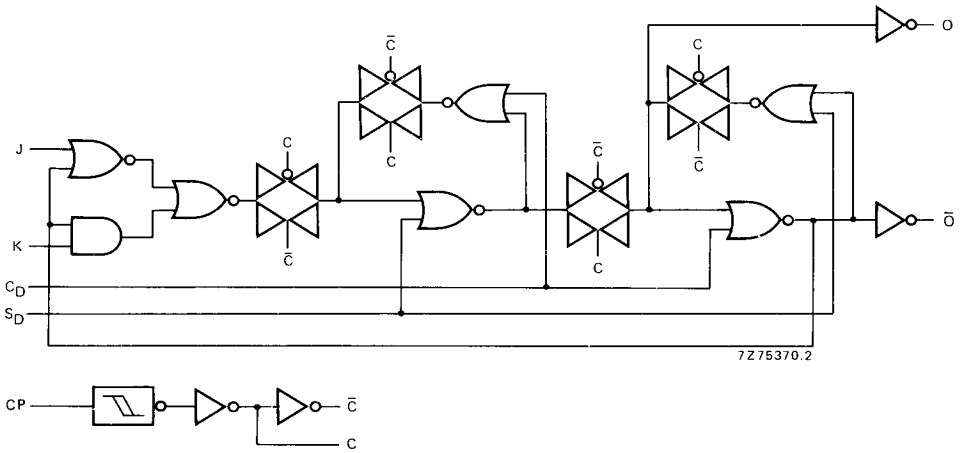

Fig. 3 Logic diagram (one flip-flop).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O, $\overline{O}$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	27 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
S_D → O	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
C_D → O	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	33 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
S_D → $\overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
C_D → $\overline{O}$	5			75	150	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time	5		50	25		ns	
J, K → CP	10	t_{su}	30	10		ns	
	15		20	5		ns	
Hold time	5		25	0		ns	
J, K → CP	10	t_{hold}	20	0		ns	
	15		15	5		ns	
Minimum clock pulse width; LOW	5		80	40		ns	see also waveforms Figs 4 and 5
	10	t_{WCPL}	30	15		ns	
	15		24	12		ns	
Minimum S_D, C_D pulse width; HIGH	5		90	45		ns	
	10	t_{WSDH}, t_{WCDH}	40	20		ns	
	15		30	15		ns	
Recovery time for S_D, C_D	5		20	−15		ns	
	10	t_{RSD}, t_{RCD}	15	−10		ns	
	15		10	−5		ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Maximum clock pulse frequency J = K = HIGH	5	f_{max}	4	8	MHz	see also waveforms Fig. 4
	10		12	25	MHz	
	15		15	30	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

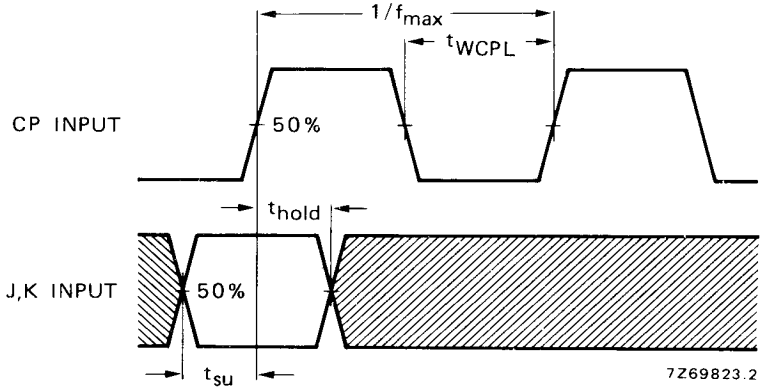

Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width.
Set-up and hold times are shown as positive values but may be specified as negative values.

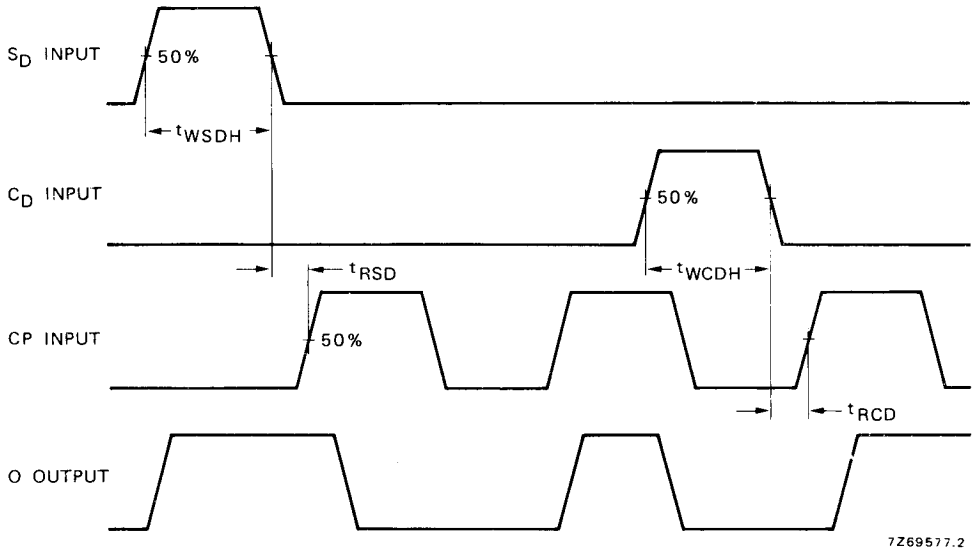

Fig. 5 Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4027B are:

- Registers
- Counters
- Control circuits