1-OF-10 DECODER

The HEF4028B is a 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 to A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the device may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0, A_1 and A_2 selecting an output O_0 to O_7. Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The HEF4028B may also be used as an 8-output (O_0 to O_7) demultiplexer with A_0 to A_2 as address inputs and A_3 as an active LOW data input. The outputs are fully buffered for best performance.

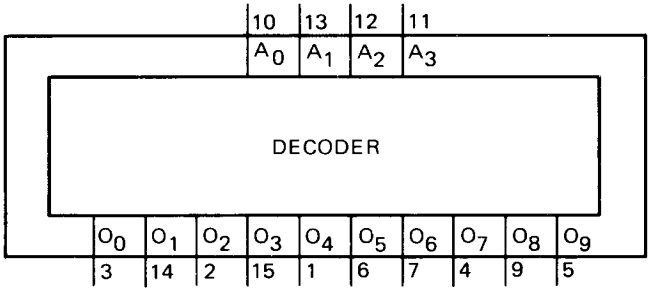

Fig.1 Functional diagram.

Fig.2 Pinning diagram

HEF4028BP : 16-lead DIL; plastic (SOT-38Z).
HEF4028BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4028BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

A_0 to A_3 address inputs, 1-2-4-8 BCD
O_0 to O_9 outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

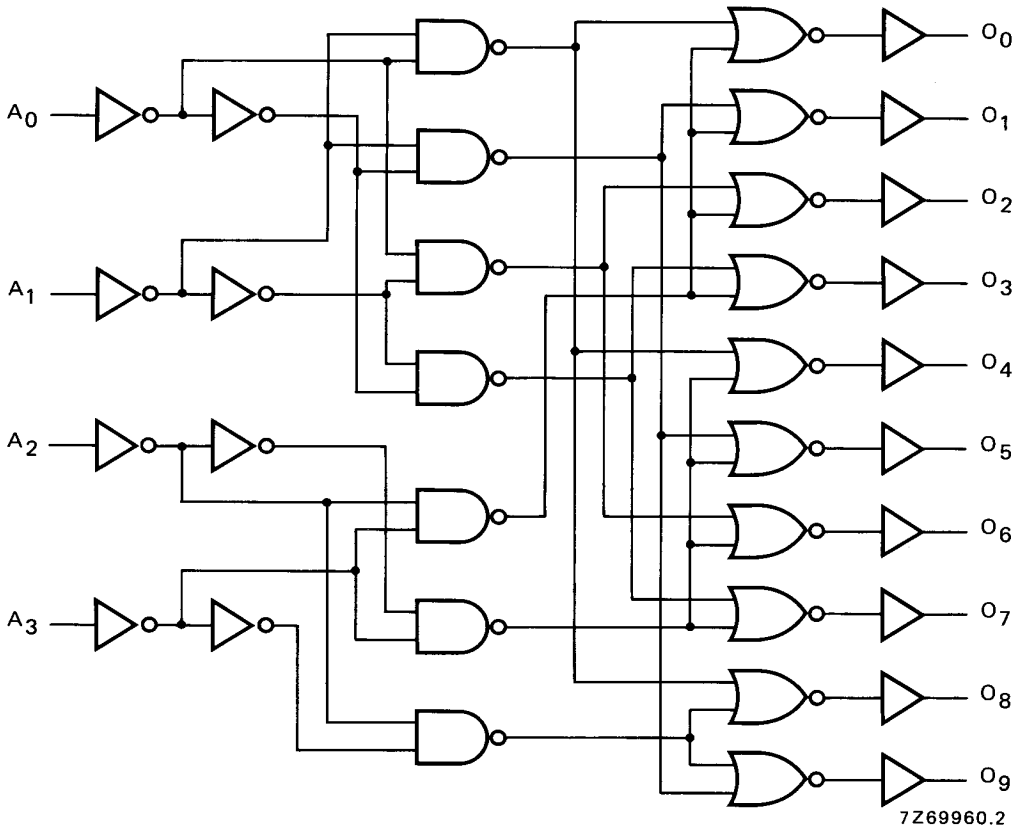

Fig. 3 Logic diagram.

TRUTH TABLE

inputs				outputs										
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	
L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	H	H	H	L	L	L	L	L	L	L	H	L	L	
H	L	L	L	L	L	L	L	L	L	L	L	H	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	H	
H	L	H	L	L	L	L	L	L	L	L	L	L	L	*
H	L	H	H	L	L	L	L	L	L	L	L	L	L	
H	H	L	L	L	L	L	L	L	L	L	L	L	L	
H	H	L	H	L	L	L	L	L	L	L	L	L	L	
H	H	H	L	L	L	L	L	L	L	L	L	L	L	
H	H	H	H	L	L	L	L	L	L	L	L	L	L	

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

* Extraordinary states.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$A_n \longrightarrow O_n$	5		100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$350\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7\,350\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	