OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The HEF40374B is an octal D-type flip-flop with 3-state buffered outputs with a common clock input (CP). The device is used primarily as an 8-bit positive edge-triggered storage register for interfacing with a 3-state bus. Data on the D-inputs is transferred to storage during the LOW-to-HIGH transition of the clock (CP) input. The 3-state output buffers are controlled by an active LOW output enable input ($\overline{EO}$). A HIGH on $\overline{EO}$ forces the eight outputs to a high impedance OFF-state. When $\overline{EO}$ is LOW, the data in the register appears at the outputs.

The output stages have high current output capability suitable for driving highly capacitive loads.
The device features hysteresis on the CP input to improve noise rejection.
Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40373B is pin and functionally compatible with the TTL '374' device.
Supply voltage range: 3 to 15 V.

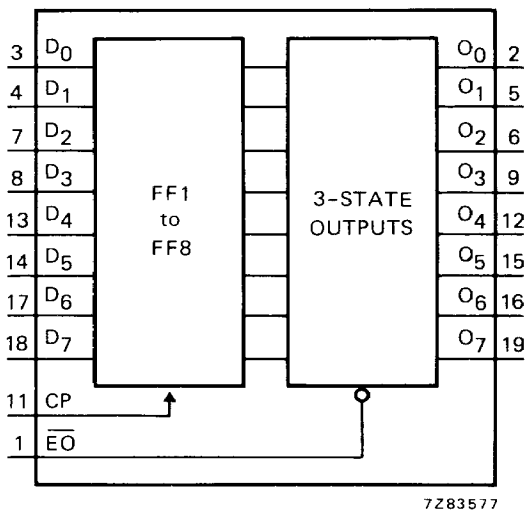

Fig. 1 Functional diagram.

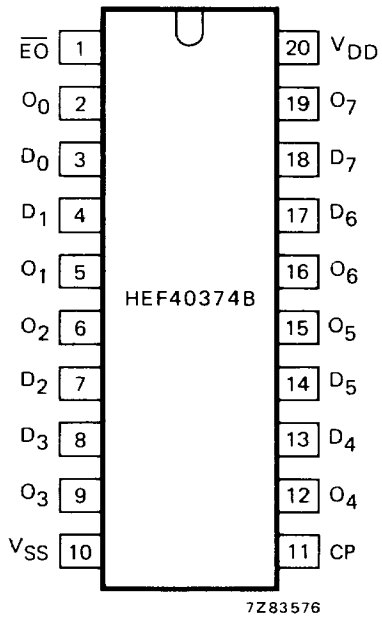

Fig. 2 Pinning diagram.

PINNING

D_0 to D_7	data inputs
CP	clock input
$\overline{EO}$	output enable input (active LOW)
O_0 to O_7	3-state buffered outputs

HEF40374BP : 20-lead DIL; plastic (SOT146).
HEF40374BD; 20-lead DIL; ceramic (cerdip) (SOT152C).
HEF40374BT : 20-lead mini-pack; plastic (SO-20; SOT163A).

FAMILY DATA | see Family Specifications

I_{DD} LIMITS category MSI

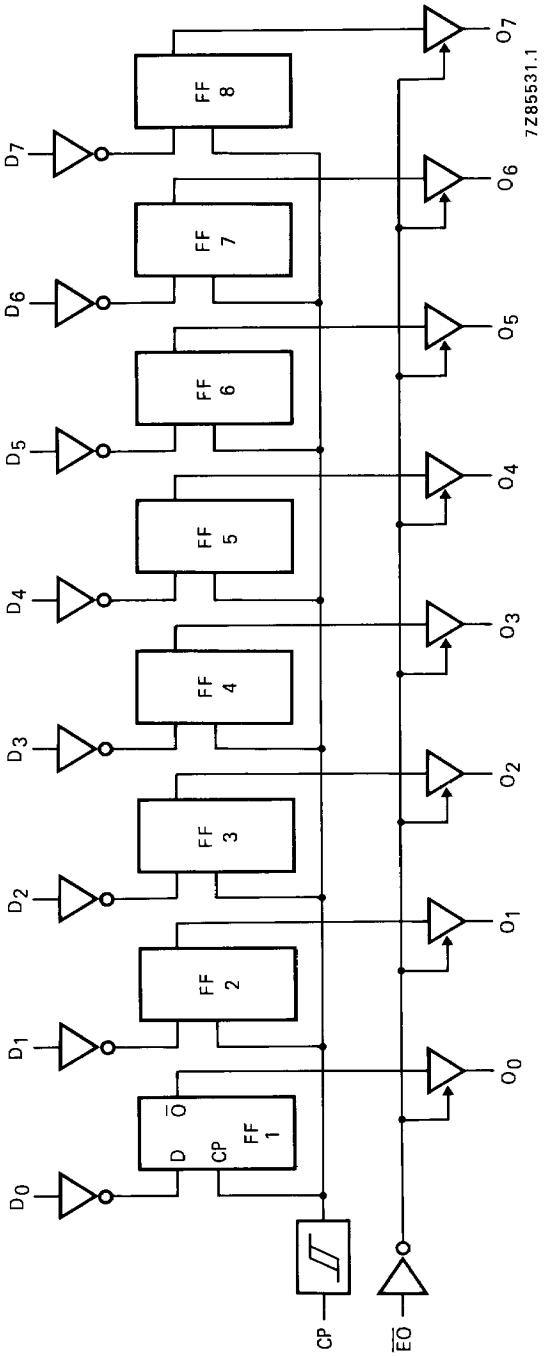

Fig. 3 Logic diagram.

FUNCTION TABLE

operating modes	inputs			internal register	outputs O_0 to O_7
	$\overline{EO}$	CP	D_n		
load & read register	L	∫	l	L	L
	L	∫	h	H	H
load register & disable outputs	H	∫	l	L	Z
	H	∫	h	H	Z

H = HIGH state (the more positive voltage)
h = HIGH state (one set-up time prior to the LOW-to-HIGH clock transition)
L = LOW state (the less positive voltage)
l = LOW state (one set-up time prior to the LOW-to-HIGH clock transition)
Z = high impedance OFF-state
∫ = LOW-to-HIGH clock transition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 typ.	+25 min.	+25 typ.	+85 min.	+85 typ.	
Output current HIGH	5	4,6			0,75		0,6	1,2	0,45		mA
	10	9,5		$-I_{OH}$	1,85		1,5	3,0	1,1		mA
	15	13,5			14,5		15	50	15,5		mA
Output current HIGH	5	3,6			9,3		10	24	10,7		mA
	10	8,4		$-I_{OH}$	14,4		15	46	15,0		mA
	15	13,2			19,5		20	62	19,8		mA
Output current LOW	5		0,4		2,9		2,3	5,4	1,75		mA
	10		0,5	I_{OL}	9,5		7,6	17	5,50		mA
	15		1,5		30,0		25	45	19,0		mA
Hysteresis voltage at clock input (CP)	5							220			mV
	10			V_H				250			mV
	15							320			mV

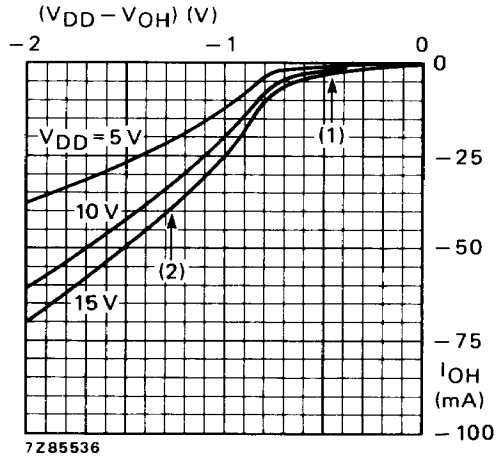

Fig. 4 Typical output source current characteristic.

(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

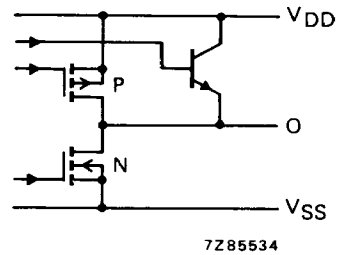

Fig. 5 Schematic diagram of output stage.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
CP → O_n	5			125	250	ns	113 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	54 ns + (0,01 ns/pF) C_L
	15			40	80	ns	36 ns + (0,07 ns/pF) C_L
CP → O_n	5			125	250	ns	122 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	53 ns + (0,03 ns/pF) C_L
	15			40	80	ns	39 ns + (0,02 ns/pF) C_L
Output transition times	5			40	80	ns	see Fig. 6
	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO}$ → O_n	5			60	120	ns	
HIGH	10	t_{PHZ}		30	60	ns	
	15			24	48	ns	
	5			70	140	ns	
LOW	10	t_{PLZ}		35	70	ns	
	15			30	60	ns	
Output enable times							
$\overline{EO}$ → O_n	5			65	130	ns	
HIGH	10	t_{PZH}		30	60	ns	
	15			24	48	ns	
	5			85	170	ns	
LOW	10	t_{PZL}		35	70	ns	
	15			25	50	ns	
Set-up time	5		20	0		ns	
D_n → CP	10	t_{su}	20	2		ns	
	15		20	5		ns	
Hold time	5		20	10		ns	
D_n → CP	10	t_{hold}	15	2		ns	
	15		10	0		ns	
Minimum clock pulse width; LOW	5		50	25		ns	
	10	t_{WCPL}	25	12		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5		25	5		MHz	
	10	f_{max}	6	12		MHz	
	15		8	17		MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3\,775\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$15\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$40\,575\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

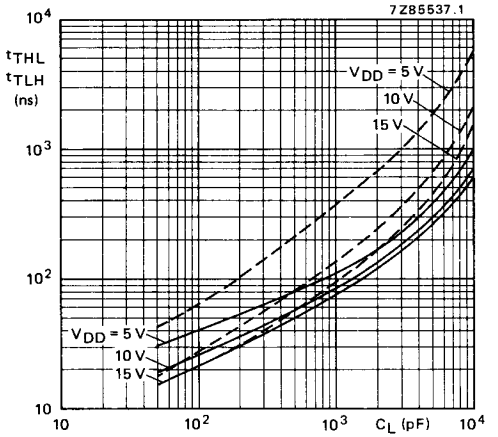

Fig. 6 Output transition times as a function of the load capacitance.
——— t_{TLH}; – – – – t_{THL}.