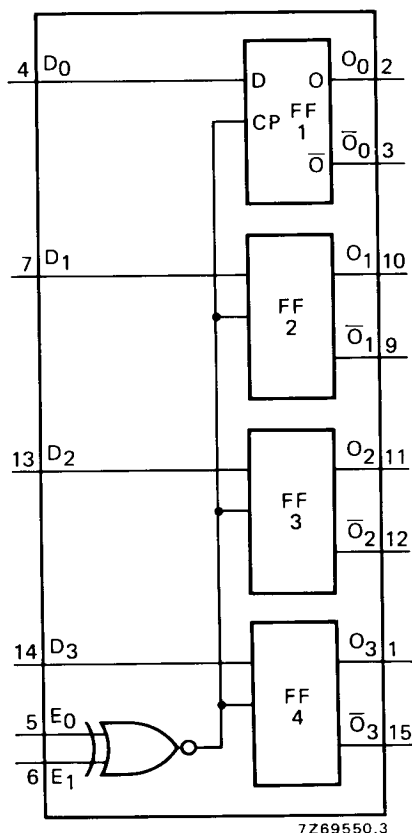


QUADRUPLE D-LATCH



The HEF4042B is a 4-bit latch with four data inputs (D_0 to D_3), four buffered latch outputs (O_0 to O_3), four buffered complementary latch outputs ($\bar{O}_0$ to $\bar{O}_3$) and two common enable inputs (E_0 and E_1). Information on D_0 to D_3 is transferred to O_0 to O_3 while both E_0 and E_1 are in the same state, either HIGH or LOW. O_0 to O_3 follow D_0 to D_3 as long as both E_0 and E_1 remain in the same state. When E_0 and E_1 are different, D_0 to D_3 do not affect O_0 to O_3 and the information in the latch is stored.

$\bar{O}_0$ to $\bar{O}_3$ are always the complement of O_0 to O_3 . The exclusive-OR input structure allows the choice of either polarity for E_0 and E_1 . With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.



FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

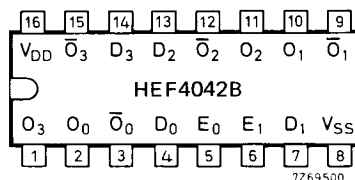


Fig. 2 Pinning diagram.

HEF4042BP : 16-lead DIL; plastic (SOT-38Z).

HEF4042BD : 16-lead DIL; ceramic (cerdip) (SOT-74).

HEF4042BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_0 to D_3 data inputs
 E_0 and E_1 enable inputs
 O_0 to O_3 parallel latch outputs
 $\bar{O}_0$ to $\bar{O}_3$ complementary parallel latch outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4042B are:

- Buffer storage
- Holding register

Fig. 1 Functional diagram.



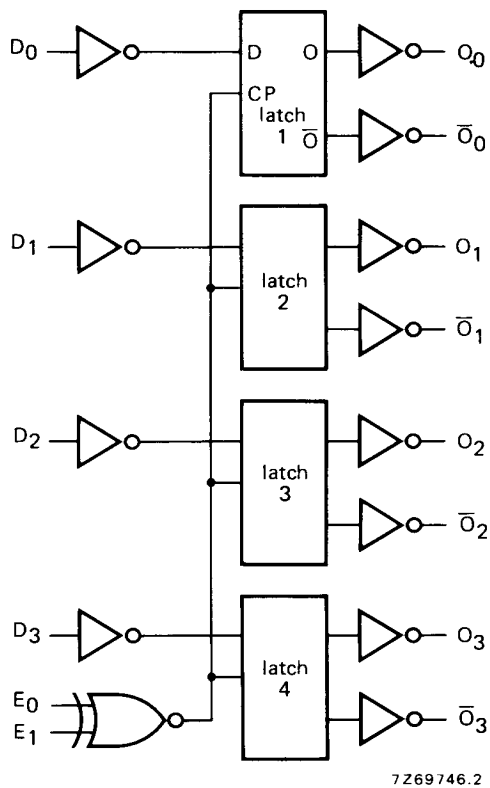


Fig. 3 Logic diagram.

FUNCTION TABLE

E_0	E_1	output O_n
L	L	D_n
L	H	latched
H	L	latched
H	H	D_n

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage).

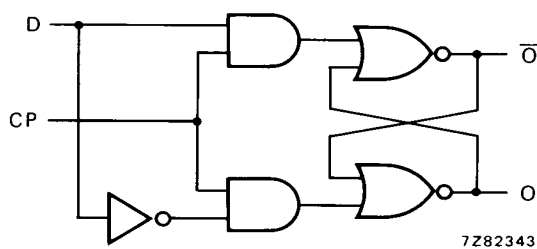


Fig. 4 Logic diagram (one latch).

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula		
Propagation delays								
D → O, $\bar{O}$	5	t _{PHL}		95	190	ns	67 ns + (0,55 ns/pF) C _L	
HIGH to LOW	10			40	80	ns	28 ns + (0,23 ns/pF) C _L	
	15			30	55	ns	22 ns + (0,16 ns/pF) C _L	
	5	t _{PLH}		85	175	ns	57 ns + (0,55 ns/pF) C _L	
LOW to HIGH	10			40	75	ns	28 ns + (0,23 ns/pF) C _L	
	15			30	60	ns	22 ns + (0,16 ns/pF) C _L	
E → O, $\bar{O}$	5	t _{PHL}		130	260	ns	102 ns + (0,55 ns/pF) C _L	
HIGH to LOW	10			50	105	ns	38 ns + (0,23 ns/pF) C _L	
	15			35	75	ns	27 ns + (0,16 ns/pF) C _L	
	5	t _{PLH}		120	245	ns	92 ns + (0,55 ns/pF) C _L	
LOW to HIGH	10			50	105	ns	38 ns + (0,23 ns/pF) C _L	
	15			35	75	ns	27 ns + (0,16 ns/pF) C _L	
Output transition times	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L	
HIGH to LOW	10			30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L	
	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L	
LOW to HIGH	10			30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L	
Set-up time	5	t _{su}	30	10		ns	see also waveforms Figs 5 and 6	
D → E	10			20	5			ns
	15			20	5			ns
Hold time	5	t _{hold}	15	−5		ns		
D → E	10			15	0			ns
	15			15	0			ns
Minimum enable pulse width	5	t _{WE}	90	45		ns		
	10			40	20			ns
	15			30	15			ns

	V_{DD} V	typical formula for P (W)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$3800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$15\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$41\,100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

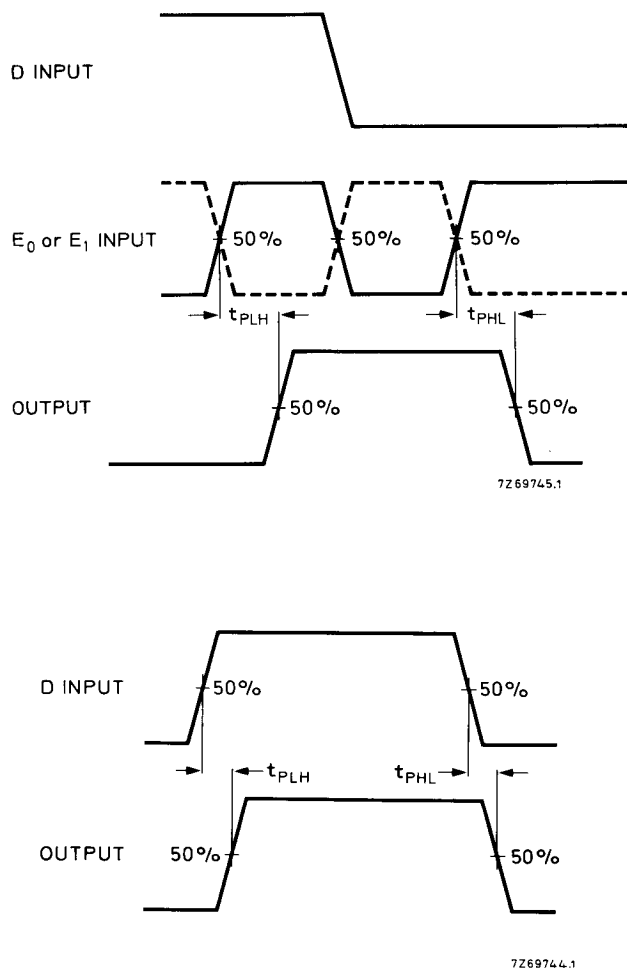


Fig. 5 Waveforms showing propagation delays for D to O, with latch enabled.

Note

Either E₀ or E₁ is held HIGH or LOW while the other enable input is pulsed as the function table shows.

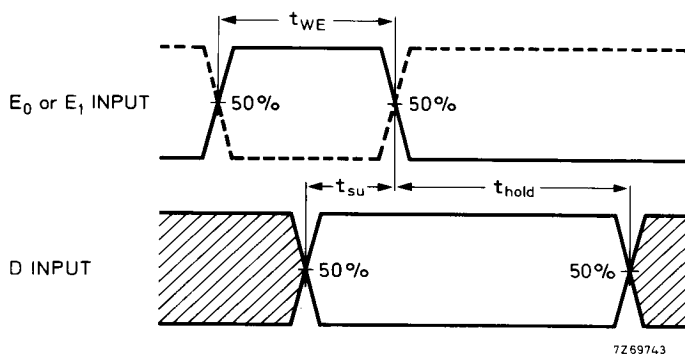


Fig. 6 Waveforms showing minimum enable pulse width, set-up time and hold time for E and D. Set-up and hold-times are shown as positive values but may be specified as negative values.