

HEX NON-INVERTING BUFFERS



The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

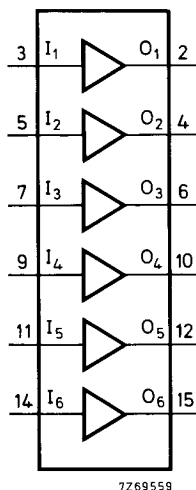


Fig. 1 Functional diagram.

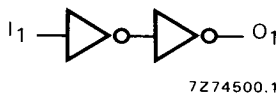


Fig. 3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4050B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

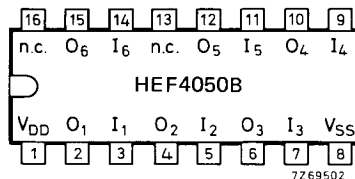


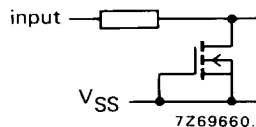
Fig. 2 Pinning diagram.

HEF4050BP : 16-lead DIL; plastic (SOT-38Z).
HEF4050BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4050BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection

Fig.4 Input protection circuit that allows input voltages in excess of V_{DD} .

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications



D.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

HEF	V_{DD} V	V_O V	symbol	$T_{amb}(^{\circ}\text{C})$					
				-40		+25		+85	
				min.	max.	min.	max.	min.	max.
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	—	2,9	—	2,3	—
	10	0,5		12,0	—	10,0	—	8,0	—
	15	1,5		24,0	—	20,0	—	16,0	—
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	—	0,44	—	0,36	—
	10	9,5		1,3	—	1,1	—	0,9	—
	15	13,5		3,6	—	3,0	—	2,4	—
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	—	1,4	—	1,1	—

HEC	V_{DD} V	V_O V	symbol	$T_{amb}(^{\circ}\text{C})$					
				-55		+25		+125	
				min.	max.	min.	max.	min.	max.
Output (sink) current LOW	4,75	0,4	I_{OL}	3,6	—	2,9	—	1,9	—
	10	0,5		12,5	—	10,0	—	6,7	—
	15	1,5		25,0	—	20,0	—	13,0	—
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	—	0,44	—	0,36	—
	10	9,5		1,3	—	1,1	—	0,9	—
	15	13,5		3,6	—	3,0	—	2,4	—

A.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays I_n O_n HIGH to LOW	5	t_{PHL}	35	70	ns	$26\text{ ns} + (0,18\text{ ns/pF})C_L$
	10		20	35	ns	$16\text{ ns} + (0,08\text{ ns/pF})C_L$
	15		15	30	ns	$12\text{ ns} + (0,05\text{ ns/pF})C_L$
LOW to HIGH	5	t_{PLH}	55	110	ns	$28\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		25	55	ns	$14\text{ ns} + (0,23\text{ ns/pF})C_L$
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF})C_L$
Output transition times HIGH to LOW	5	t_{THL}	25	50	ns	$7\text{ ns} + (0,35\text{ ns/pF})C_L$
	10		10	20	ns	$3\text{ ns} + (0,14\text{ ns/pF})C_L$
	15		7	14	ns	$2\text{ ns} + (0,09\text{ ns/pF})C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF})C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF})C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF})C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$3\,800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$11\,600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$65\,900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	