HEX INVERTER

The HEF4069UB is a general purpose hex inverter. Each of the six inverters is a single stage.

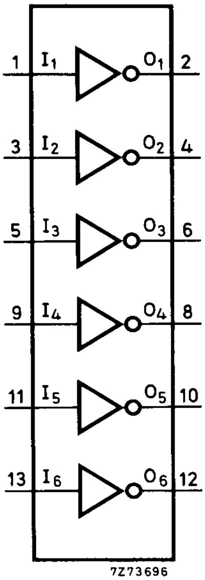


Fig. 1 Functional diagram.

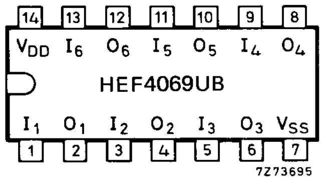


Fig. 2 Pinning diagram.

HEF4069UBP : 14-lead DIL; plastic (SOT-27).
HEF4069UBD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4069UBT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

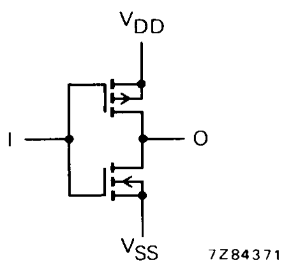


Fig. 3 Schematic diagram (one inverter).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications for V_{IH}/V_{IL} unbuffered stages

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
	10	t_{PHL}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	25	ns	7 ns + (0,16 ns/pF) C_L
LOW to HIGH	5		40	80	ns	13 ns + (0,55 ns/pF) C_L
	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$22\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

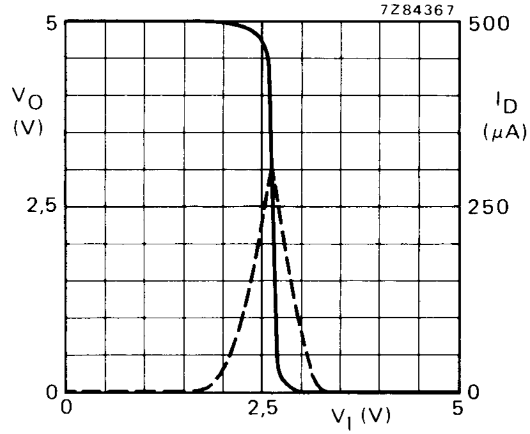


Fig. 4 Typical transfer characteristics;
—— V_O; – – – I_D(drain current); $I_O = 0$;
$V_{DD} = 5$ V.

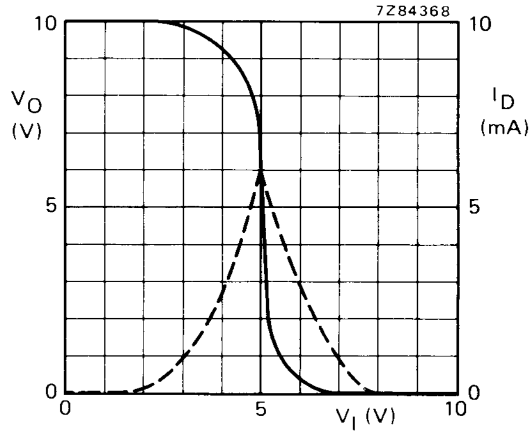


Fig. 5 Typical transfer characteristics;
—— V_O; – – – I_D(drain current); $I_O = 0$;
$V_{DD} = 10$ V.

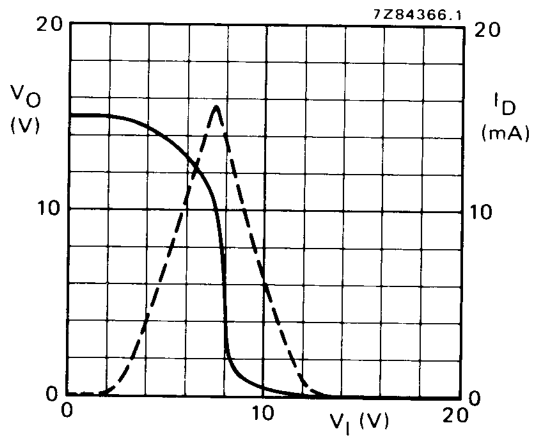
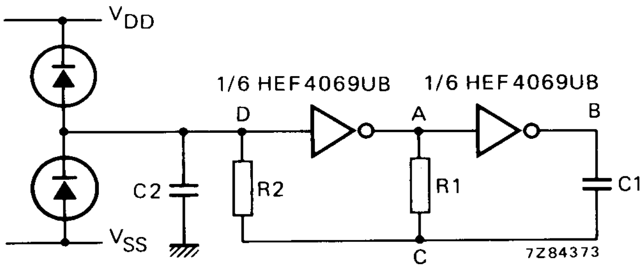


Fig. 6 Typical transfer characteristics;
—— V_O; – – – I_D(drain current) $I_O = 0$;
$V_{DD} = 15$ V.

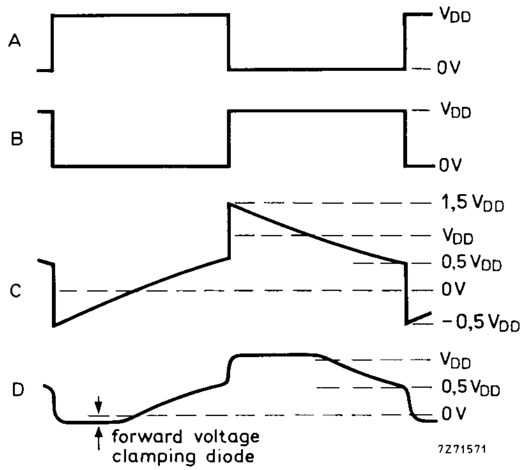
APPLICATION INFORMATION

Some examples of applications for the HEF4069UB are shown below.

In Fig. 7 an astable relaxation oscillator is given. The oscillation frequency is mainly determined by R1C1, provided R1 << R2 and R2C2 << R1C1.



(a)



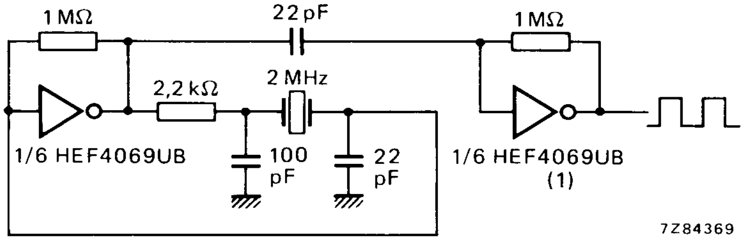
(b)

Fig. 7(a) Astable relaxation oscillator using two HEF4069UB inverters; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2\,V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

V_{ST} is the signal threshold level of the inverter. The period is fairly independent of V_{DD}, V_{ST} and temperature. The duty factor, however, is influenced by V_{ST}.



(1) This inverter is added to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig. 8 Crystal oscillator for frequencies up to 10 MHz, using two HEF4069UB inverters.

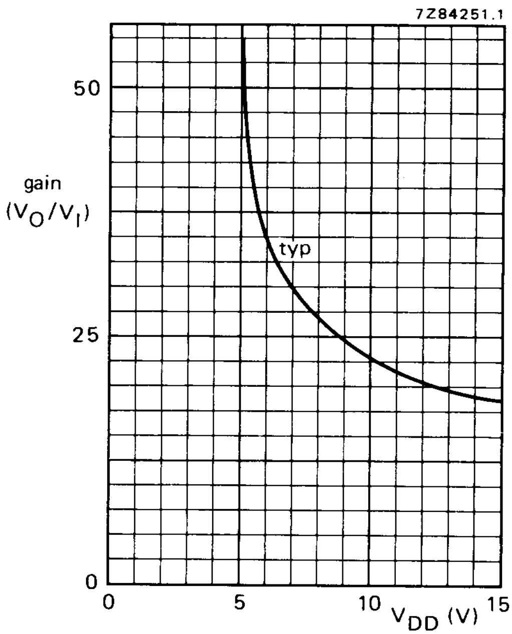


Fig. 9 Voltage gain (V_O/V_I) as a function of supply voltage.

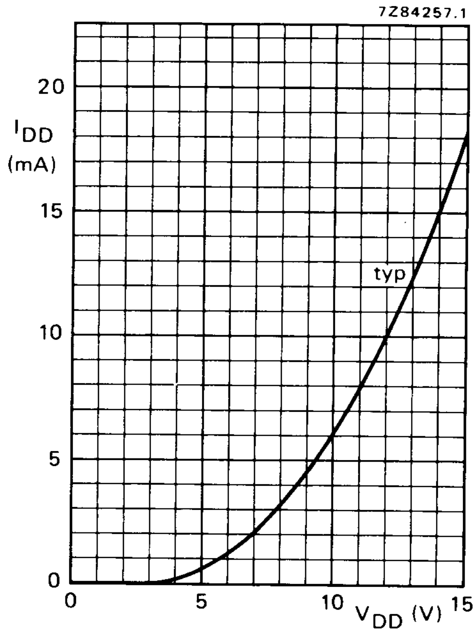


Fig. 10 Supply current as a function of supply voltage.

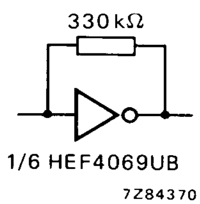


Fig. 11 Test set-up for measuring graphs of Figs 9 and 10.
It is also an example of an analogue amplifier using one HEF4069UB.

APPLICATION INFORMATION (continued)

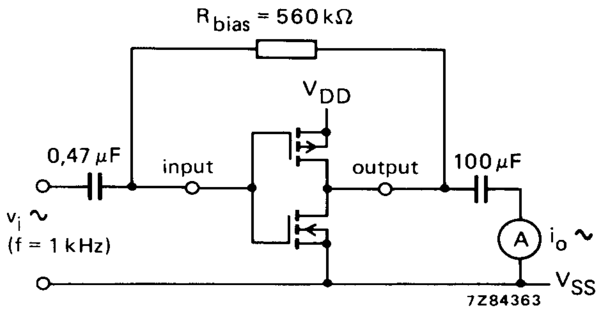


Fig. 12 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 13).

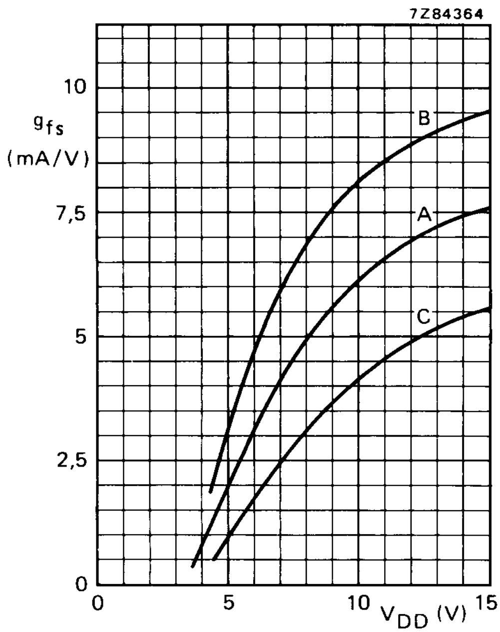


Fig. 13 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

Curves in Fig. 13:

A : average,
B : average + 2 s,
C : average −2 s, in where:
's' is the observed standard deviation.