QUADRUPLE D-TYPE REGISTER WITH 3-STATE OUTPUTS

The HEF4076B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), two active LOW data enable inputs ($\overline{ED}_0$ and $\overline{ED}_1$), a common clock input (CP), four 3-state outputs (O_0 to O_3), two active LOW output enable inputs ($\overline{EO}_0$ and $\overline{EO}_1$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is stored in the four flip-flops on the LOW to HIGH transition of CP if both $\overline{ED}_0$ and $\overline{ED}_1$ are LOW. A HIGH on either $\overline{ED}_0$ or $\overline{ED}_1$ prevents the flip-flops from changing on the LOW to HIGH transition of CP, independent of the information on D_0 to D_3. When both $\overline{EO}_0$ and $\overline{EO}_1$ are LOW, the contents of the four flip-flops are available at O_0 to O_3. A HIGH on either $\overline{EO}_0$ or $\overline{EO}_1$ forces O_0 to O_3 into the high impedance OFF-state. A HIGH on MR resets all four flip-flops, independent of all other input conditions.

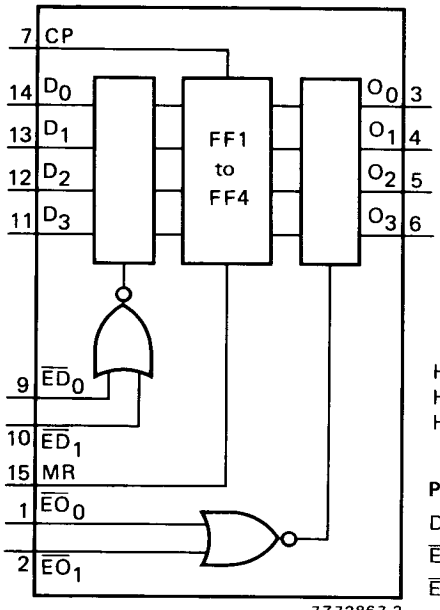

Fig. 1 Functional diagram.

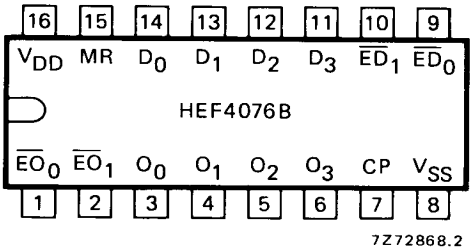

Fig. 2 Pinning diagram.

HEF4076BP : 16-lead DIL; plastic (SOT-38Z).
HEF4076BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4076BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

D_0 to D_3	data inputs
$\overline{ED}_0$, $\overline{ED}_1$	data enable inputs (active LOW)
$\overline{EO}_0$, $\overline{EO}_1$	output enable inputs (active LOW)
CP	clock input (LOW to HIGH, edge-triggered)
MR	master reset input
O_0 to O_3	data outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

Products approved to CECC 90 104-051.

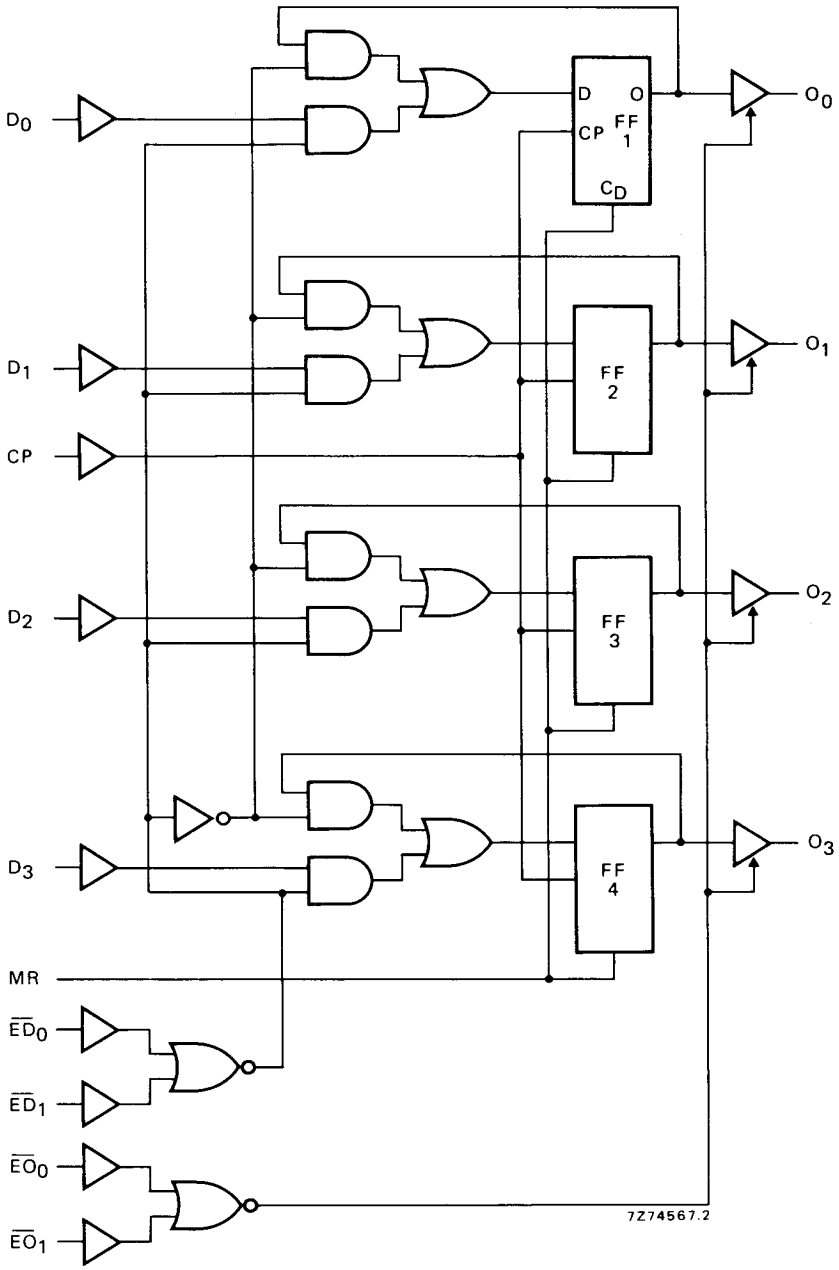

Fig. 3 Logic diagram.

FUNCTION TABLE

inputs					outputs
MR	CP	$\overline{ED}_0$	$\overline{ED}_1$	D_n	O_n
H	X	X	X	X	L
L	∫	H	X	X	no change
L	∫	X	H	X	no change
L	∫	L	L	H	H
L	∫	L	L	L	L
L	⌡	X	X	X	no change

$\overline{EO}_0 = \overline{EO}_1$ = LOW

When either $\overline{EO}_0$ or $\overline{EO}_1$ is HIGH, the outputs are disabled (high impedance OFF-state).
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌡ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP → O_n	5			150	305 ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	85 ns	37 ns + (0,16 ns/pF) C_L
	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
MR → O_n	5			95	190 ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60 ns	9 ns + (0,42 ns/pF) C_L
HIGH to LOW	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5			60	120 ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
3-state propagation delays						
Output disable times	5			50	105 ns	
$\overline{EO}_n$ → O_n	10	t_{PHZ}		35	70 ns	
HIGH	15			30	65 ns	
	5			45	90 ns	
LOW	10	t_{PLZ}		30	65 ns	
	15			30	60 ns	
Output enable times	5			65	130 ns	
$\overline{EO}_n$ → O_n	10	t_{PZH}		30	55 ns	
HIGH	15			20	40 ns	
	5			60	120 ns	
LOW	10	t_{PZL}		25	50 ns	
	15			20	35 ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Set-up times	5		10	−15		ns	
$D_n \rightarrow CP$	10	t_{su}	0	−10		ns	
	15		0	−5		ns	
	5		0	−50		ns	
$\overline{ED}_n \rightarrow CP$	10	t_{su}	0	−20		ns	
	15		0	−15		ns	
Hold times	5		55	30		ns	
$D_n \rightarrow CP$	10	t_{hold}	20	10		ns	
	15		15	10		ns	
	5		25	−25		ns	
$\overline{ED}_n \rightarrow CP$	10	t_{hold}	10	−10		ns	
	15		5	−5		ns	see also waveforms Fig. 4
Minimum clock pulse width; LOW	5		120	60		ns	
	10	t_{WCPL}	45	20		ns	
	15		30	15		ns	
Minimum MR pulse width; HIGH	5		55	25		ns	
	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time for MR	5		90	45		ns	
	10	t_{RMR}	35	15		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5		4	8		MHz	
	10	f_{max}	11	22		MHz	
	15		16	32		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$24\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

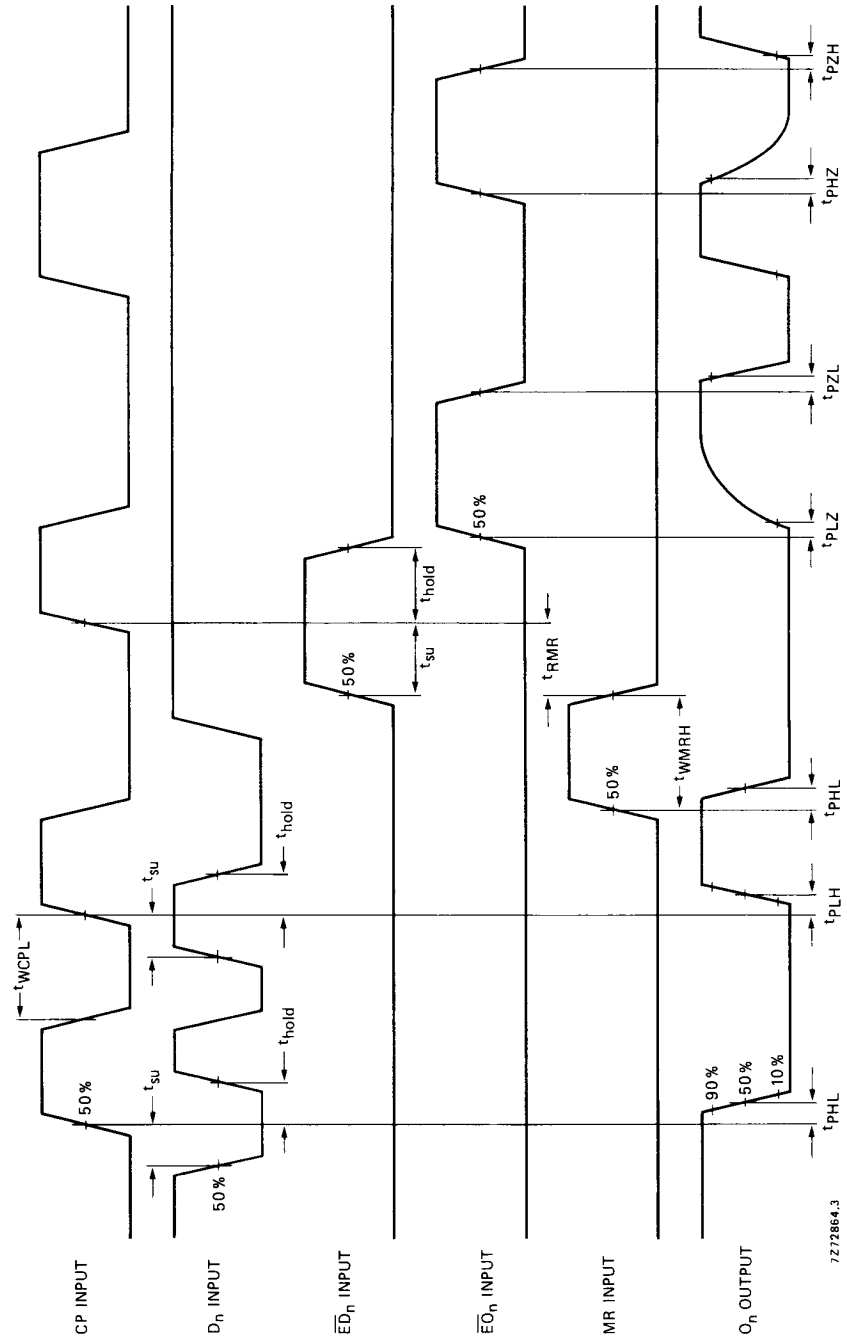

Fig. 4 Waveforms showing propagation delays, output disable/enable times, minimum CP and MR pulse widths, set-up and hold times for D_n to CP and $\overline{ED}_n$ to CP, and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.