

BCD UP/DOWN COUNTER



The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if $\overline{CE}$ is LOW. UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 and O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of all other input conditions.

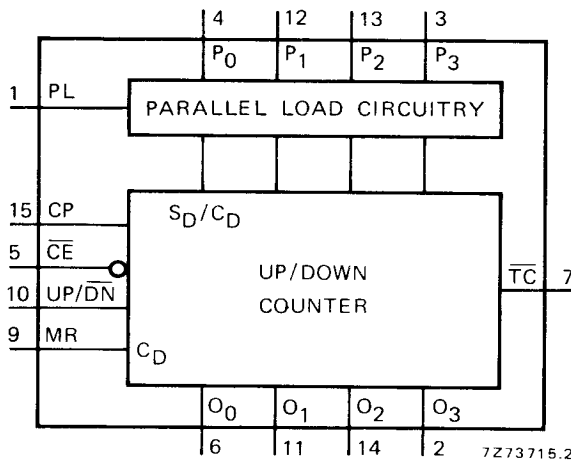


Fig. 1 Functional diagram.

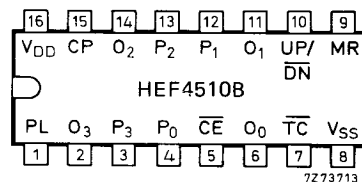


Fig. 2 Pinning diagram.

HEF4510BP : 16-lead DIL; plastic (SOT-38Z).

HEF4510BD : 16-lead DIL; ceramic (cerdip) (SOT-74).

HEF4510BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

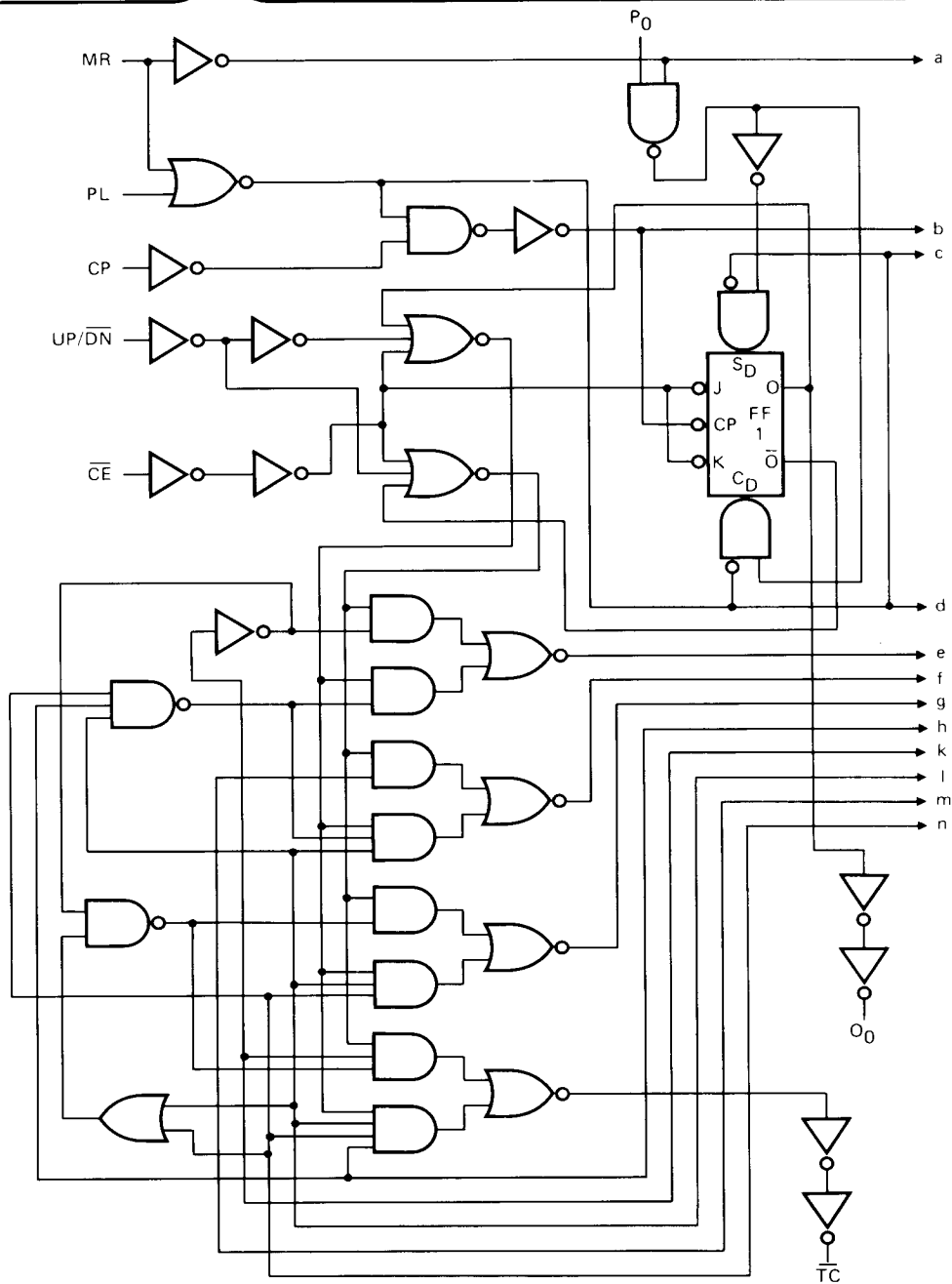
PINNING

PL	parallel load input (active HIGH)	UP/DN	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{CE}$	count enable input (active LOW)	$\overline{TC}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA

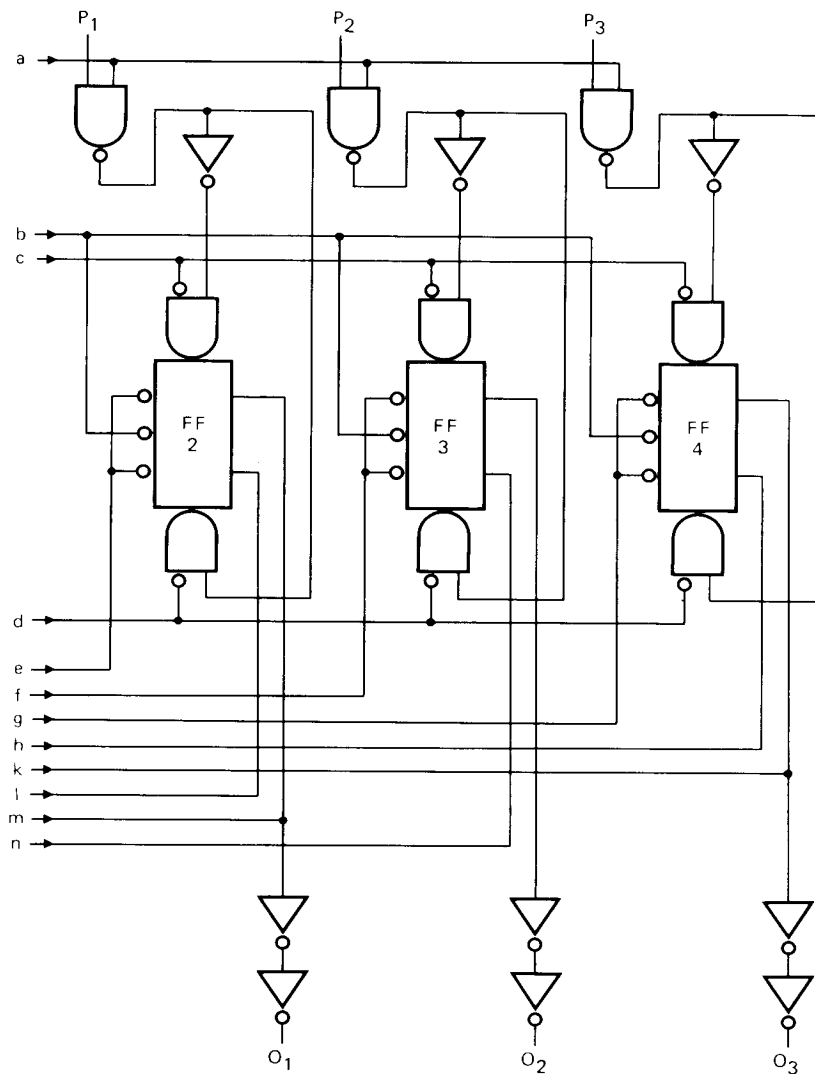
I_{DD} LIMITS category MSI

see Family Specifications



7275079.1

Fig. 3a Logic diagram (continued in Fig. 3b).



7Z75080.1

Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

MR	PL	UP/DN	CE	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	/	count down
L	L	H	L	/	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
/ = positive-going transition

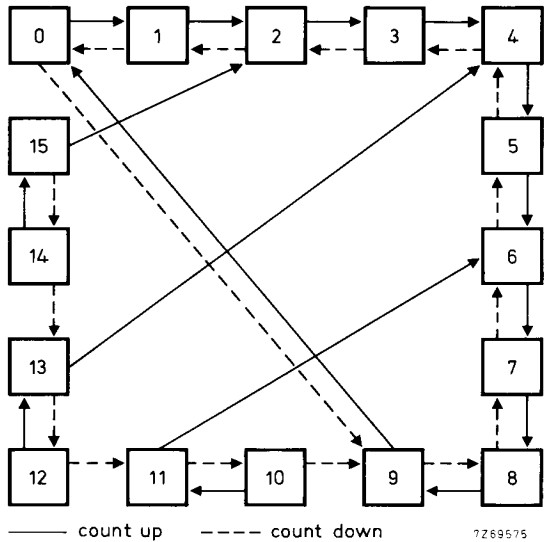


Fig. 4 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{ (\overline{UP/DN}) \cdot O_0 \cdot O_3 + (\overline{UP/DN}) \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	1000 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	4500 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	11 200 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
CP → O _n	5			145	290	ns	118 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C _L
	15			45	90	ns	37 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			155	310	ns	128 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C _L
	15			45	90	ns	37 ns + (0,16 ns/pF) C _L
CP → $\overline{TC}$	5			260	525	ns	233 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		105	210	ns	94 ns + (0,23 ns/pF) C _L
	15			75	150	ns	67 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			180	360	ns	153 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C _L
	15			55	115	ns	47 ns + (0,16 ns/pF) C _L
PL → O _n	5			125	255	ns	98 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C _L
	15			40	85	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			170	340	ns	143 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C _L
	15			50	105	ns	42 ns + (0,16 ns/pF) C _L
PL → $\overline{TC}$	5			250	500	ns	223 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		110	220	ns	99 ns + (0,23 ns/pF) C _L
	15			80	160	ns	72 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			250	500	ns	223 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		110	220	ns	99 ns + (0,23 ns/pF) C _L
	15			80	160	ns	72 ns + (0,16 ns/pF) C _L
$\overline{CE}$ → $\overline{TC}$	5			165	330	ns	138 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C _L
	15			50	100	ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			145	290	ns	118 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		60	125	ns	49 ns + (0,23 ns/pF) C _L
	15			45	95	ns	37 ns + (0,16 ns/pF) C _L
MR → O _n , $\overline{TC}$	5			205	405	ns	178 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C _L
	15			45	85	ns	37 ns + (0,16 ns/pF) C _L
MR → $\overline{TC}$	5			225	450	ns	198 ns + (0,55 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C _L
	15			50	100	ns	42 ns + (0,16 ns/pF) C _L

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Output transition times	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{THL}		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t_{TLH}		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Minimum clock pulse width; LOW	5		95	45	ns	
	10	t_{WCPL}	35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5		105	55	ns	
	10	t_{WPLH}	45	25	ns	
	15		35	15	ns	
Minimum MR pulse width; HIGH	5		120	60	ns	
	10	t_{WMRH}	50	25	ns	
	15		40	20	ns	
Recovery time for MR	5		130	65	ns	
	10	t_{RMR}	45	20	ns	
	15		30	15	ns	
Recovery time for PL	5		150	75	ns	
	10	t_{RPL}	50	25	ns	
	15		30	15	ns	
Set-up times	5		100	50	ns	
$P_n \rightarrow PL$	10	t_{su}	50	25	ns	
	15		40	20	ns	
$UP/\overline{DN} \rightarrow CP$	5		250	125	ns	
	10	t_{su}	100	50	ns	
	15		75	35	ns	
$\overline{CE} \rightarrow PL$	5		120	60	ns	
	10	t_{su}	40	20	ns	
	15		25	10	ns	
Hold times	5		10	-40	ns	
$P_n \rightarrow PL$	10	t_{hold}	5	-20	ns	
	15		0	-20	ns	
$UP/\overline{DN} \rightarrow CP$	5		35	-90	ns	
	10	t_{hold}	15	-35	ns	
	15		15	-25	ns	
$\overline{CE} \rightarrow CP$	5		20	-40	ns	
	10	t_{hold}	5	-15	ns	
	15		5	-10	ns	
Maximum clock pulse frequency	5		5	10	MHz	
	10	f_{max}	12	24	MHz	
	15		17	34	MHz	

 see also waveforms
Figs 5 and 6

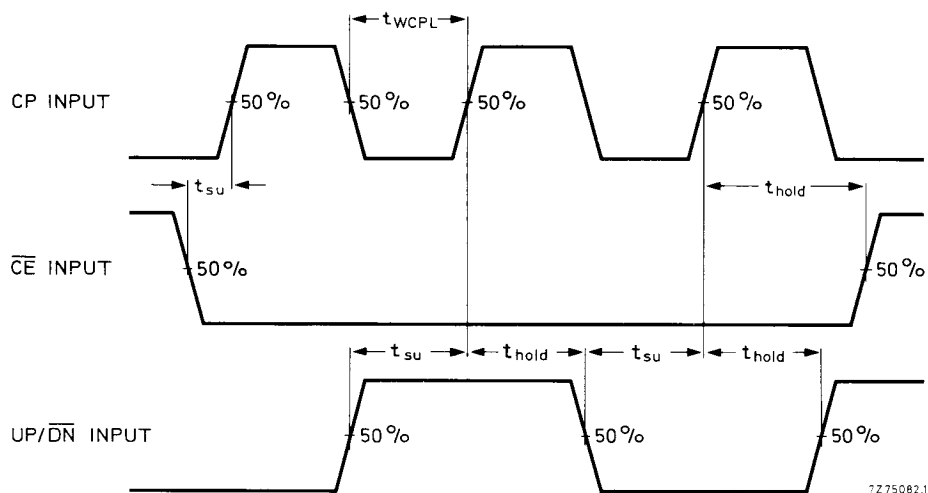


Fig. 5 Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/ $\overline{DN}$ to CP.

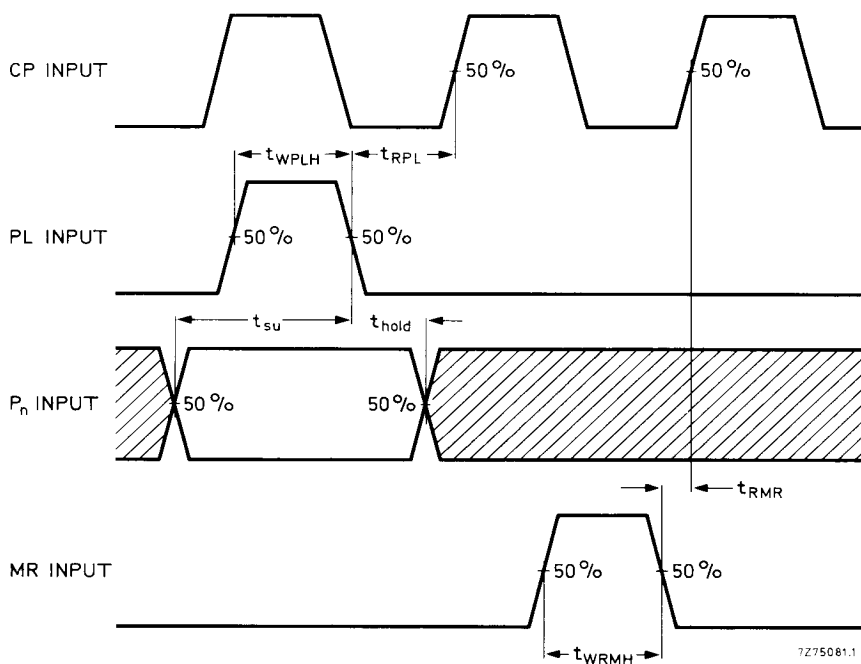


Fig. 6 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

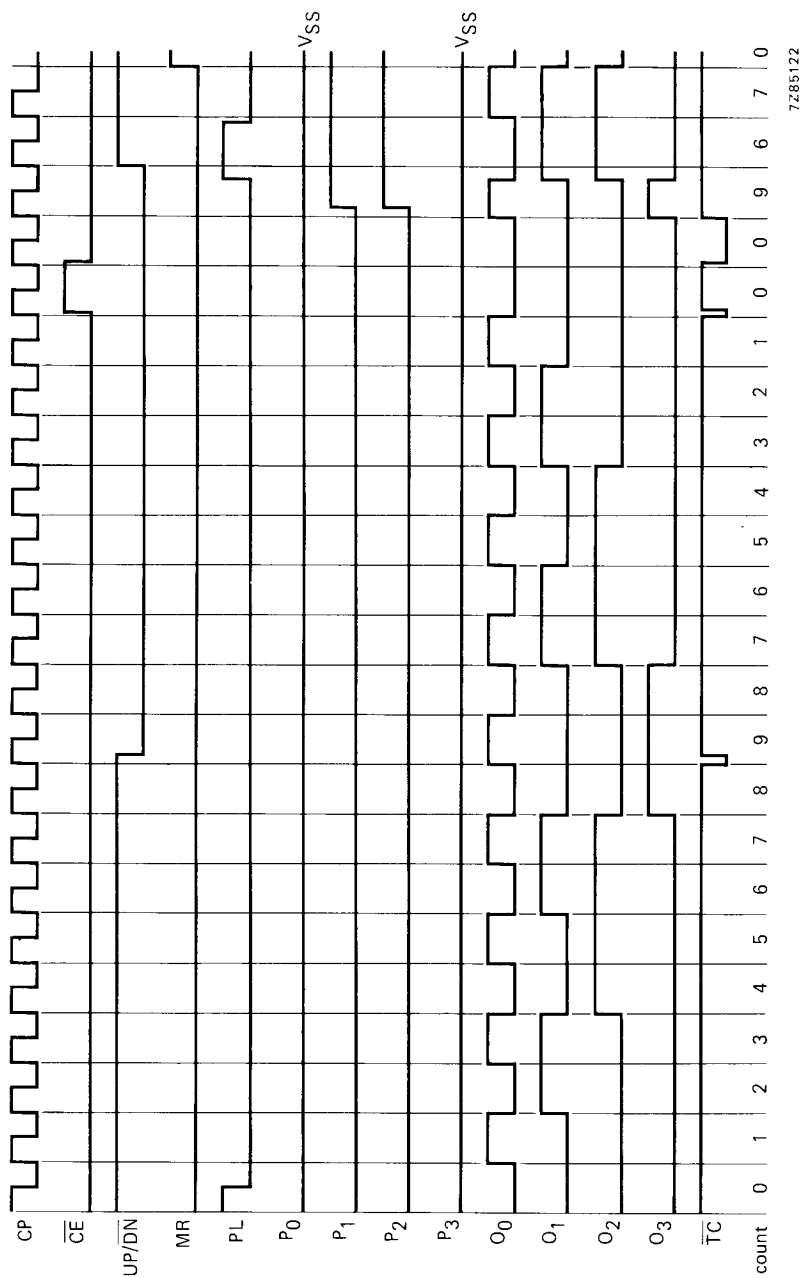


Fig. 7 Timing diagram.