1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

The HEF4514B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input ($\overline{E}$). The 16 outputs (O_0 to O_{15}) are mutually exclusive active HIGH. When EL is HIGH, the selected output is determined by the data on A_n. When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch. When the HEF4514B is used as a demultiplexer, $\overline{E}$ is the data input and A_0 to A_3 are the address inputs.

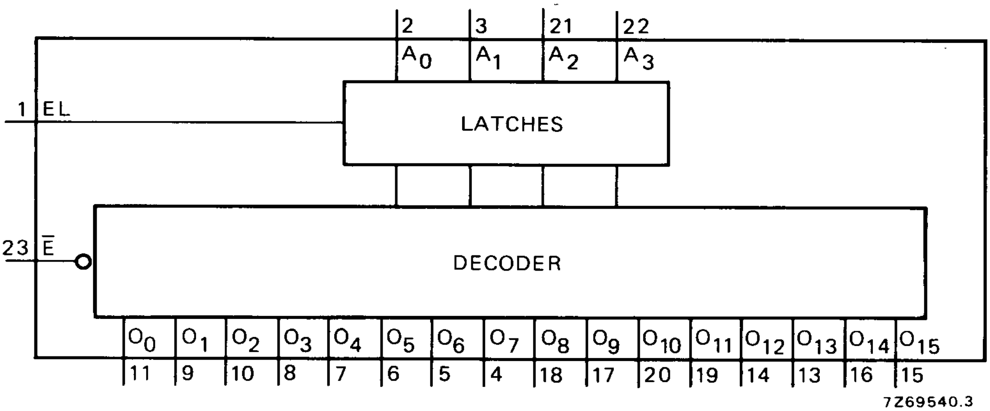

Fig. 1 Functional diagram.

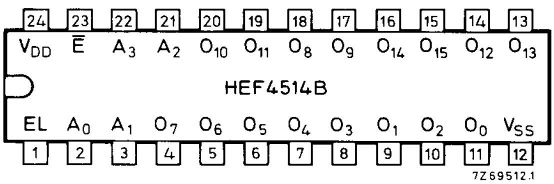

Fig. 2 Pinning diagram.

HEF4514BP : 24-lead DIL; plastic (SOT-101A).
HEF4514BD: 24-lead DIL; ceramic (cerdip) (SOT-94).
HEF4514BT : 24-lead mini-pack; plastic (SO-24; SOT-137A).

PINNING

A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
EL	latch enable input
O_0 to O_{15}	outputs (active HIGH)

APPLICATION INFORMATION

Some examples of applications for the HEF4514B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA
I_{DD} LIMITS category MSI
} see Family Specifications

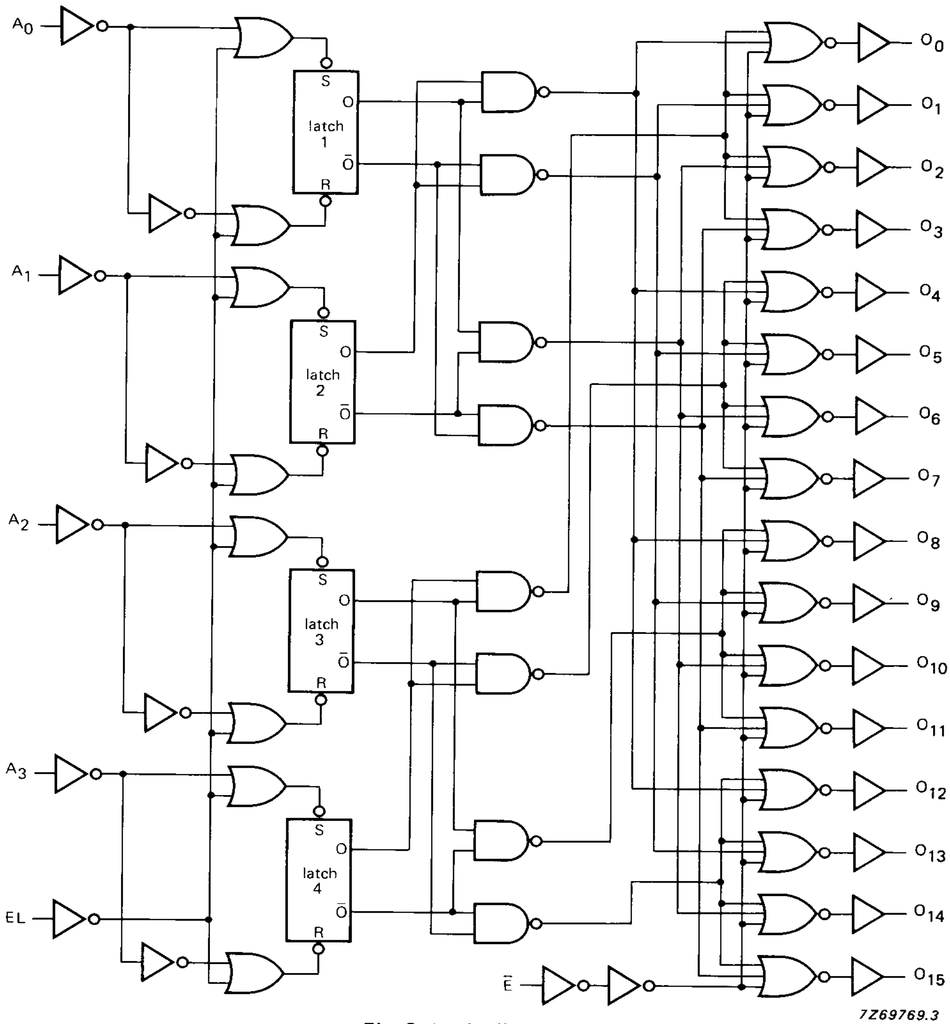

Fig. 3 Logic diagram.

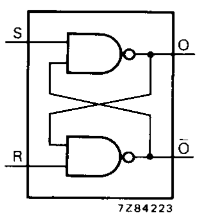

Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs															
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
A_n, EL → O_n	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\overline{E}$ → O_n	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Output transition times HIGH to LOW	5			90	180	ns	40 ns + (1,0 ns/pF) C_L
	10	t_{THL}		35	65	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
LOW to HIGH	5			85	170	ns	35 ns + (1,0 ns/pF) C_L
	10	t_{TLH}		35	70	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
Set-up time $A_n \rightarrow$ EL	5		120	60		ns	see also waveforms Fig. 5
	10	t_{su}	40	20		ns	
	15		30	15		ns	
Hold time $A_n \rightarrow$ EL	5		0	60		ns	
	10	t_{hold}	0	20		ns	
	15		0	15		ns	
Minimum EL pulse width; HIGH	5		120	60		ns	
	10	t_{WELH}	40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$5500\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$16\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

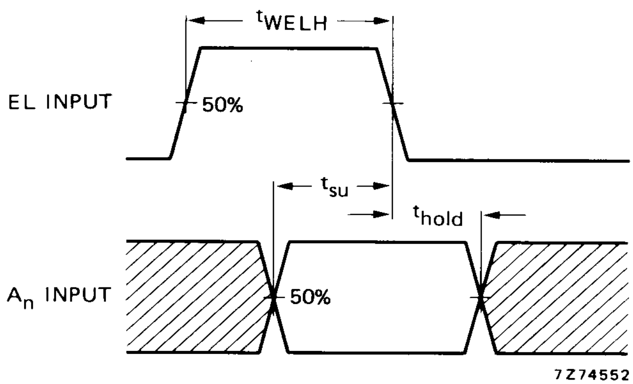

Fig. 5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL.
Set-up and hold times are shown as positive values but may be specified as negative values.