

PROGRAMMABLE TIMER



The HEF4541B is a programmable timer which consists of a 16-stage binary counter, an integrated oscillator to be used with external timing components, an automatic power-on reset and output control logic. The frequency of the oscillator is determined by the external components R_T and C_T within the frequency range 1 Hz to 100 kHz. This oscillator may be replaced by an external clock signal at input RS, the timer advances on the positive-going transition of RS. A LOW on the auto reset input ($\overline{AR}$) and a LOW on the master reset input (MR) enables the internal power-on reset. A HIGH level at input MR resets the counter independent on all other inputs. Resetting disables the oscillator to provide no active power dissipation.

A HIGH at input $\overline{AR}$ turns off the power-on reset to provide a low quiescent power dissipation of the timer. The 16-stage counter divides the oscillator frequency by 2^8 , 2^{10} , 2^{13} or 2^{16} depending on the state of the address inputs (A_0 , A_1). The divided oscillator frequency is available at output O. The phase input (PH) features a complementary output signal. If the mode select input (MODE) is LOW or HIGH the timer can be used respectively as a single transition timer or 2^n frequency divider.

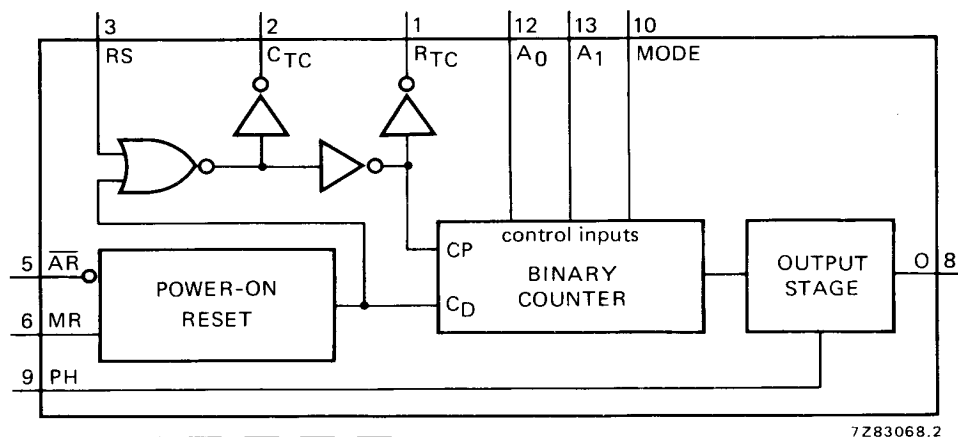


Fig. 1 Functional diagram.

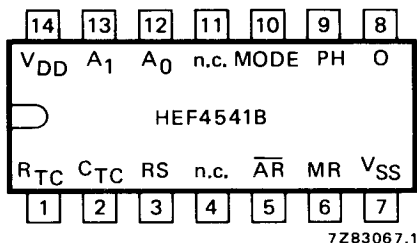


Fig. 2 Pinning diagram.

HEF4541BP : 14-lead DIL; plastic (SOT-27).
HEF4541BD : 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4541BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

FAMILY DATA

see Family Specifications

IDD LIMITS category MSI

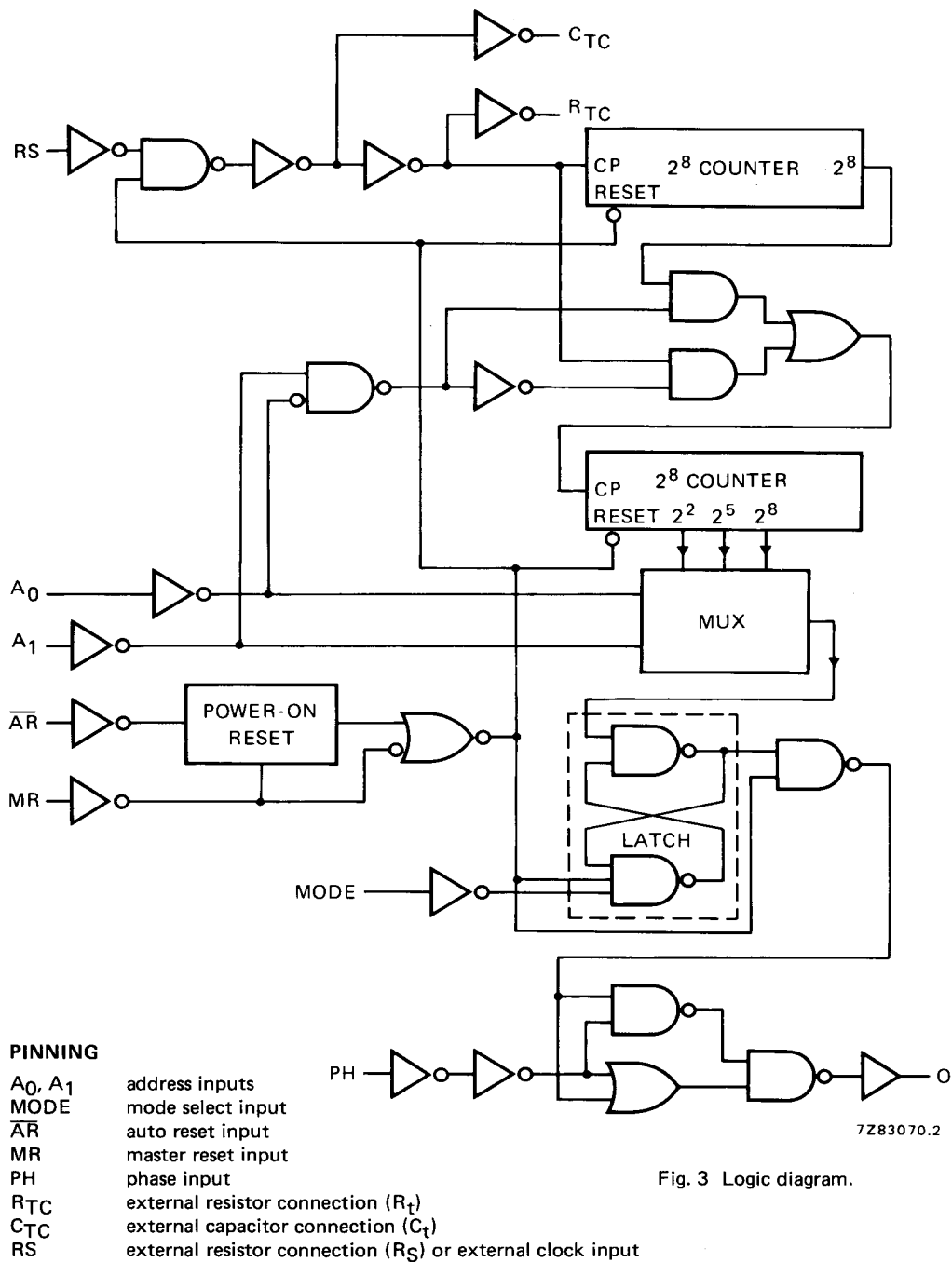


Fig. 3 Logic diagram.

FREQUENCY SELECTION TABLE

A ₀	A ₁	number of counter stages n	$\frac{f_{osc}}{f_{out}} = 2^n$
L	L	13	8 192
L	H	10	1 024
H	L	8	256
H	H	16	65 536

FUNCTION TABLE

inputs				mode
$\overline{AR}$	MR	PH	MODE	
H	L	X	X	auto reset disabled
L	L	X	X	auto reset enabled
X	H	X	X	master reset active
X	L	X	H	normal operation selected
X	L	X	L	division to output
X	L	L	X	single-cycle mode*
X	L	L	X	output initially LOW, after reset
X	L	H	X	output initially HIGH, after reset

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

* The timer is initialized on a reset pulse and the output changes state after 2^{n-1} counts and remains in that state (latched). Reset of this latch is obtained by master reset or by a LOW to HIGH transition on the MODE input.

RC oscillator

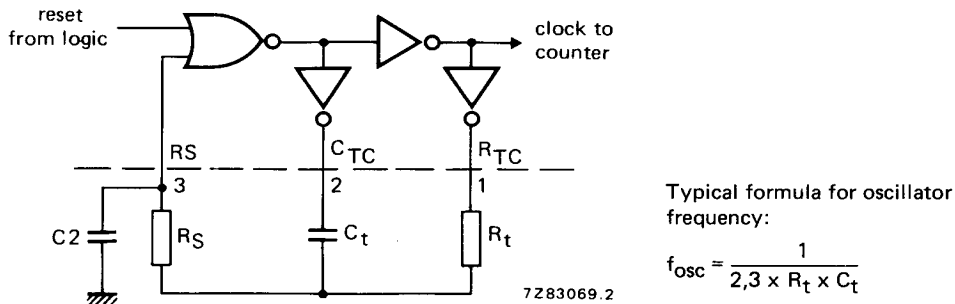


Fig. 4 External component connection for RC oscillator; $R_S \approx 2R_t$.

Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_t \ll R_S$ and $R_S C_2 \ll R_t C_t$. The function of R_S is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500Ω at $V_{DD} = 5 \text{ V}$, 300Ω at $V_{DD} = 10 \text{ V}$ and 200Ω at $V_{DD} = 15 \text{ V}$.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

$$C_t \geq 100 \text{ pF, up to any typical value,}$$

$$10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega.$$

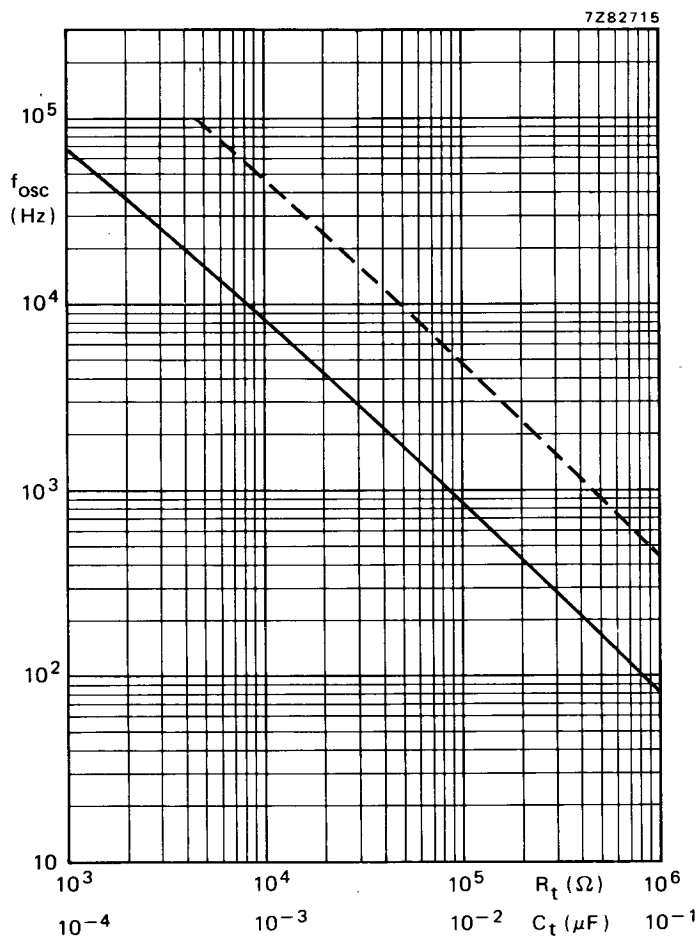


Fig. 5 RC oscillator frequency as a function of R_t and C_t at $V_{DD} = 5$ to 15 V ; $T_{amb} = 25^\circ \text{C}$.

- C_t curve at $R_t = 56 \text{ k}\Omega$; $R_S = 120 \text{ k}\Omega$.
- - - R_t curve at $C_t = 1 \text{ nF}$; $R_S = 2R_t$.

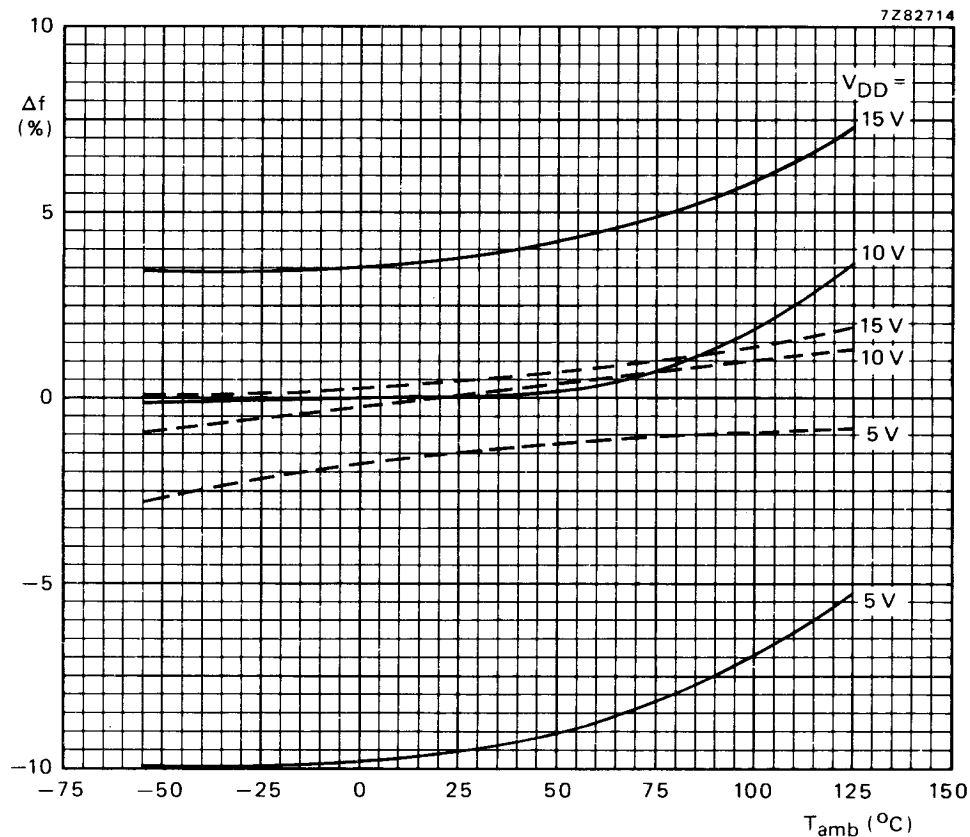


Fig. 6 Frequency deviation (Δf) as a function of ambient temperature; referenced at : f_{osc} at $T_{amb} = 25^\circ C$ and $V_{DD} = 10 V$.

— $R_t = 56 k\Omega$; $C_t = 1 nF$; $R_S = 0$.

- - - $R_t = 56 k\Omega$; $C_t = 1 nF$; $R_S = 120 k\Omega$.

D.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OL} V	V_{OH} V	symbol	T_{amb} (°C)					
					-40		+25		+85	
					min.	max.	min.	typ.	max.	min. max.
Supply current power-on reset enabled (note)	5			I_D	—	80	—	20	80	— 230 μA
	10				—	750	—	250	600	— 700 μA
	15				—	1600	—	500	1300	— 1500 μA
Supply voltage for automatic reset initialization (note)				V_{DD}	—	—	8,5	5	—	— — V
Output current HIGH; C_{TC} , R_{TC}	5		4,6	$-I_{OH}$	0,5	—	0,4	—	—	0,3 — mA
	10		9,5		1,4	—	1,2	—	—	0,95 — mA
	15		13,5		4,8	—	4,0	—	—	3,2 — mA
Output current LOW; C_{TC} , R_{TC}	5		2,5	$-I_{OH}$	1,4	—	1,2	—	—	0,95 — mA
	5	0,4		I_{OL}	0,33	—	0,27	—	—	0,20 — mA
	10	0,5			1,00	—	0,85	—	—	0,68 — mA
	15	1,5			3,20	—	2,70	—	—	2,30 — mA

Note

All inputs at 0 V or V_{DD} , except input $\overline{AR}$ = input MR = 0 V (power-on reset active).

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)*
Dynamic power dissipation per package (P)	5	$1\,300 f_i + f_o C_L V_{DD}^2$
	10	$5\,300 f_i + f_o C_L V_{DD}^2$
	15	$12\,000 f_i + f_o C_L V_{DD}^2$
Total power dissipation when using the on-chip oscillator (P)	5	$1\,300 f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 10 V_{DD}$
	10	$5\,300 f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 100 V_{DD}$
	15	$12\,000 f_{osc} + f_o C_L V_{DD}^2 + 2C_t V_{DD}^2 f_{osc} + 400 V_{DD}$

* where:

 f_i = input frequency (MHz) f_o = output frequency (MHz) C_L = load capacitance (pF) V_{DD} = supply voltage (V) C_t = timing capacitance (pF) f_{osc} = oscillator frequency (MHz)

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
RS $\rightarrow$ O						
2 ⁸ selected	5			375	750 ns	348 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		150	300 ns	139 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t _{PLH}		110	220 ns	102 ns + (0,16 ns/pF) C_L
RS $\rightarrow$ O						
2 ¹⁰ selected	5			425	850 ns	398 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		165	330 ns	154 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t _{PLH}		120	240 ns	112 ns + (0,16 ns/pF) C_L
RS $\rightarrow$ O						
2 ¹³ selected	5			510	1020 ns	483 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		190	380 ns	179 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t _{PLH}		135	270 ns	127 ns + (0,16 ns/pF) C_L
RS $\rightarrow$ O						
2 ¹⁶ selected	5			575	1150 ns	548 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		210	420 ns	199 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t _{PLH}		150	300 ns	142 ns + (0,16 ns/pF) C_L
Minimum clock pulse width; LOW	5		60	30	ns	
	10	t _{WRSL}	30	15	ns	
	15		24	12	ns	
Minimum reset pulse width; HIGH	5		60	30	ns	
	10	t _{WMRH}	30	15	ns	
	15		24	12	ns	
Maximum clock pulse frequency	5		8	16	MHz	
	10	f _{max}	15	30	MHz	
	15		18	36	MHz	
Oscillator frequency	5			90	kHz	$R_t = 5\text{ k}\Omega$ $C_t = 1\text{ nF}$ $R_S = 10\text{ k}\Omega$
	10	f _{osc}		90	kHz	
	15			90	kHz	
Oscillator frequency	5			8	kHz	$R_t = 56\text{ k}\Omega$ $C_t = 1\text{ nF}$ $R_S = 120\text{ k}\Omega$
	10	f _{osc}		8	kHz	
	15			8	kHz	