DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4556B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active LOW ($\overline{O}_0$ to $\overline{O}_3$). When used as a decoder, $\overline{E}$ when HIGH, forces $\overline{O}_0$ to $\overline{O}_3$ HIGH. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with $\overline{E}$ as data input. All unselected outputs are HIGH.

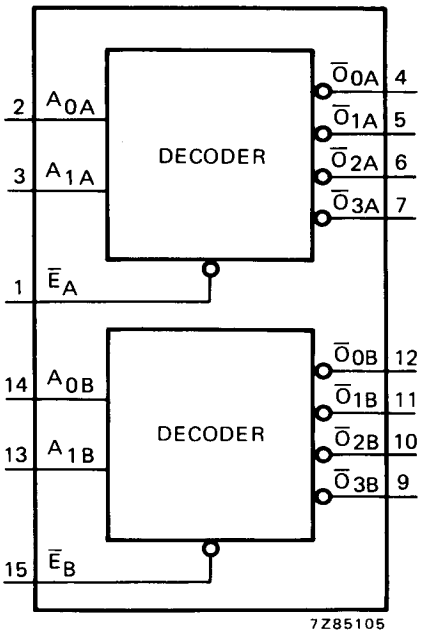

Fig. 1 Functional diagram.

Fig. 2 Pinning diagram.

HEF4556BP : 16-lead DIL; plastic (SOT-38Z).
HEF4556BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4556BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
$\overline{O}_0$ to $\overline{O}_3$	outputs (active LOW)

FAMILY DATA
I_{DD} LIMITS category MSI
see Family Specifications

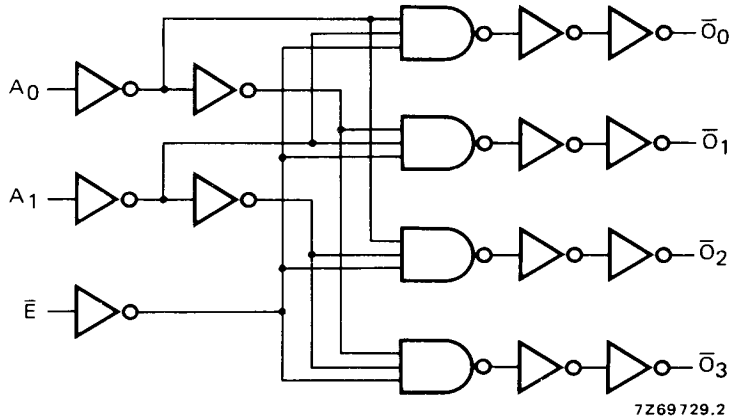

Fig. 3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

inputs			outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$A_n \rightarrow \overline{O}_n$	5			130	255	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow \overline{O}_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			105	205	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	4400 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	18 000 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	
	15	43 300 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	

APPLICATION INFORMATION

Some examples of applications for the HEF4556B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.