# UNIVERSAL TIMER MODULE

The HEF4753B is a universal timer module for counting and dividing as well as for event-recognition and manipulation of input sequences.
The following functions are included: synchronization and edge-detection of the input signal, programmable counter, clock divider with different lengths, operating mode decoder, control logic and output multiplexer.
Depending on the operating mode and the application, the circuit works as a presettable 8-bit counter with transient-pulse suppression, pulse duration selector divider, counter, positive or negative edge delaying module or low-frequency control circuit.
All manipulation possibilities depend on a time scaling, which is adjustable by the 8-bit programmable counter and the system clock. The system clock can be divided internally by 1, 16, 256 or 4096 as input clock for the counter. In all cases the manipulated input sequence appears at the only output OUT.

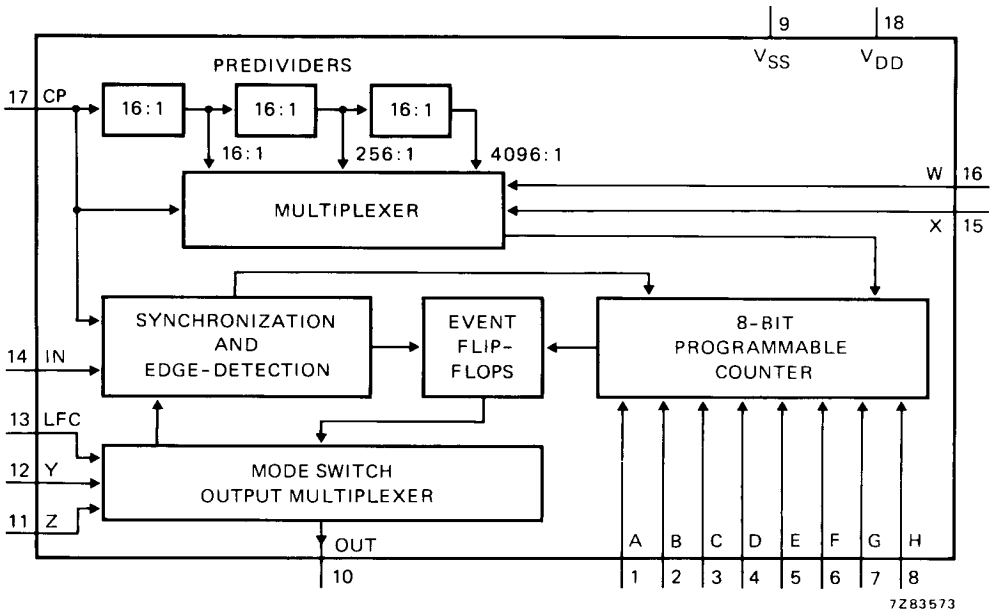
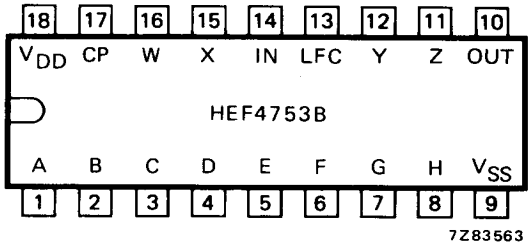



Fig. 1 Functional diagram.

**FAMILY DATA**

**$I_{DD}$ LIMITS category LSI**

see Family Specifications




HEF4753BP: 18-lead DIL; plastic (SOT-102).
HEF4753BD: 18-lead DIL; ceramic (cerdip) (SOT-133B).

Fig. 2 Pinning diagram.

## FUNCTION TABLES

| inputs | | | operating mode |
|---|---|---|---|
| LFC | Y | Z | |
| L | L | H | counter |
| L | H | L | divider |
| H | H | L | delayed LOW to HIGH edge |
| H | L | H | delayed HIGH to LOW edge |
| H | H | H | transient pulse suppression |
| L | H | H | frequency recognition |
| LFC | L | L | digital pulse duration selector |

H = HIGH state (the more positive voltage).
L = LOW state (the less positive voltage).

**Programmable 8-bit counter ***

| inputs active LOW | value |
|---|---|
| A | 1 |
| B | 2 |
| C | 4 |
| D | 8 |
| E | 16 |
| F | 32 |
| G | 64 |
| H | 128 |

**12-bit predivider**

| W | X | clock for programmable counter CP/X |
|---|---|---|
| L | L | X = 1 |
| L | H | X = 16 |
| H | L | X = 256 |
| H | H | X = 4096 |

* All inputs A to H HIGH is not allowed.

## FUNCTIONAL DESCRIPTION

### Clock divider and decoder

The clock signal at input CP is, at its original frequency, the system clock, but it also drives the programmable counter. The counter input frequency can be predivided by the factors 1/16, 1/256 and 1/4096, depending on the logic state of inputs W and X (according to the function tables above).

### 8-bit programmable counter

The 8 inputs A to H are the set inputs of the 8 counter flip-flops. The setting is triggered by an edge of the input signal (at input IN) depending on of the chosen mode.

**Event flip-flops, synchronization and edge-detection**

The event flip-flops are used to recognize the positive and/or negative edge of the input signal at IN. Parts of the flip-flops are used together with the programmable 8-bit counter as a retriggerable mono-flop, which defines the time scaling for event recognition.
The input IN is synchronized by the clock signal CP.

**Mode switch and output multiplexer**

This function switches the chosen output to the output (OUT) and gives the mode of which the edge at input IN has to be detected. The inputs Z, Y and LFC give 7 modes +1, that means in mode 'Digital Filter' the input LFC can be HIGH or LOW.

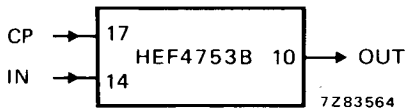
## OPERATING MODES

The circuit has 6 operating modes which are activated by the logic state of inputs LFC, Y and Z. An extra mode is possible by using two circuits which are connected such so they function as a digital band-filter.

**1. Counter mode** (LFC = LOW; Y = LOW; Z = HIGH)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig. 3 and note 1).

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | L | H | H | H | H | H | L | L | L | L | H |



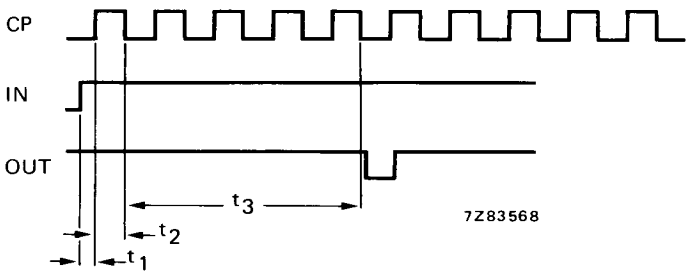




Fig. 3 Timing diagram for counter mode; $t_1$ = delay until set of 8-bit counter; $t_2$ = delay to set 8-bit counter; $t_3$ = predefined delay by programming.

**OPERATING MODES** (continued)

**2. Divider mode** (LFC = LOW; Y = HIGH; Z = LOW)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig. 4 and note 1).

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | H | H | H | H | H | H | L | L | L | H | L |

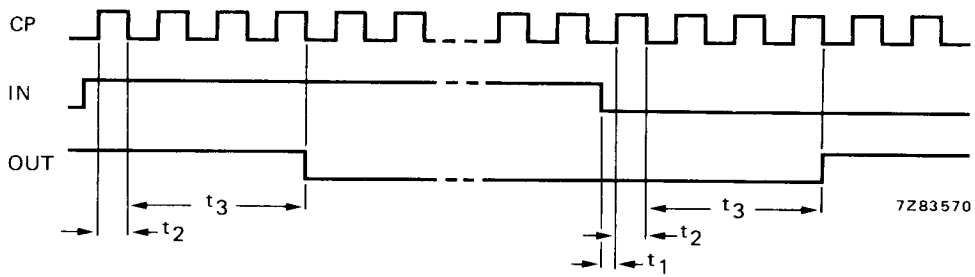




Fig. 4 Timing diagram for divider mode; $t_1$ = delay until set of 8-bit counter; $t_2$, $t_3$ see Fig. 3.

**3. Delayed LOW to HIGH edge mode; see note 2** (LFC = HIGH; Y = HIGH; Z = LOW)

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | L | H | H | H | H | H | H | L | L | H | H | L |

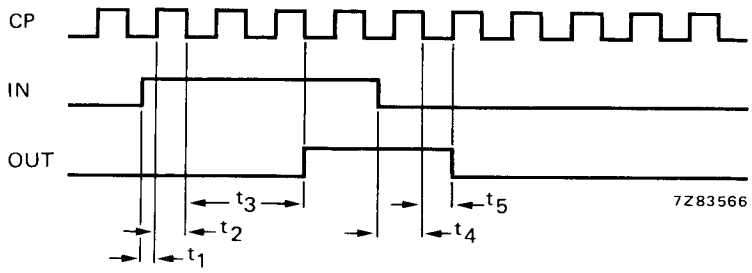
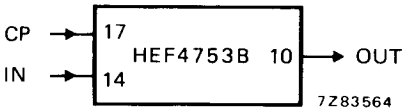




Fig. 5 Timing diagram for delayed LOW to HIGH edge mode; $t_1$ = delay until set of 8-bit counter; $t_2$ = delay to set 8-bit counter; $t_3$ = predefined delay by programming; $t_4$ = delay until next negative clock edge; $t_5$ = delay until next positive clock edge.

**4. Delayed HIGH to LOW edge mode; see note 2** (LFC = HIGH; Y = LOW; Z = HIGH)

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | L | H | H | H | H | H | H | L | L | H | L | H |



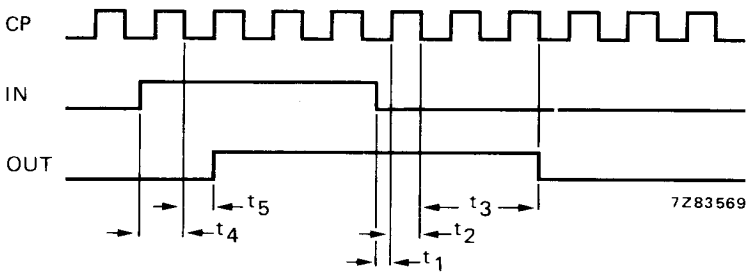




Fig. 6 Timing diagram for delayed HIGH to LOW edge mode; for $t_1$ to $t_5$ see Fig. 5.

**5. Transient pulse suppression and pulse delaying mode; see note 2** (LFC = Y = Z = HIGH)

In this mode the circuit is working as a digital low-pass filter. An undisturbed pulse will only be delayed (see Fig. 7).

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | H | H | H | H | H | H | L | L | H | H | H |

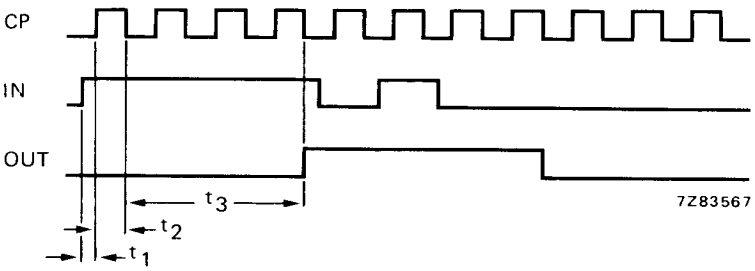



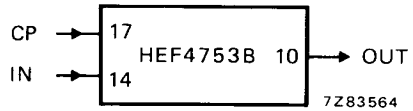

Fig. 7 Timing diagram for transient pulse suppression and pulse delaying mode; for $t_1$, $t_2$ and $t_3$ see Fig. 5.

**OPERATING MODES** (continued)

**6. Frequency recognition mode** (LFC = LOW; Y = HIGH; Z = HIGH)

The incoming signal must be symmetrical within the limits as given by the specified delay time in note 2, to achieve lower or higher frequency detection (see Fig. 8).

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | H | L | H | H | H | H | H | L | L | L | H | H |




Minimum dividing number is 3.

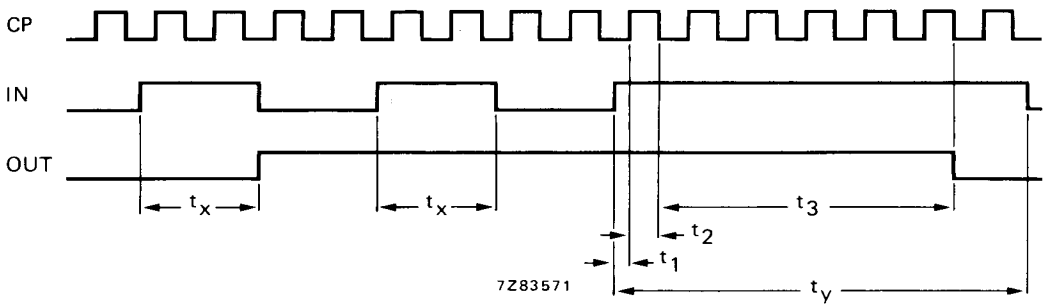


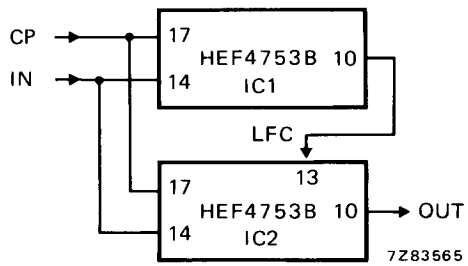

Fig. 8 Timing diagram for frequency recognition mode; $t_x$ = time shorter than $t_3$ (OUT = H); $t_y$ = time greater than $t_3$ (OUT = L); for $t_1$, $t_2$ and $t_3$ see Fig. 5.

**7. Digital pulse duration selector mode** (Y = Z = LOW)

This mode is a combination of two circuits, both used for frequency recognition. Both circuits are driven by the same clock and same input signal, but programmed for different frequencies. The LFC input of the low-frequency circuit is set to logic LOW, the output is connected to the LFC input of the high-frequency circuit, whose output (OUT) is the 'filter' output. The delay time depends on the same facts as given in note 2. For timing diagram see Fig. 9.

| A | B | C | D | E | F | G | H | W | X | LFC | Y | Z | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | L | H | H | H | H | H | L | L | L | H | H | IC1 |
| L | L | H | H | H | H | H | H | L | L | OUT (IC1) | L | L | IC2 |

Minimum dividing number is 3.



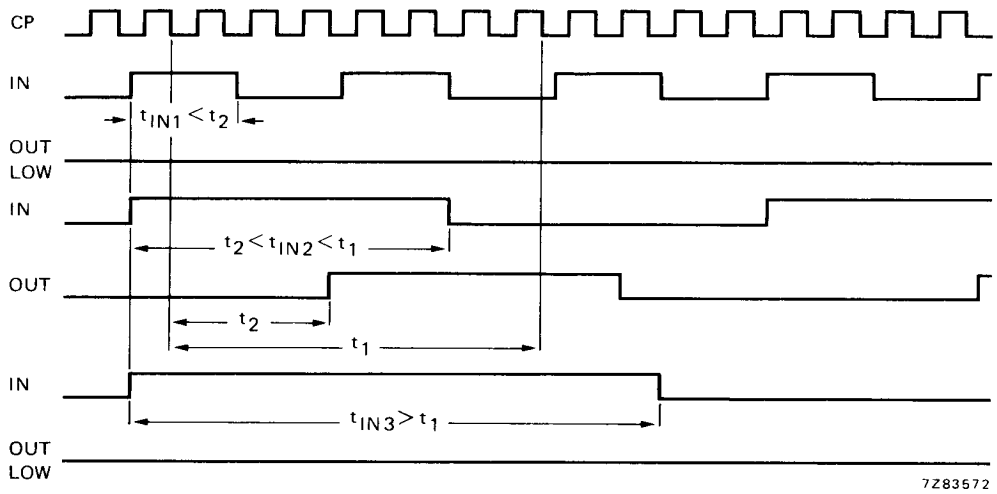



Fig. 9 Timing diagram for digital pulse duration selector mode; $t_{IN1}$, $t_{IN2}$ and $t_{IN3}$ are the IN input pulse durations; $t_1$ = predefined delay by programming IC1; $t_2$ = predefined delay by programming IC2.

**Notes to operating modes**

1. The number of clocks for one cycle in the counter and divider mode is:
   a. Contents of programmable counter plus one if X = W = LOW.
   b. Contents of programmable counter multiplied by 16, 256 or 4096 if X and/or W = HIGH.
2. The delay in the modes 3, 4, 6 and 7, and the delay which is identical to the maximum duration of the transient pulse in mode 5 depend on the optional divided clock frequency, the input conditions of the 8-bit presetable counter and in addition, different times of propagation delays, jitter and maximum one half of a clock frequency period.

## D.C. CHARACTERISTICS

$V_{SS}$ = 0 V

| | $V_{DD}$ V | $V_{OH}$ V | $V_{OL}$ V | symbol | $T_{amb}$ (°C) −40 min. | −40 max. | +25 min. | +25 max. | +85 min. | +85 max. | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Output (sink) | 4,75 | | 0,4 | | 2,7 | – | 2,3 | – | 1,8 | – | mA |
| current LOW | 10 | | 0,5 | $I_{OL}$ | 9,5 | – | 8,0 | – | 6,3 | – | mA |
| (pin 10) | 15 | | 1,5 | | 24,0 | – | 20,0 | – | 16,0 | – | mA |
| Output (source) | 5 | 4,6 | | | 0,6 | – | 0,5 | – | 0,4 | – | mA |
| current HIGH | 10 | 9,5 | | $-I_{OH}$ | 1,8 | – | 1,5 | – | 1,2 | – | mA |
| (pin 10) | 15 | 13,5 | | | 6,0 | – | 5,0 | – | 4,0 | – | mA |

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ⩽ 20 ns

| | $V_{DD}$ V | symbol | min. | typ. | max. | | typical extrapolation formula |
|---|---|---|---|---|---|---|---|
| Propagation delays | 5 | | | 420 | 850 | ns | |
| CP ⟶ OUT | 10 | $t_{PHL}$ | | 180 | 360 | ns | |
| HIGH to LOW | 15 | | | 120 | 250 | ns | |
| | 5 | | | 450 | 900 | ns | |
| LOW to HIGH | 10 | $t_{PLH}$ | | 200 | 400 | ns | |
| | 15 | | | 140 | 280 | ns | |
| Output transition | 5 | | | 30 | 60 | ns | |
| times | 10 | $t_{THL}$ | | 15 | 30 | ns | |
| HIGH to LOW | 15 | | | 10 | 20 | ns | |
| | 5 | | | 60 | 120 | ns | |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | |
| | 15 | | | 20 | 40 | ns | |
| Input rise and | 5 | | | | | | |
| fall times | 10 | $t_r, t_f$ | no limit | | | | |
| pins 13, 14, 17 | 15 | | | | | | |
| Maximum clock | 5 | | 3 | 6 | | MHz | |
| pulse frequency | 10 | $f_{max}$ | 7 | 14 | | MHz | |
| pin 17; δ = 50% | 15 | | 8 | 17 | | MHz | |

| | $V_{DD}$ V | typical formula for P (μW) | where |
|---|---|---|---|
| Dynamic power dissipation per package (P) | 5 | $1\,800\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$ | $f_i$ = input freq. (MHz) |
| | 10 | $8\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$ | $f_o$ = output freq. (MHz) |
| | 15 | $19\,000\ f_i + \Sigma\ (f_o C_L) \times V_{DD}^2$ | $C_L$ = load capacitance (pF) |
| | | | $\Sigma\ (f_o C_L)$ = sum of outputs |
| | | | $V_{DD}$ = supply voltage (V) |