



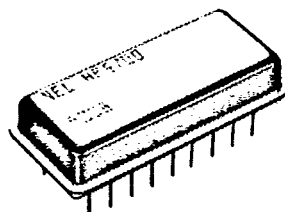
Programmable Clock Generator

T-50-23

HF-5700 Series

781.25 kHz -

200.0 MHz



Description

The HF-5700 Series is designed to enhance the operating performance of the National Semiconductor (NSC) DP8531 IC, in those requirements where jitter and RFI are a critical consideration. This clock generator is intended to supply a number of synchronized clock signals for a wide range of applications, including graphics, fiber optics, LAN and disk drives.

This device incorporates the NSC DP8531 programmable clock generator IC, with a proprietary NEL Frequency Controls, Inc. ASIC TTL/CMOS clock oscillator, a quartz crystal and loop filter, designed into a single 18 pin DIP package. The outputs of the device are generated from the internal crystal controlled clock oscillator, and provide programmable pixel (PCLK) and systems clocks (SCLK, LCLK and GCLK) as required by the user, based on the digital control lines.

- Special attention is given to construction and layout, to minimize jitter and RFI.
- Peak-Peak phase jitter less than 1 nanosecond under worst case conditions.
- Pixel clock output frequency up to 200 MHz.

Suggested Applications

- ☐ Computer Graphics
- ☐ Disk Drives — constant density recording
- ☐ Fiber Optics
- ☐ LAN Requirements

Clock Functions

PIXEL CLOCK

- ☐ PCLK — ECL 10 K and 100K compatible
- ☐ PCLK — ECL complementary output (range 781.25 kHz - 200.0 MHz, both outputs)
- ☐ PCLK — TTL compatible (80.0 MHz maximum)

SYSTEMS CLOCKS

- ☐ SCLK — TTL clock to drive graphics processor clock input.
- ☐ LCLK — TTL compatible non-gated load clock to drive external devices.
- ☐ GCLK — same as LCLK, except with delayed phase transitions.

Specifications

PARAMETER	CONDITION	MINIMUM	TYPICAL	MAXIMUM
Supply Voltage (V _{cc})		4.75	5	5.25
OSC V _{cc} , Volts				
Supply Current, mA	No Load		140	
Frequency Crystal, OSC, MHz				20.000 (18-40 MHz optional)
Tolerance	25°C	±.005%		
Stability		±.01%		
Operating Temperature Range		0°C		70°C
P Clock				
TTL Compatible		781.25KHz		80MHz
P Clock		781.25KHz		200MHz
ECL Compatible				
Resolution				.25%
L Clock Frequency		3.052KHz		200MHz



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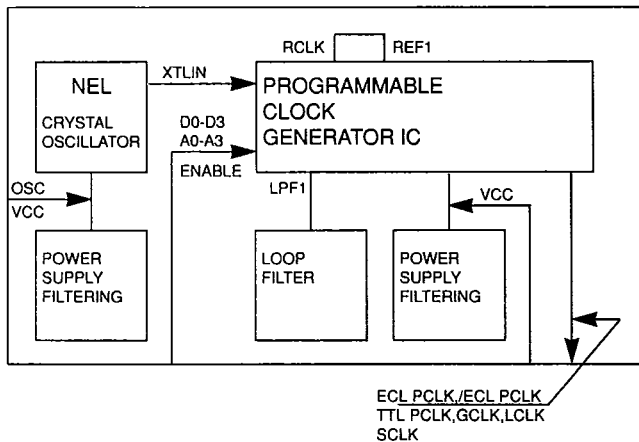
200.0 MHz

Features

- Low phase jitter
- Case at electrical ground
- Simplified design and board layout (see block diagram)

- ☐ High reliability
- ☐ All metal resistance weld hermetically sealed package
- ☐ High shock resistance to 3000 G's
- ☐ RFI shielding

Functional Block Diagram

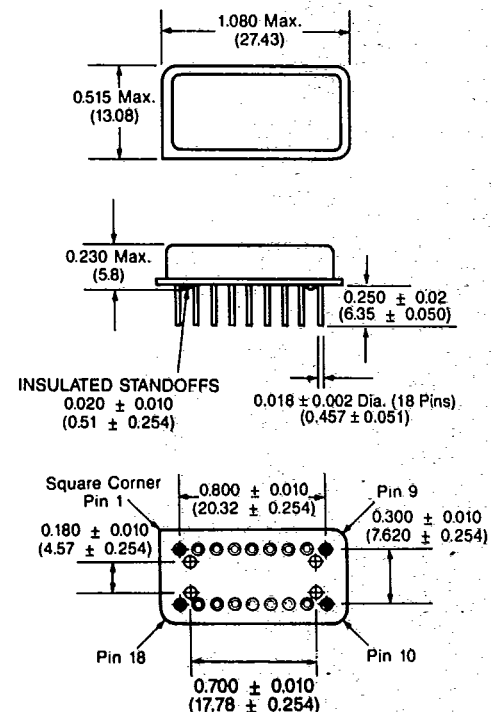


Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
TTL Signals	
Inputs	7V
Outputs	7V
ECL Signals	
Output Current	-50 mA
Supplies (V _{CC} to Ground)	-0.5V to +7V
ESD Susceptibility	500v

Pin Out

Pin #	Signal
1	Ground & Case
2	ECL PCLK
3	/ECL PCLK
4	TTL PCLK
5	GCLK
6	LCLK
7	SCLK
8	D0
9	D1
10	V _{CC} (+5V)
11	D2
12	D3
13	A0
14	A1
15	A2
16	A3
17	ENABLE
18	OSCILLATOR V _{CC} (+5V)



This information is believed to be reliable at the time of printing; no responsibility is assumed for inaccuracies. NEL Frequency Controls reserves the right to make changes at any time.

Dimensions are for reference only, inches (mm).