

850MHz, Low Distortion Current Feedback Operational Amplifiers

The HFA1100, 1120 are a family of high-speed, wideband, fast settling current feedback amplifiers. Built with Harris' proprietary complementary bipolar UHF-1 process, these devices are the fastest monolithic amplifiers available from any semiconductor manufacturer.

The HFA1100 is a basic op amp with uncommitted pins 1, 5, and 8. The HFA1120 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

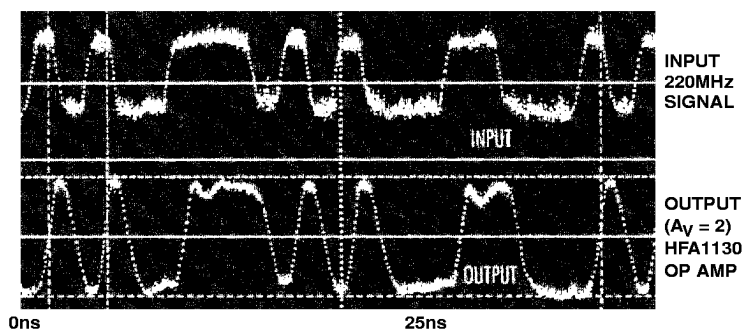
These devices offer a significant performance improvement over the AD811, AD9617/18, the CLC400-409, and the EL2070, EL2073, EL2030.

For Military grade product refer to the HFA1100/883, HFA1120/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA1100IP	-40 to 85	8 Ld PDIP	E8.3
HFA1100IB (H1100I)	-40 to 85	8 Ld SOIC	M8.15
HFA1120IB (H1120I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board for High-Speed Op Amps		

The Op Amps With Fastest Edges



Features

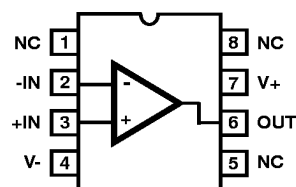
- Low Distortion (30MHz, HD2) -56dBc
- -3dB Bandwidth 850MHz
- Very Fast Slew Rate 2300V/ μ s
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
 - (100MHz) ± 0.14 dB
 - (50MHz) ± 0.04 dB
 - (30MHz) ± 0.01 dB
- High Output Current 60mA
- Overdrive Recovery <10ns

Applications

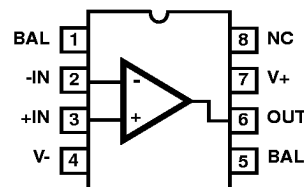
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems
- Related Literature
 - AN9420, Current Feedback Theory
 - AN9202, HFA11XX Evaluation Fixture

Pinouts

HFA1100
(PDIP, SOIC)
TOP VIEW



HFA1120
(SOIC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^{\circ}\text{C}$

Voltage Between V_+ and V_- 12V
 Input Voltage V_{SUPPLY}
 Differential Input Voltage 5V
 Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^{\circ}\text{C}/\text{W}$) θ_{JC} ($^{\circ}\text{C}/\text{W}$)
 PDIP Package 130 N/A
 SOIC Package 170 N/A
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC - Lead Tips Only)

Electrical Specifications $V_{\text{SUPPLY}} = \pm 5\text{V}$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. ($^{\circ}\text{C}$)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (Note 3)		A	25	-	2	6	mV
		A	Full	-	-	10	mV
Input Offset Voltage Drift		C	Full	-	10	-	$\mu\text{V}/^{\circ}\text{C}$
V_{IO} CMRR	$\Delta V_{CM} = \pm 2\text{V}$	A	25	40	46	-	dB
		A	Full	38	-	-	dB
V_{IO} PSRR	$\Delta V_S = \pm 1.25\text{V}$	A	25	45	50	-	dB
		A	Full	42	-	-	dB
Non-Inverting Input Bias Current (Note 3)	$+I_N = 0\text{V}$	A	25	-	25	40	μA
		A	Full	-	-	65	μA
$+I_{BIAS}$ Drift		C	Full	-	40	-	$\text{nA}/^{\circ}\text{C}$
$+I_{BIAS}$ CMS	$\Delta V_{CM} = \pm 2\text{V}$	A	25	-	20	40	$\mu\text{A}/\text{V}$
		A	Full	-	-	50	$\mu\text{A}/\text{V}$
Inverting Input Bias Current (Note 3)	$-I_N = 0\text{V}$	A	25	-	12	50	μA
		A	Full	-	-	60	μA
$-I_{BIAS}$ Drift		C	Full	-	40	-	$\text{nA}/^{\circ}\text{C}$
$-I_{BIAS}$ CMS	$\Delta V_{CM} = \pm 2\text{V}$	A	25	-	1	7	$\mu\text{A}/\text{V}$
		A	Full	-	-	10	$\mu\text{A}/\text{V}$
$-I_{BIAS}$ PSS	$\Delta V_S = \pm 1.25\text{V}$	A	25	-	6	15	$\mu\text{A}/\text{V}$
		A	Full	-	-	27	$\mu\text{A}/\text{V}$
$-I_{BIAS}$ Adj. Range (HFA1120)		A	25	± 100	± 200	-	μA
Non-Inverting Input Resistance		A	25	25	50	-	$\text{k}\Omega$
Inverting Input Resistance		C	25	-	20	30	Ω
Input Capacitance (Either Input)		B	25	-	2	-	pF
Input Common Mode Range		C	Full	± 2.5	± 3.0	-	V
Input Noise Voltage (Note 3)	100kHz	B	25	-	4	-	$\text{nV}/\sqrt{\text{Hz}}$
$+I_{\text{Input Noise Current}}$ (Note 3)	100kHz	B	25	-	18	-	$\text{pA}/\sqrt{\text{Hz}}$
$-I_{\text{Input Noise Current}}$ (Note 3)	100kHz	B	25	-	21	-	$\text{pA}/\sqrt{\text{Hz}}$

HFA1100, HFA1120

Electrical Specifications $V_{\text{SUPPLY}} = \pm 5\text{V}$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified							
Open Loop Transimpedance (Note 3)		B	25	-	300	-	k Ω
-3dB Bandwidth (Note 3)	$V_{\text{OUT}} = 0.2V_{\text{P-P}}$, $A_V = +1$	B	25	530	850	-	MHz
-3dB Bandwidth	$V_{\text{OUT}} = 0.2V_{\text{P-P}}$, $A_V = +2$, $R_F = 360\Omega$	B	25	-	670	-	MHz
Full Power Bandwidth	$V_{\text{OUT}} = 4V_{\text{P-P}}$, $A_V = -1$	B	25	-	300	-	MHz
Gain Flatness (Note 3)	To 100MHz	B	25	-	± 0.14	-	dB
Gain Flatness	To 50MHz	B	25	-	± 0.04	-	dB
Gain Flatness	To 30MHz	B	25	-	± 0.01	-	dB
Linear Phase Deviation (Note 3)	DC to 100MHz	B	25	-	0.6	-	Degrees
Differential Gain	NTSC, $R_L = 75\Omega$	B	25	-	0.03	-	%
Differential Phase	NTSC, $R_L = 75\Omega$	B	25	-	0.05	-	Degrees
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified							
Output Voltage (Note 3)	$A_V = -1$	A	25	± 3.0	± 3.3	-	V
		A	Full	± 2.5	± 3.0	-	V
Output Current	$R_L = 50\Omega$, $A_V = -1$	A	25, 85	50	60	-	mA
		A	-40	35	50	-	mA
DC Closed Loop Output Impedance (Note 3)		B	25	-	0.07	-	Ω
2nd Harmonic Distortion (Note 3)	30MHz, $V_{\text{OUT}} = 2V_{\text{P-P}}$	B	25	-	-56	-	dBc
3rd Harmonic Distortion (Note 3)	30MHz, $V_{\text{OUT}} = 2V_{\text{P-P}}$	B	25	-	-80	-	dBc
3rd Order Intercept (Note 3)	100MHz	B	25	20	30	-	dBm
1dB Compression	100MHz	B	25	15	20	-	dBm
TRANSIENT RESPONSE $A_V = +2$, Unless Otherwise Specified							
Rise Time	$V_{\text{OUT}} = 2.0\text{V Step}$	B	25	-	900	-	ps
Overshoot (Note 3)	$V_{\text{OUT}} = 2.0\text{V Step}$	B	25	-	10	-	%
Slew Rate	$A_V = +1$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	B	25	-	1400	-	V/ μs
Slew Rate	$A_V = +2$, $V_{\text{OUT}} = 5V_{\text{P-P}}$	B	25	1850	2300	-	V/ μs
0.1% Settling (Note 3)	$V_{\text{OUT}} = 2\text{V to } 0\text{V}$	B	25	-	11	-	ns
0.2% Settling (Note 3)	$V_{\text{OUT}} = 2\text{V to } 0\text{V}$	B	25	-	7	-	ns
Overdrive Recovery Time	2X Overdrive	B	25	-	7.5	10	ns
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		B	Full	± 4.5	-	± 5.5	V
Supply Current (Note 3)		A	25	-	21	26	mA
		A	Full	-	-	33	mA

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
3. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor (R_F)

The enclosed plots of inverting and non-inverting frequency response detail the performance of the HFA1100/1120 in various gains. Although the bandwidth dependency on A_{CL} isn't as severe as that of a voltage feedback amplifier, there is an appreciable decrease in bandwidth at higher gains. This decrease can be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F . All current feedback amplifiers require a feedback resistor, even for unity gain applications, and the R_F , in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F . The HFA1100, 1120 designs are optimized for a 510 Ω R_F , at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth. The table below lists recommended R_F values for various gains, and the expected bandwidth.

A_{CL}	R_F (Ω)	BW (MHz)
+1	510	850
-1	430	580
+2	360	670
+5	150	520
+10	180	240
+19	270	125

Offset Adjustment

The HFA1120 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F , so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F . With $R_F = 510\Omega$, the typical adjust range is $\pm 100\text{mV}$. For offset adjustment connect a 10k Ω potentiometer between pins 1 and 5 with the wiper connected to V_- .

Use of Die in Hybrid Applications

These amplifiers are designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For $A_V = +2$ the recommended starting point is 300 Ω , while unity gain applications should try 400 Ω .

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC

board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!

Attention should be given to decoupling the power supplies. A large value (10 μF) tantalum in parallel with a small value chip (0.1 μF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

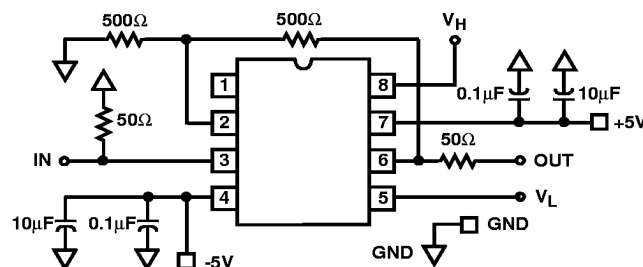
Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown below.

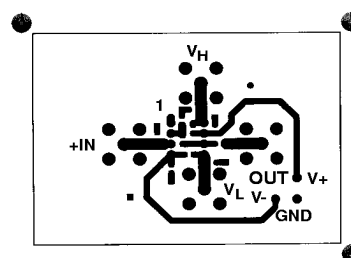
Evaluation Board

An evaluation board is available for the HFA1100 (Part Number HFA11XXEVAL). Please contact your local sales office for information.

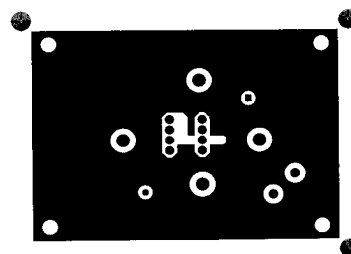
The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT



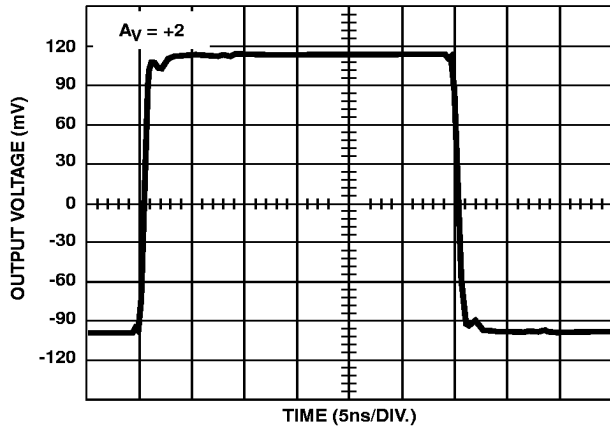
Typical Performance Curves $V_{\text{SUPPLY}} = \pm 5\text{V}$, $R_F = 510\Omega$, $T_A = 25^\circ\text{C}$, $R_L = 100\Omega$, Unless Otherwise Specified


FIGURE 1. SMALL SIGNAL PULSE

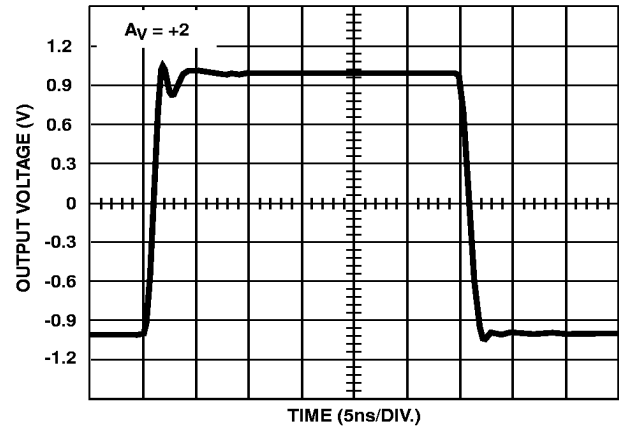


FIGURE 2. LARGE SIGNAL PULSE

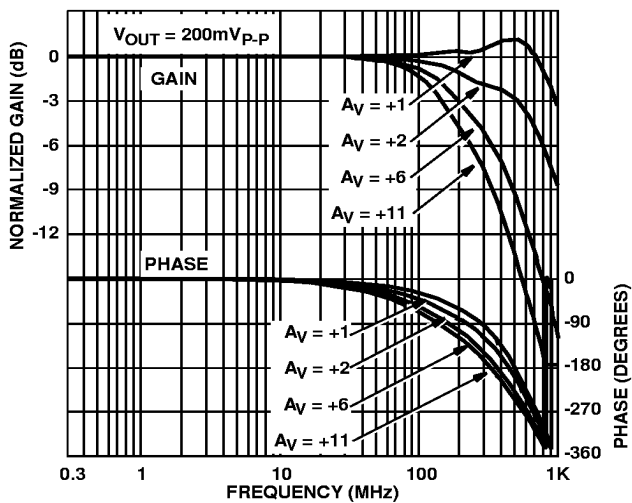


FIGURE 3. NON-INVERTING FREQUENCY RESPONSE

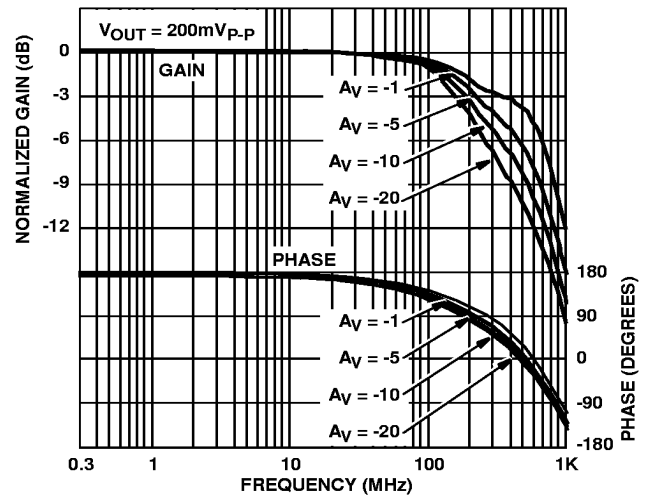


FIGURE 4. INVERTING FREQUENCY RESPONSE

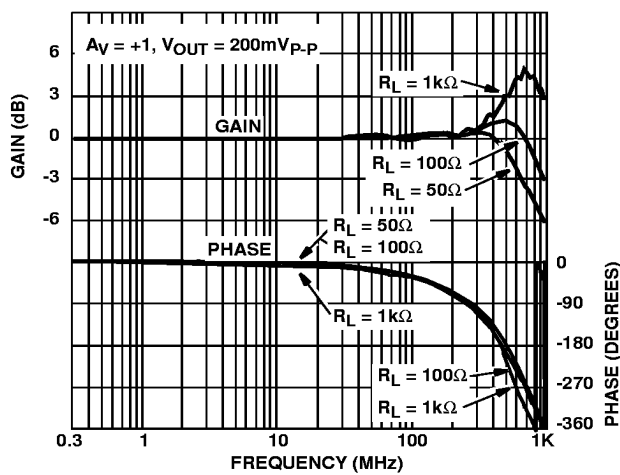


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

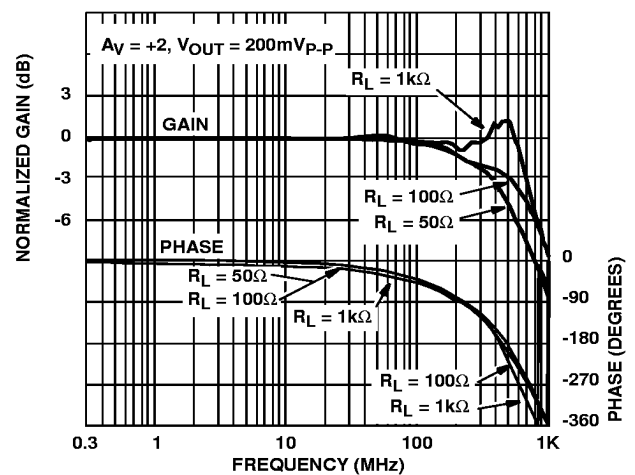


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

Typical Performance Curves $V_{\text{SUPPLY}} = \pm 5\text{V}$, $R_F = 510\Omega$, $T_A = 25^\circ\text{C}$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

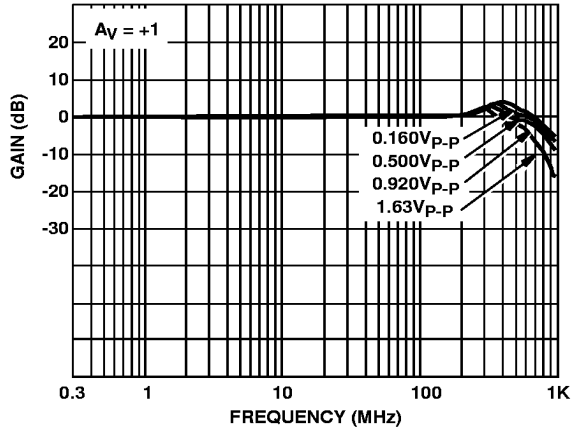


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

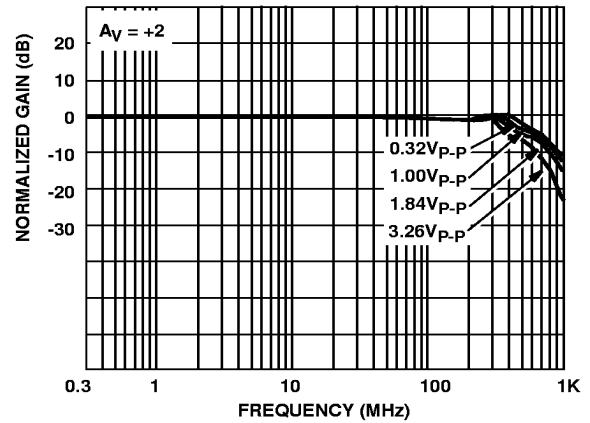


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

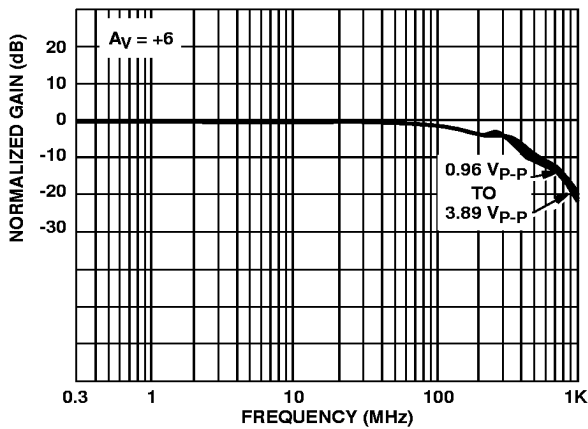


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

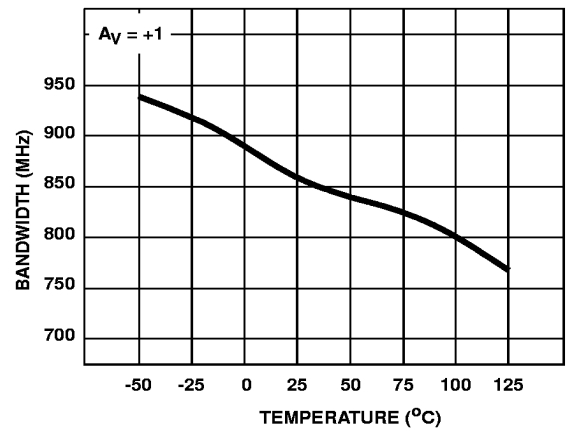


FIGURE 10. -3dB BANDWIDTH vs TEMPERATURE

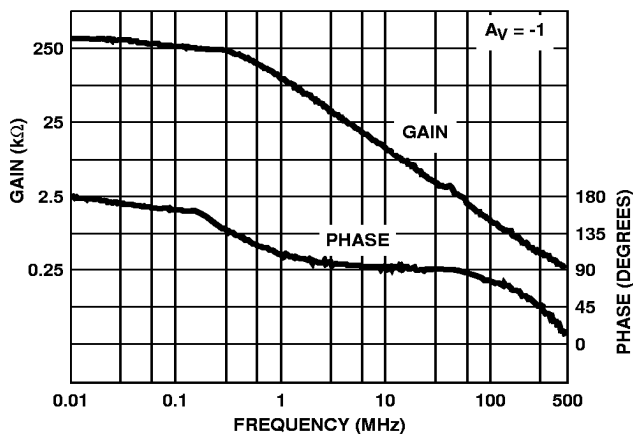


FIGURE 11. OPEN LOOP TRANSIMPEDANCE

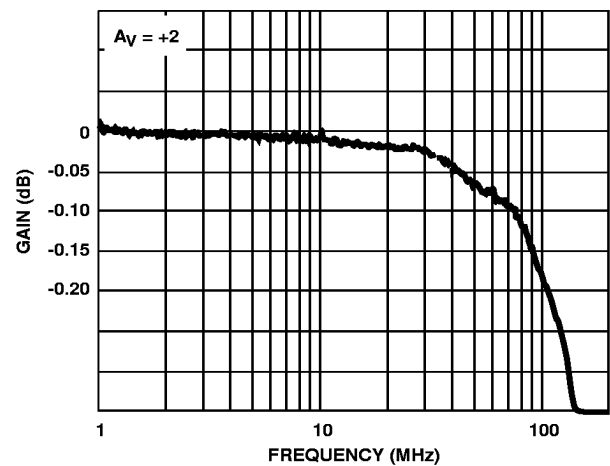


FIGURE 12. GAIN FLATNESS

Typical Performance Curves $V_{\text{SUPPLY}} = \pm 5\text{V}$, $R_F = 510\Omega$, $T_A = 25^\circ\text{C}$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

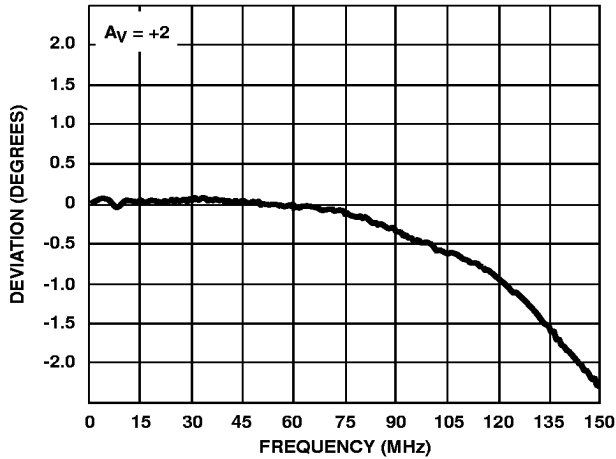


FIGURE 13. DEVIATION FROM LINEAR PHASE

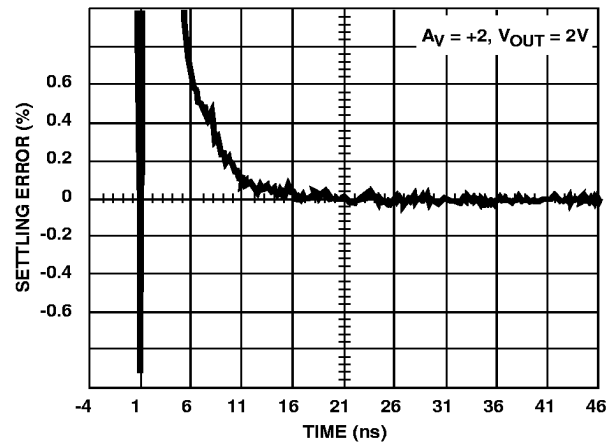


FIGURE 14. SETTLING RESPONSE

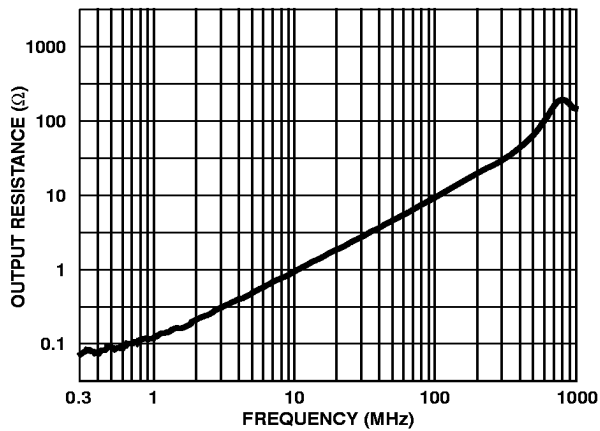


FIGURE 15. CLOSED LOOP OUTPUT RESISTANCE

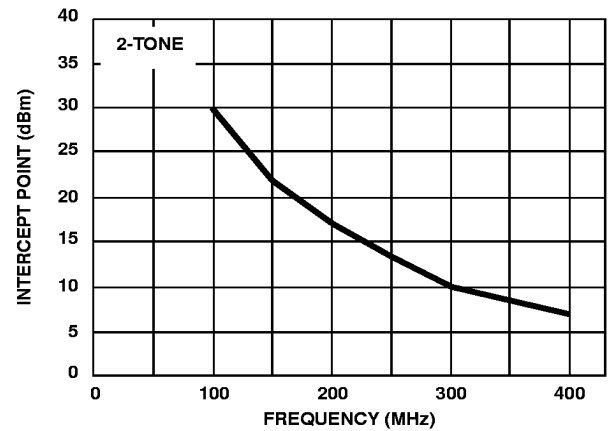


FIGURE 16. 3rd ORDER INTERMODULATION INTERCEPT

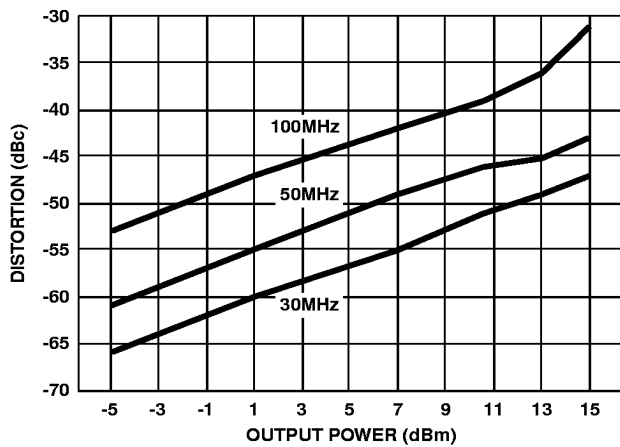


FIGURE 17. 2nd HARMONIC DISTORTION vs P_{OUT}

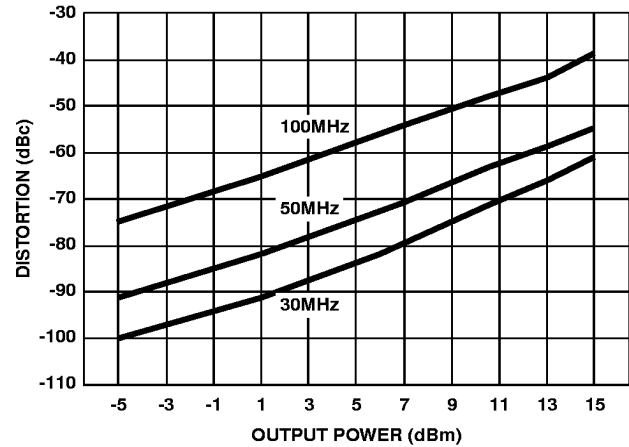


FIGURE 18. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{\text{SUPPLY}} = \pm 5\text{V}$, $R_F = 510\Omega$, $T_A = 25^\circ\text{C}$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

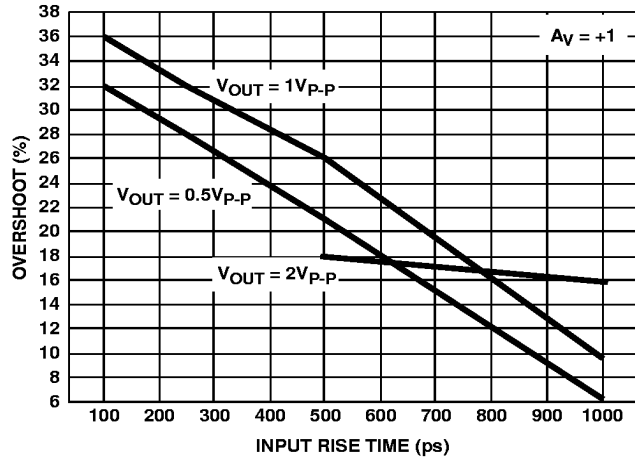


FIGURE 19. OVERSHOOT vs INPUT RISE TIME

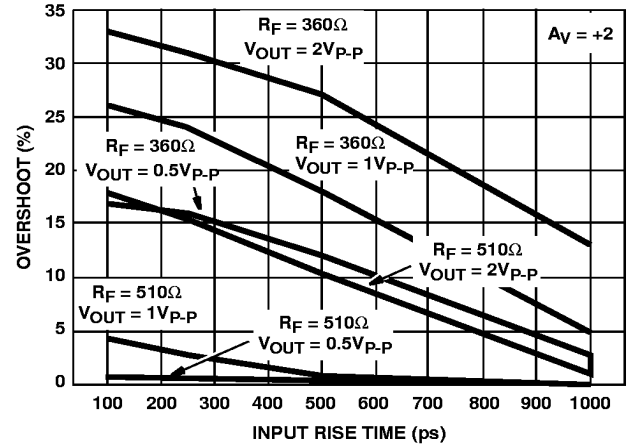


FIGURE 20. OVERSHOOT vs INPUT RISE TIME

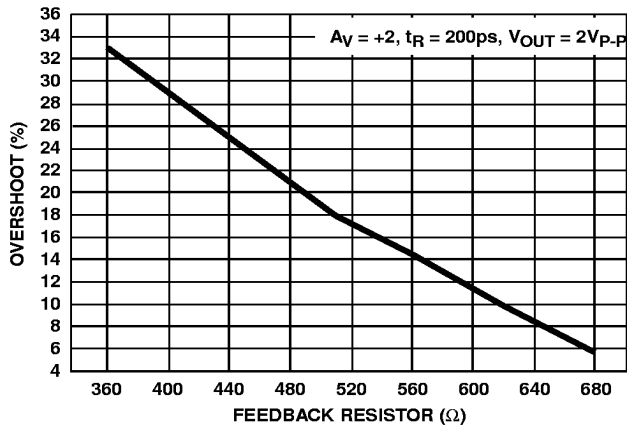


FIGURE 21. OVERSHOOT vs FEEDBACK RESISTOR

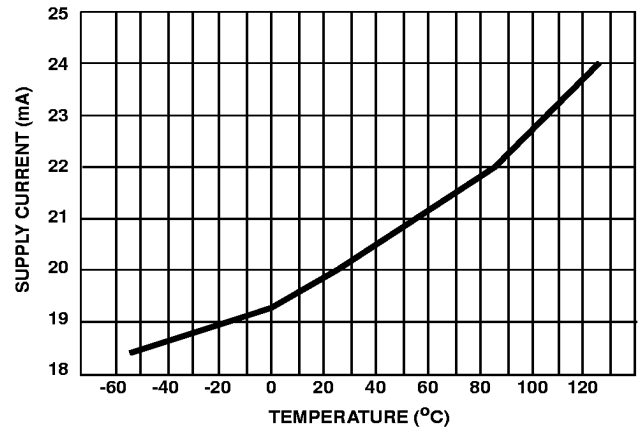


FIGURE 22. SUPPLY CURRENT vs TEMPERATURE

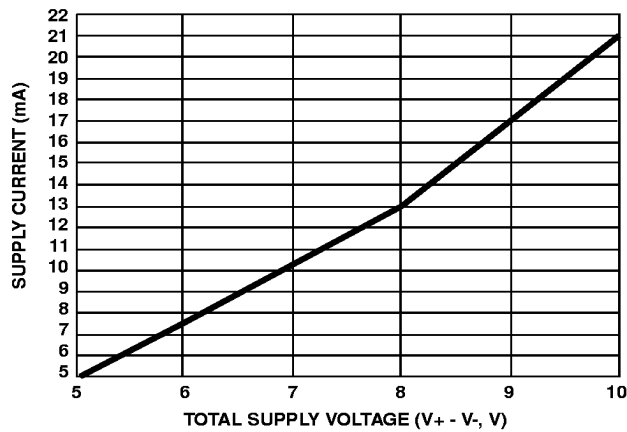


FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

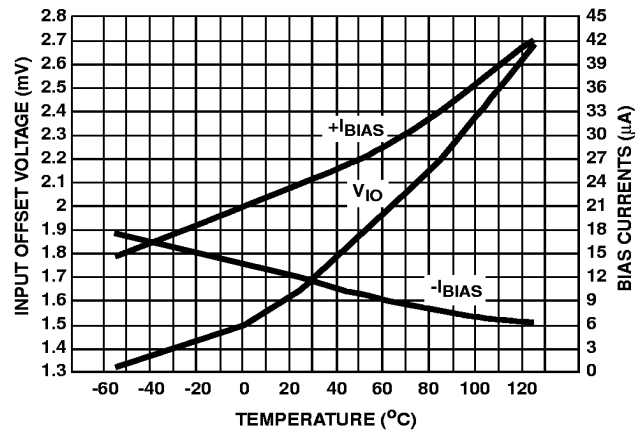


FIGURE 24. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $T_A = 25^\circ C$, $R_L = 100\Omega$, Unless Otherwise Specified (Continued)

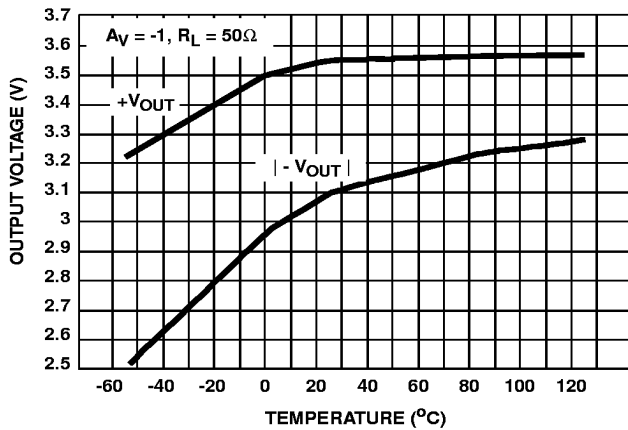


FIGURE 25. OUTPUT VOLTAGE vs TEMPERATURE

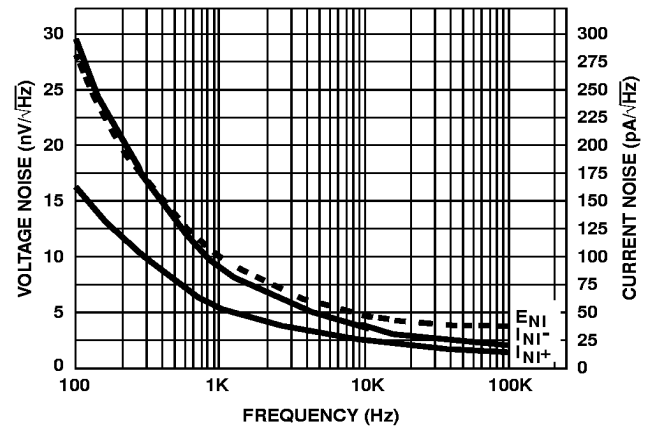


FIGURE 26. INPUT NOISE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600 μ m x 1130 μ m

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8k $\text{\AA}$ $\pm$ 0.4k $\text{\AA}$
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16k $\text{\AA}$ $\pm$ 0.8k $\text{\AA}$

PASSIVATION:

Type: Nitride
Thickness: 4k $\text{\AA}$ $\pm$ 0.5k $\text{\AA}$

TRANSISTOR COUNT:

52

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

Metallization Mask Layout

