HARRIS SEMICONDUCTOR

HFA1103

200MHz, Video Op Amp with High Speed Sync Stripper

November 1996

Features

- **Removes Sync Signal From Component Video**
- **Low Residual Sync . . . . . 8mV (Typ)**
- **-3dB Bandwidth 200MHz**
- **Very Fast Slew Rate 600V/μs**
- **Fast Settling Time (0.1%) 9ns**
- **Excellent Gain Flatness, 32MHz . . . . . ±0.1dB**
- **Overdrive Recovery . . . . . <12ns**

Applications

- **RGB Video Sync Stripping**
- **RGB Video Distribution Amplifier for Workstations and PC Networks**
- **Video Conferencing Systems**
- **RGB Video Monitor Preamp**
- **Fiberoptic Receivers**

Description

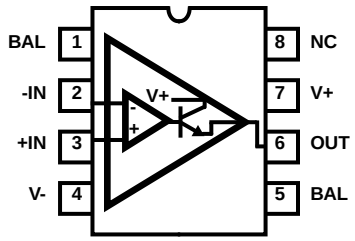
The HFA1103 is a high-speed, wideband, fast settling current feedback op amp with a sync stripping function. The HFA1103 is a basic op amp with a modified output stage that enables it to strip the sync from a component video signal. The output stage has an open emitter NPN transistor that prevents the output from going low during the sync pulse. Removing the sync signal benefits digitizing systems because only the active video information is applied to the A/D converter. This enables the full dynamic range of the A/D converter to be used to process the video signal. The HFA1103 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

Ordering Information

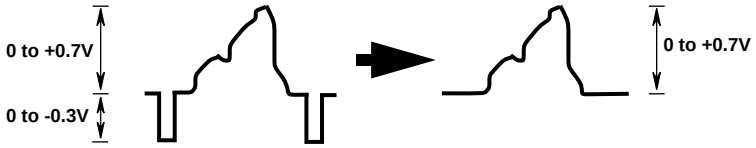
PART NUMBER (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HFA1103IP	-40 to 85	8 Ld PDIP	E8.3
HFA1103IB (H1103I)	-40 to 85	8 Ld SOIC	M8.15

Pinout

HFA1103
(PDIP, SOIC)
TOP VIEW



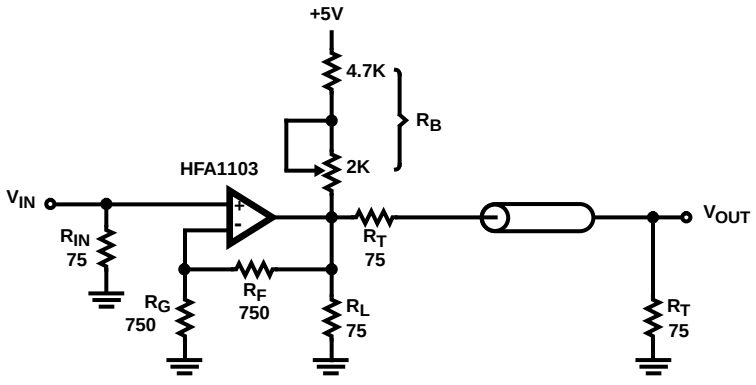
Sync Stripper Waveforms



COMPONENT (RGB) VIDEO INPUT

HFA1103 OUTPUT

Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3957.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Differential Input Voltage. 5V
Output Current (50% Duty Cycle). 60mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	130
SOIC Package	170

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +2$, $R_F = 750\Omega$, $R_L = 50\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Residual Sync (Note 2)	V_{IN} = -300mV, A_V = +1	25	-	8	10	mV
		Full	-	-	12	mV
Output Offset Voltage (Notes 3, 5)		25	-	10	30	mV
		Full	-	-	40	mV
Output Offset Voltage Drift (Note 3)		Full	-	10	-	$\mu V/^oC$
V_{OS} PSRR	$\Delta V_S = \pm1.25V$	25	39	45	-	dB
		Full	35	-	-	dB
Non-Inverting Input Bias Current	+IN = 0V	25	-	5	40	µA
		Full	-	-	65	µA
Inverting Input Bias Current	-IN = 0V	25	-	5	50	µA
		Full	-	-	60	µA
$-I_{BIAS}$ Adjust Range (Notes 4, 6)		25	100	200	-	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance		25	-	16	30	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±3.0	-	V
Input Noise Voltage	100kHz	25	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current	100kHz	25	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current	100kHz	25	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS A_V = +2, Unless Otherwise Specified						
Open Loop Transimpedance		25	-	500	-	kΩ
-3dB Bandwidth	$V_{OUT} = 1.0V_{P-P}$, A_V = +2	25	-	200	-	MHz
Gain Flatness	To ±0.1dB	25	-	32	-	MHz
Minimum Stable Gain		Full	1	-	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified						
Output Voltage (Note 3)		25, 85	2.5	3.0	-	V
		-40^oC	1.75	2.5	-	V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +2$, $R_F = 750\Omega$, $R_L = 50\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN	TYP	MAX	UNITS
Output Current		25, 85	50	60	-	mA
		-40^oC	35	50	-	mA
Linearity Near Zero		25	-	0.01	-	%
TRANSIENT RESPONSE $A_V = +2$, Unless Otherwise Specified						
Rise Time	$V_{OUT} = 2.0V$ Step	25	-	2	-	ns
Overshoot	$V_{OUT} = 2.0V$ Step	25	-	10	-	%
Slew Rate	$A_V = +2$, $V_{OUT} = 0$ to 2V, +2V to 0V	25	-	600	-	V/µs
0.1% Settling	$V_{OUT} = 2V$ to 0V	25	-	9	-	ns
Overdrive Recovery Time	2X Overdrive	25	-	12	-	ns
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current (No Load)		25	-	11	16	mA
		Full	-	-	23	mA

NOTES:

2. The residual sync is specified at the output of a doubly terminated circuit (see page 1 of this data sheet).
3. Since the HFA1103 has an open emitter NPN output stage, this measurement is only valid for positive values.
4. The $-I_{BIAS}$ current can be used to adjust the offset voltage to zero, but $-I_{BIAS}$ does not flow bidirectionally because the HFA1103 output stage is an open emitter NPN transistor.
5. V_{OS} includes the error contribution of I_{BSN} at $R_F = 750\Omega$.
6. This is the minimum change in inverting input bias current when a BAL pin is connected to V- through a 50Ω resistor.

Test Circuit

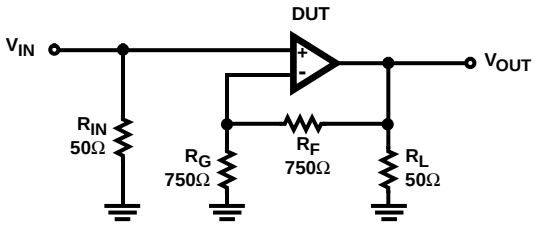


FIGURE 1. TEST CIRCUIT

Application Information

Offset Adjustment

The HFA1103 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F, so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F. With $R_F = 750\Omega$, the typical adjust range is 150mV. For offset adjustment connect a 10kΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Evaluation Board

The HFA1100 series evaluation board may be used for the HFA1103 with minor modifications. The evaluation board may be ordered using part number HFA11XXEVAL. Please note that an HFA1103 sample is not included with the evaluation board and must be ordered separately.

The layout and schematic of the board are shown below:

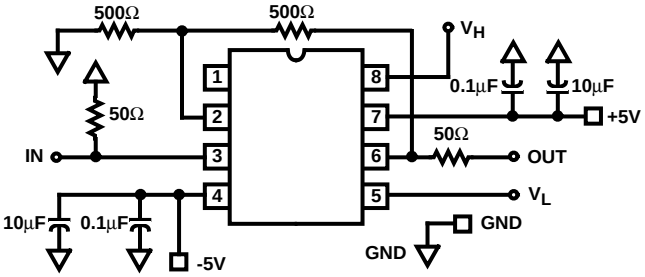
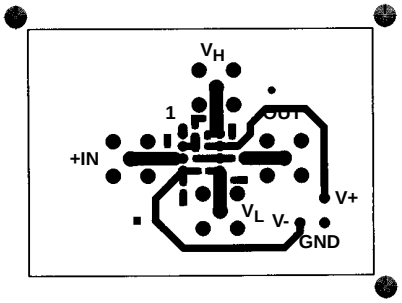


FIGURE 2. EVALUATION BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT

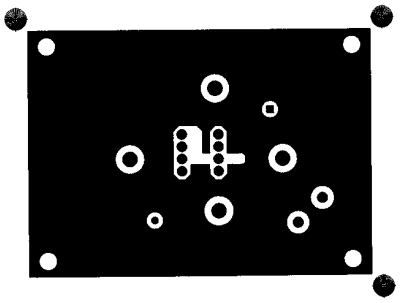


FIGURE 3. EVALUATION BOARD ARTWORK

Typical Application

A circuit which performs the sync stripper and DC restore functions is shown in Figure 4. Please reference Harris Application Note AN9514, titled "Video Amplifier with Sync Stripper and DC Restore", for details on this circuit.

The standard output of a VM700 video measurement set is shown in Figure 5. The output, after passing through the Applications Schematic shown on the first page of this data sheet, is shown in Figure 6.

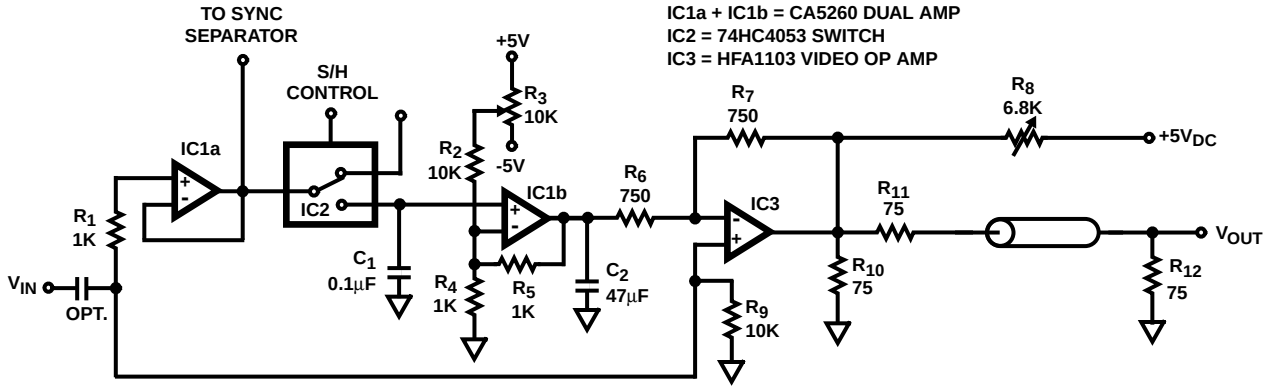


FIGURE 4. VIDEO AMPLIFIER WITH SYNC STRIPPER AND DC RESTORE

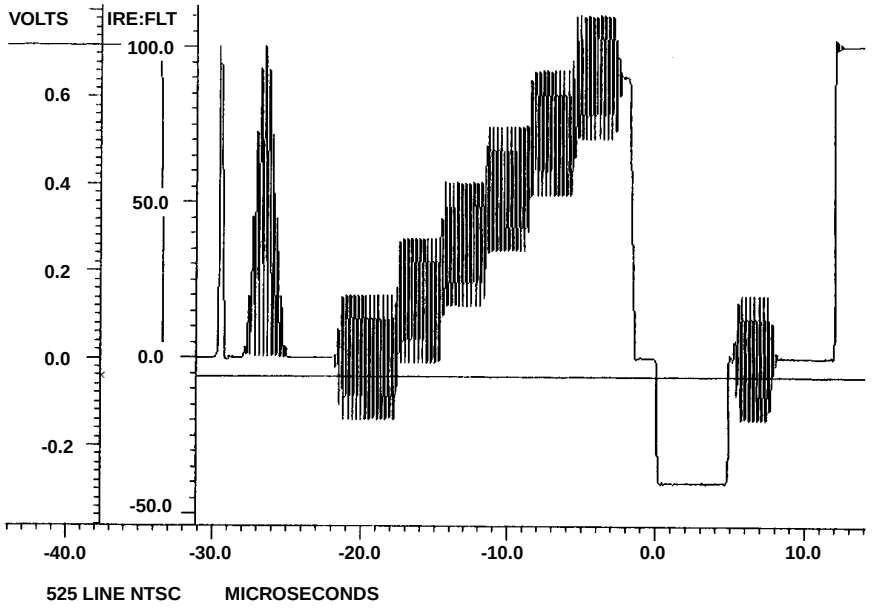


FIGURE 5. OUTPUT OF VM700 VIDEO MEASUREMENT SET

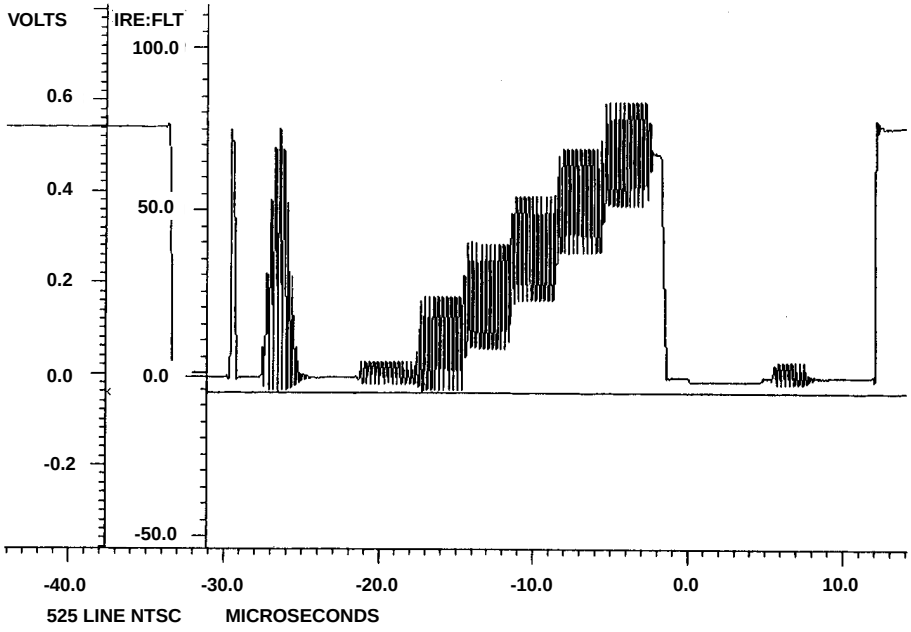


FIGURE 6. OUTPUT OF HFA1103 SYNC STRIPPER CONFIGURED AS ON THE FIRST PAGE OF THIS DATA SHEET

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (2%)
Thickness: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

Floating (Recommend Connection to V-)

PASSIVATION:

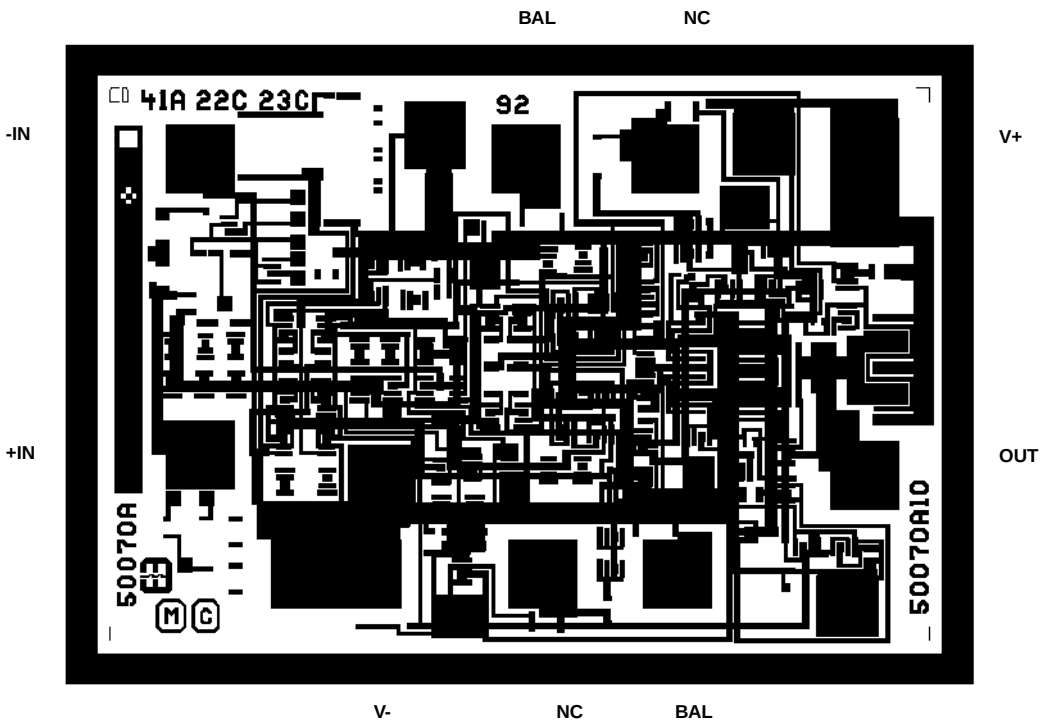
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

50

Metallization Mask Layout

HFA1103



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