# HFD3212

## TTL Output Receiver

### OPERATION

Optical power (photons) from the fiber strikes the photodiode and is converted to electrical current. This current is then converted into a voltage in the transimpedance preamplifier. The postamplifier is a voltage gain stage with excellent temperature tracking. The edge detection circuit includes an operational amplifier configured as a differentiator, whose output is proportional to the rate of change of the optical signal. A latch retains the most recent edge transition and an inverting buffer drives the TTL output. For example, a light On to light Off transition of the input produces a TTL high output logic level.

Bandwidth has been limited to minimize noise problems. Reduced pulse width distortion (PWD) is a by-product of the bandwidth limitation. The output of the differentiator has a fixed settling time, assuring good PWD in most applications. Another effect of fixed settling time is the increase of PWD with increased optical power. Very high input optical power may overdrive the differentiator, causing high PWD due to the settling time. The accompanying curves illustrate how PWD increases with increased optical power, increased temperature, and decreased duty cycle.

PWD manifests itself as an increase in the width of the TTL low portion of an output waveform, with the TTL high portion decreasing by a like amount. The amount of PWD that a given system can tolerate without an error due to a missing bit of information, is dependant upon system considerations. The output of the HFD3212 will typically connect to the input of some form of a Serial Interface Adaptor IC. The specifications for that IC govern the amount of PWD that can be tolerated in that system.

The edge detection circuit monitors the output of the differentiator, and triggers when its output exceeds preset levels. These levels are established to be sufficiently above the worst case RMS noise level to allow excellent bit error rate and are low enough to give high sensitivities which permit operation over long link lengths. This circuitry recognizes the polarity of the change of the optical signal, setting the latch to a "1" when the optical input decreases.

Note: the final output stage inverts the polarity. When initially powered up, the output state is set to a "1". After setting of the device occurs, incoming edge transitions are recognized and logic switching occurs.

Because the HFD3212 reacts to transitions in the optical signal rather than DC levels, it shows excellent stability versus temperature and other operating conditions. Also, the device is much less sensitive to the absolute level of the optical signal than DC coupled receivers, allowing for a large range of optical source powers and/or link distances to be directly interfaced.

Not recommended for new designs

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**ELECTRO-OPTICAL CHARACTERISTICS** ($T_C$ = 25°C, $V_{CC}$ = 5 VDC unless otherwise stated)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Minimum Input Sensitivity | $P_{IN}$ (peak) | | 0.5 | 1.0 | µW | $\lambda_P$ = 850 nm into 100/140 µm optical fiber, f = 2.5 MHz, Duty Cycle = 50% |
| High Level Logic Output Voltage | $V_{OH}$ | 2.4 | 3.3 | | V | $P_{IN} \leq 0.1$ µW, $I_O \leq 0.8$ mA |
| Low Level Logic Output Voltage | $V_{OL}$ | | | 0.4 | V | $P_{IN} \geq 1$ µW, $I_O \leq 0.8$ mA |
| Rise Time | $t_R$ | | 12 | | ns | $P_{IN}$ = 1 µW, $V_O$ = 0.4 to 2.4 V |
| Fall Time | $t_F$ | | 3 | | ns | $P_{IN}$ = 1 µW, $V_O$ = 2.4 to 0.4 V |
| Supply Current | $I_{CC}$ | | 15 | 20 | mA | $P_{IN} \geq 1$ µW, $V_{CC}$ = 5.0 V |
| Pulse Width Distortion | PWD | | 5 | 10 | % | $P_{IN}$ = 1 µW peak |
| | | | 20 | 25 | | $P_{IN}$ = 100 µW peak<br>f = 2.5 MHz, Duty Cycle = 50% |

**ABSOLUTE MAXIMUM RATINGS**

(25°C Free-Air Temperature unless otherwise noted)

| | |
|---|---|
| Storage temperature | -40 to +100°C |
| Operating temperature | -40 to +100°C |
| Lead solder temperature | 260°C, 10 s |
| Junction temperature | 150°C |
| Supply voltage | +6 V |

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED OPERATING CONDITIONS**

| | |
|---|---|
| Operating temperature | -40 to +85°C |
| Supply voltage | +4.5 to +5.5 V |
| Optical input power | 1 to 100 µW |
| Optical signal pulse width | > 100 ns |
| Optical signal edges (10 to 90%) | < 20 ns |

Not recommended for new designs

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### ORDER GUIDE

| Description | Catalog Listing |
|---|---|
| Fiber DIP package | HFD3212-002 |
| Fiber DIP package Alternate Pinout | HFD3212-003 |

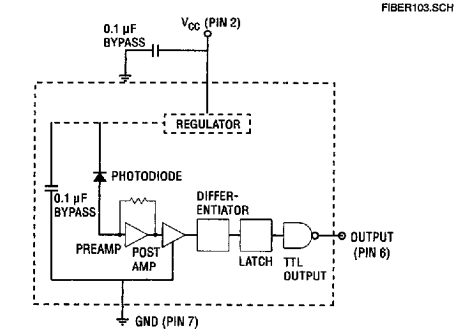
### CAUTION

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.


### FIBER INTERFACE

Honeywell detectors are designed to interface with multimode fibers with sizes (core/cladding diameters) ranging from 50/125 to 200/230 microns. Honeywell performs final tests using 100/140 micron core fiber. The fiber chosen by the end user will depend upon a number of application issues (distance, link budget, cable attenuation, splice attenuation, and safety margin). The 50/125 and 62.5/125 micron fibers have the advantages of high bandwidth and low cost, making them ideal for higher bandwidth installations. The use of 100/140 and 200/230 micron core fibers results in greater power being coupled by the transmitter, making it easier to splice or connect in bulkhead areas. Optical cables can be purchased from a number of sources.

### BLOCK DIAGRAM




### SWITCHING WAVEFORM

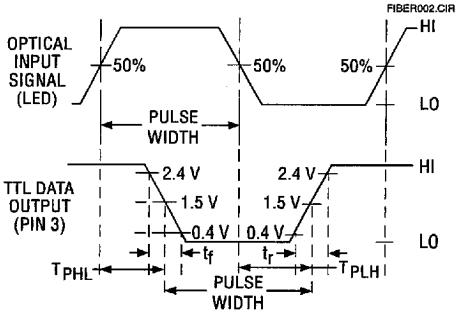



Fig. 1 Pulse Width Distortion vs Temperature

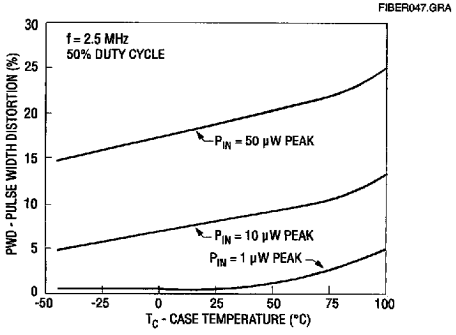
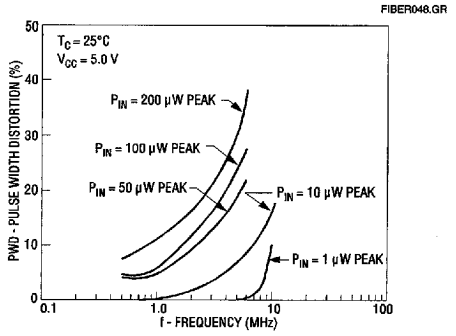



Fig. 2 Pulse Width Distortion vs Frequency





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## TTL Output Receiver

Fig. 3 Pulse Width Distortion vs Optical Input Power

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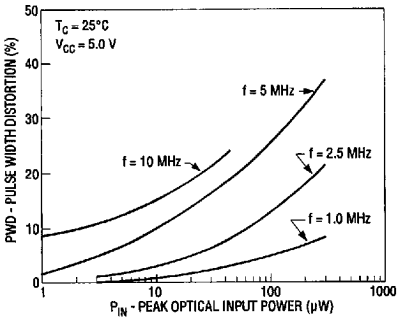


Fig. 4 Propagation Delay vs Optical Input Power

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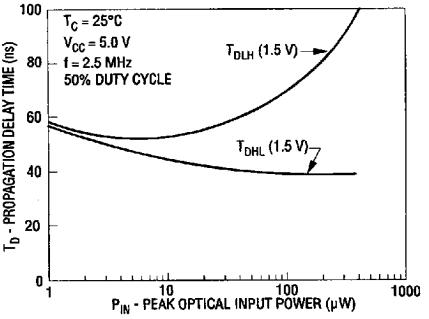


Fig. 5 Supply Current vs Temperature

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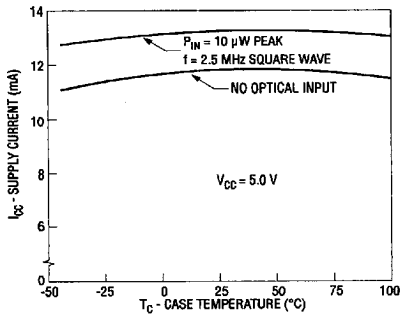


Fig. 6 Spectral Responsivity

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