APPLICATION (continued)

Resistor R_{ADJ} adjusts the $\overline{SQ}$ threshold upward. A 70 µA current from this node to ground increases the threshold by 1 dB of optical power. R_{ADJ}'s high side is at 4.3 V (nominal).

The open collector output ($\overline{PKT}$) indicates presence of a valid Ethernet packet. This output goes low following the first two data edges that are 200 ns or less apart at the start of a packet. It returns high before the end of the first cycle of a valid 1 MHz idle signal.

The HFM1200 is designed to operate with a 12 V supply (normally present in FOIRL interfaces and personal computer backplanes). The module requires a minimum +8.5 V total voltage. If a +12 V supply is not available, +5 V to V_{CC} pin and -5 V to GND pin will operate the module. Since the outputs are typically AC coupled, this voltage shift is generally not a problem. Data out2 (+) is positive with respect to data out1 (-) when no light is present at the optical input.

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HFM1200

Ethernet Receiver

ELECTRO-OPTICAL CHARACTERISTICS (Over 0 to 70°C, V_{CC} = 11.25 to 15.75 VDC unless otherwise stated)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Data Rate			10		Mbd	Manchester coding
Input Power		-35		-12	dBm	Average power (10^{-10} BER)
Supply Current			32	43	mA	Excluding SQ, SQLED, PKT
Propagation Delay			28	40	ns	
Jitter (uncorrelated)			0.4	0.6	ns	RMS, -32.5 dBm average input
Pulse Width Distortion (1)				7	ns	SQ Low, -12 dBm average input
Signal Quality Detect (SQ) (2)			-35	-32.5	dBm	Threshold for SQ, high to low Transition
Signal Quality Detect Hysteresis			-1.3		dB	Threshold change for SQ low to high transition
Delay Time (acceptable level) (3)				4	µs	P_{IN} > -30 dBm average
Delay Time (unacceptable level)		3		20	µs	P_{IN} < -12 dBm average
Packet Detection (PKT)						Bit times @ 10 Mbd (with < 20 pF and 4 kΩ load)
Delay of Packet Start				2		
End of Packet Delay				4		
Optical Idle Signal						
Frequency		0.85	1	1.25	MHz	
Duty Cycle		45		55	%	
Output (Out1/Out2)						
Load		500			Ω	
Output Swing		1	1.6		V	Peak to peak
			+1000		ppm/°C	Over temperature
SQ/PKT V_{OL}				0.4	V	I_{OL} ≤ 3 mA
SQLED Sink Current			12		mA	

Notes

1. Using a 10 MHz square wave input optical signal; t_r= 7 ns, t_f= 10 ns. The maximum PWD specified could be achieved by the user in system operation at 70°C.
2. Using R_{ADJ} = infinity Ohms.
3. See Figure 1.

ABSOLUTE MAXIMUM RATINGS

(25°C Free-Air Temperature unless otherwise noted)

Supply voltage (V_{CC})	8.5 to 15.75 V
Temperature	-40 to +85°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Supply voltage (V_{CC})	11.25 to 12.75 V
Temperature	0 to +70°C

ORDER GUIDE

Description	Catalog Listing
Fiber Optic Ethernet Receiver, 16 pin DIP	HFM1200-331

CAUTION

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.

Honeywell