H1824
H1824C

1800 CMOS Microprocessor Family
32×8 Static RAM

HUGHES AIRCRAFT COMPANY

MICROELECTRONICS CENTER

32 x 8 Static RAM — 1824

DESCRIPTION

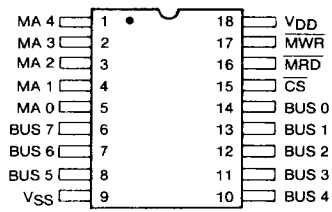
Hughes 1824 is a static CMOS Random Access Memory organized as 32 registers of 8 bits, and contains a common bi-directional three state data bus enabled by the Memory Read ($\overline{MRD}$) signal. Data is written into the RAM when the chip is selected ($\overline{CS}$ = 0) and the Memory Write ($\overline{MWR}$) signal is asserted. Data is accessed by decoding the address lines and is transmitted onto the data bus when $\overline{CS}$ and $\overline{MRD}$ are enabled. The 1824 is fully decoded and does not require a precharge or clocking signal. This RAM may be used to provide a data stack or buffer storage for small systems.

The 1824 operates over a 4-10.5 voltage supply while the 1824C operates over a 4-6.5 voltage supply. The 1824 is available in an 18 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request.

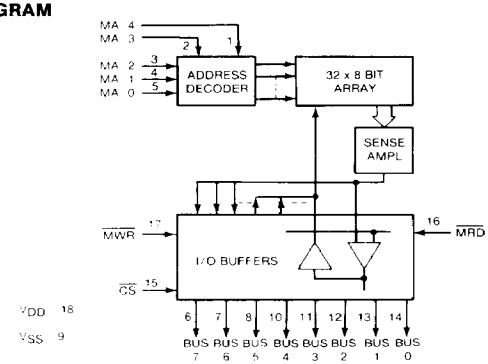
FEATURES

- Static Silicon Gate CMOS Circuitry
- Interfaces Directly to 1802A Microprocessor without Additional Components
- Access Time
  550ns typical at V_{DD} = 5V
  270ns typical at V_{DD} = 10V
- Single Voltage Supply
- Low Quiescent and Operating Power
- No Precharge or Clock Required

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... − 55 to + 125°C
- Plastic Package ..... − 40 to + 85°C

DC Supply — Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1824 ..... − 0.5 to + 13 Volts
- 1824C ..... − 0.5 to + 7 Volts

Input Voltage Range ..... V_{SS} −0.3V to V_{DD} + 0.3V
Storage Temperature Range (T_{stg}) .... − 65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

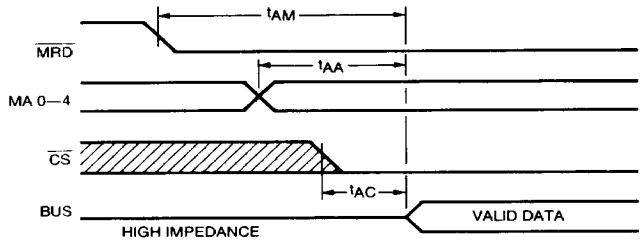
OPERATING CONDITIONS at T_A = Full Package Temperature Range Unless Otherwise Specified

CHARACTERISTICS	CONDITIONS V_{DD} (V)	LIMITS 1824 Min.	1824 Max.	1824C Min.	1824C Max.	UNITS
Supply Voltage Range	—	4	10.5	4	6.5	V
Recommended Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r, t_f	5	—	5	—	5	µS
	10	—	2	—	—	

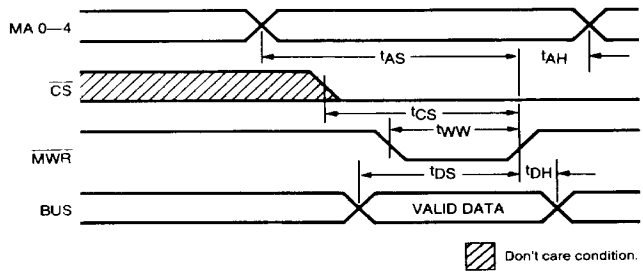
CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	1824 Min.	1824 Typ.[1]	1824 Max.	1824C Min.	1824C Typ.[1]	1824C Max.	UNITS
STATIC ELECTRICAL CHARACTERISTICS at T_A = −55 to +125° C, V_{DD} ± 5%										
Quiescent Device Current, I_L[4]	—	—	5	—	50	100	—	250	500	A
	—	—	10	—	250	500	—	—	—	
Output Voltage	—	0.5	5	—	0	0.5	—	0	0.5	V
Low Level, V_{OL}[3]	—	0, 10	10	—	0	0.5	—	—	—	
High Level, V_{OH}[3]	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Voltage	1.5, 2	—	5	—	—	1.5	—	—	1.5	V
Low Level, V_{IL}	1, 9	—	10	—	—	3	—	—	—	
High Level, V_{IH}	1.5, 2	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Output Drive Current	0, 5	.4	5	1.8	2.3	—	1.8	2.3	—	mA
N-Channel (Sink) I_{DN}	0, 10	.5	10	3.6	4.5	—	—	—	—	
P-Channel (Source), I_{DP}	0, 5	4.6	5	− 0.9	− 1.1	—	− 0.9	− 1.1	—	
	0, 10	9.5	10	− 1.8	−2.3	—	—	—	—	
Input Leakage, I_{IL}, I_{IH}[4]	—	Any Input	5, 10	—	± 1	± 1	—	±1	± 1	µA
3-State Output Leakage	0, 5	0, 5	5	—	± 1	±1	—	±1	±1	µA
Current I_{OUT}[4]	0, 10	0, 10	10	—	± 1	±1	—	—	—	
DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = −55 to 125°C, V_{DD} nominal, C_L = 50 pF, R_L > 10MΩ										
Read Operation										
Access Time From	—	—	5	—	550	710	—	550	710	ns
Address Change, t_{AA}		—	10	—	270	320	—	—	—	
Access Time From	—	—	5	—	540	690	—	540	690	ns
Chip Select, t_{AC}[2]		—	10	—	260	310	—	—	—	
Output Valid From	—	—	5	—	540	690	—	540	690	ns
MRD, t_{AM}[2]		—	10	—	260	310	—	—	—	
Write Operation										
Write Pulse Width, t_{WW}	—	—	5		300	425		300	425	ns
		—	10		150	180	—	—	—	
Data Setup Time, t_{DS}	—	—	5		300	425		300	425	ns
		—	10		150	180	—	—	—	
Data Hold Time, t_{DH}	—	—	5		70	70		70	70	ns
		—	10		30	35	—	—	—	
Chip Select Setup Time, t_{CS}	—	—	5		300	425		300	425	ns
		—	10		150	215	—	—	—	
Address Setup Time, t_{AS}	—	—	5		500	650		500	650	ns
		—	10		300	390	—	—	—	
Address Hold Time, t_{AH}	—	—	5	—	100	100	—	100	100	ns
		—	10	—	50	50	—	—	—	

NOTE 1: Typical values are for T_A = +25°C and nominal V_{DD}.
NOTE 2: t_{AC} and t_{AM} are given as minimum times for valid data outputs. Longer times will initiate an earlier but invalid input.
NOTE 3: Design assured but not tested.
NOTE 4: Parameters guaranteed by other tests at −55°C.

Read Operation



Write Operation



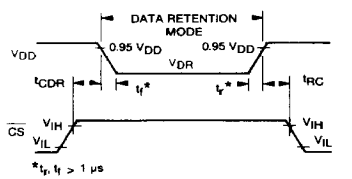
The dynamic characteristic table and the above timing diagrams represent maximum performance capability of the 1824. When used in direct system interface with the 1802A microprocessor, the timing relation will be determined by the clock frequency and timing signal generation of the microprocessor. In the latter case the following general timing conditions hold.

$t_{WW} = 2t_C$ $t_{AH} = 1.0t_C$ $t_{AS} = 4.5t_C$
$t_{DH} = 1.0t_C$
$t_{DS} = 5.5t_C$ Data transfers from 1802A to Memory

$\overline{MRD}$ occurs one clock period (t_C) earlier than address bus MA 0-MA 7
t_C = 1/1802A clock frequency

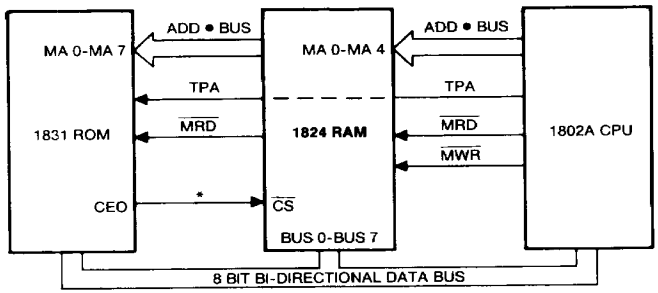
DATA RETENTION CHARACTERISTICS at T_A = −55 to +125° C

CHARACTERISTICS	CONDITIONS	V_{DD} (V)	1824		1824C		UNITS
			Min.	Max.	Min.	Max.	
Data Retention Voltage, V_{DR}	—	—	2.5	—	2.5	—	V
Data Retention Quiescent Current, I_{DD}	V_{DR} = 2.5V	—	—	50	—	250	µA
Chip Deselect to Data Retention Time, t_{CDR}	V_{DR} = 2.5V	5 10	600 300	—	600 —	—	ns
Recovery to Normal Operation Time, t_{RC}	V_{DR} = 2.5V	5 10	600 300	—	600 —	—	



Low V_{DD} data retention waveforms and timing diagram.

SYSTEM INTERCONNECT



*Chip select may be derived through (1) address decode, (2) CEO signal from ROM, or (3) always enabled (GND) per system requirements.

For a microprocessor system requiring a minimal amount of writable storage, the 1824 can be used as an adequate scratch pad memory and as stack storage for a wide range of control applications. No additional interface elements are required.

SIGNAL DESCRIPTION

MA 0-MA 4: These five input address lines select one of 32 eight bit words. They are statically decoded on the chip to directly access the register array.

BUS 0-BUS 7: These eight bi-directional three state data lines form a data bus common with the 1802A microprocessor. Data is written into the RAM or read from the RAM through these lines.

$\overline{\text{MRD}}$, $\overline{\text{MWR}}$, $\overline{\text{CS}}$: These three control signals determine chip selection bi-directional data control and operation of the chip when activated as follows:

$\overline{\text{MRD}}$ = Memory Read
$\overline{\text{MWR}}$ = Memory Write
$\overline{\text{CS}}$ = Chip Select (allows memory expansion)

FUNCTION	$\overline{\text{CS}}$	$\overline{\text{MRD}}$	$\overline{\text{MWR}}$	DATA LINES
Read	0	0	X	Output Mode
Write	0	1	0	Input Mode
Not Selected	1	X	X	High Impedance Mode
Standby	0	1	1	High Impedance Mode

Logic 1 = High Logic 0 = Low X = Don't Care
NOTE: $\overline{\text{MRD}}$ overrides $\overline{\text{MWR}}$

Hughes Microelectronics Center
500 Superior Avenue, Box H
Newport Beach, CA 92658-8903
Tele: (714) 759-2727
FAX: (714) 759-2720

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