H1824 H1824C



1800 CMOS Microprocessor Family 32×8 Static RAM

MICROELECTRONICS CENTER

32 x 8 Static RAM --- 1824

DESCRIPTION

Hughes 1824 is a static CMOS Random Access Memory organized as 32 registers of 8 bits, and contains a common bi-directional three state data bus enabled by the Memory Read ($\overline{\text{MRD}}$) signal. Data is written into the RAM when the chip is selected ($\overline{\text{CS}}$ = 0) and the Memory Write ($\overline{\text{MWR}}$) signal is asserted. Data is accessed by decoding the address lines and is transmitted onto the data bus when $\overline{\text{CS}}$ and $\overline{\text{MRD}}$ are enabled. The 1824 is fully decoded and does not require a precharge or clocking signal. This RAM may be used to provide a data stack or buffer storage for small systems.

The 1824 operates over a 4-10.5 voltage supply while the 1824C operates over a 4-6.5 voltage supply. The 1824 is available in an 18 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

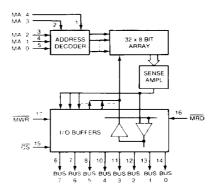
Static Silicon Gate CMOS Circuitry

- Interfaces Directly to 1802A Microprocessor without Additional Components
- Access Time 550ns typical at Vpp = 5V 270ns typical at Vpp = 10V
- Single Voltage Supply
- · Low Quiescent and Operating Power
- No Precharge or Clock Required

PIN CONFIGURATION

MA 4 🖂	1 • ~	18	DO VDD
МАЗ□	2	17	MWR
MA 2 [3	16	MRD
MA 1 🚞	4	15	cs cs
MA 0	5	14	BUS 0
BUS 7 🗔	6	13	BUS 1
BUS 6 🗔	7	12	BUS 2
BUS 5	8	11	BUS 3
Vss C	9	10	BUS 4

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (TA) Ceramic Package - 55 to + 125°C Plastic Package - 40 to + 85°C DC Supply -- Voltage Range (VDD)

(All voltage values referenced to VSS terminal)

1824 - 0.5 to + 13 Volts 1824C - 0.5 to + 7 Volts

Input Voltage Range VSS -0.3V to VDD + 0.3V Storage Temperature Range (T_{stg}) -65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at TA = Full Package Temperature Range Unless Otherwise Specified

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CHARCIERITICS	Voc.	1 2 1 1	24	140	46	
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Supply Voltage Range	_	4	10.5	4	6.5	V
Recommended Input Voltage Range	_	Vss	VDD	v _{ss}	V _{DD}	٧
	5		5		5	μS
Input Signal Rise and Fall Time, t _f , t _f ,	10		2	_	_	F -

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		CHENTICH			115		m 🔠	in profit		li ic
- constraint of	10	STATE OF STATE OF STATE OF			1954			Type	Name:	
STATIC ELECTRICAL CHARACTERISTIC	CS at TA = -55 to	+125° C, V	D ± 5%							
		- I	5		50	100		250	500	
Quiescent Device Current, IL4	_		10	_	250	500				
Output Voltage		0.5	5	_	0	0.5		0	0.5	
Low Level, VOL 3	_	0, 10	10		0	0.5] ,
		0, 5	5	4.9	5		4.9	5	_	٧
High Level, VOH3	_	0, 10	10	9.9	10		_			
input Voltage	1.5, 2		5	_		1.5			1.5	
Low Level, VIL	1, 9		10		_	3				v
	1.5, 2		5	3.5		_	3.5	_		•
High Level, V _{IH}	1, 9	_	10	7	-		_	-	-	
Output Drive Current	0, 5	.4	5	1.8	2.3	_	1.8	2.3		
N-Channel (Sink) I _D N	0, 10	.5	10	3.6	4.5	-	_		_	
	0, 5	4.6	5	- 0.9	- 1.1	_	- 0.9	- 1.1		m
P-Channel (Source), IDP	0, 10	9.5	10	- 1.8	-2.3	_	_		-	
					± 1	± 1	_	±1	± 1	į.
nout Leakage, hr., luu 4		Any Input	5, 10	_	T	I				
	0, 5	Any Input 0, 5	5, 10	_	±1	±1		±1	±1	
Input Leakage, I _{IL} , I _{IH} ⁴ 3-State Output Leakage Current Iou II ⁴	0, 5 0, 10							±1	±1 —	μ
	0, 10	0, 5 0, 10	5 10	=	±1	±1		±1 —	±1 —	μ,
3-State Output Leakage Current I _{OUT} ⁴ DYNAMIC ELECTRICAL CHARACTERIST	0, 10	0, 5 0, 10	5 10	=	±1	±1		±1 —	±1 —	μ
3-State Output Leakage Current I _{OUT} 4 DYNAMIC ELECTRICAL CHARACTERIST Read Operation	0, 10	0, 5 0, 10	5 10	=	±1	±1		±1 —	#1 —	
3-State Output Leakage Current I _{OUT} 4 DYNAMIC ELECTRICAL CHARACTERIST Read Operation	0, 10	0, 5 0, 10 125°C, V _D	5 10 p nominal,		± 1 ± 1 oF, R _L > 10	±1 ±1 Mn				
3-State Output Leakage Current I _{OUT} ⁴ DYNAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, t _{AA}	0, 10	0, 5 0, 10 125°C, V _D	5 10 p nominat, 5		± 1 ± 1 oF, R _L > 10	±1 ±1 MΩ				n
3-State Output Leakage Current toUT ** OUTPUT AND THE STATE OF T	0, 10	0, 5 0, 10 125°C, V _D	5 10 p nominal, 5		± 1 ± 1 oF, R _L > 10 550 270	±1 ±1 MΩ 710 320		550	710	n
3-State Output Leakage Current I _{QUT} ⁴ DVNAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, t _{AA} Access Time From Chip Select, t _{AC} ²	0, 10	0, 5 0, 10 125°C, V _D	5 10 D nominat, 5 10 5		± 1 ± 1 oF, R _L > 10 550 270 540	±1 ±1 MΩ 710 320 690		550	710	n
3-State Output Leakage Current I _{QUT} ⁴ DVNAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, I _{AA} Access Time From Chip Select, I _{AC} ² Output Valid From	0, 10	0, 5 0, 10 0 125°C, VD	5 10 D nominai, 5 10 5		± 1 ± 1 5F, R _L > 10 550 270 540 260	±1 ±1 Mn 710 320 690 310		550 540	710 — 690	n
3-State Output Leakage Current toUT ⁴ POYNAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, taA Access Time From Chip Select, taC ² Output Valid From MRD, taMa ²	0, 10	0, 5 0, 10 0 125°C, VD	5 10 nominal, 5 10 5		±1 ±1 5F, R _L > 10 550 270 540 260 540	±1 ±1 MΩ 710 320 690 310 690		550 540	710 — 690	n
3-State Output Leakage Current ToUT 4 POPMAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, t _A A Access Time From Chip Select, t _A C ² Output Valid From MRD, t _A M ² Write Operation	0, 10	0, 5 0, 10 0 125°C, VD	5 10 nominal, 5 10 5		±1 ±1 5F, R _L > 10 550 270 540 260 540	±1 ±1 MΩ 710 320 690 310 690		550 540	710 — 690	n
3-State Output Leakage Current ToUT 4 POPMAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, t _A A Access Time From Chip Select, t _A C ² Output Valid From MRD, t _A M ² Write Operation	0, 10	0, 5 0, 10 0 125°C, VD	5 10 0 nominal, 5 10 5 10 5		±1 ±1 oF, R _L > 10 550 270 540 260 540 260	±1 ±1 MΩ 710 320 690 310 690 310		550 	710 — 690 — 690	n
3-State Output Leakage Current I _{QUT} ⁴ OVINAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, I _{AA} Access Time From Chip Select, I _{AC} ² Output Valid From MRD, I _{AM} ² Write Operation Write Pulse Width, I _{WW}	0,10 O,10 O,10	0, 5 0, 10 0 125°C, VD	5 10 0 nominat, 5 10 5 10 5		±1 ±1 5F, R _L > 10 550 270 540 260 540 260 300	#1 #1 #1 Mn 710 320 690 310 690 310 425	_ _ _ _	550 	710 — 690 — 690	n
3-State Output Leakage Current I _{QUT} ⁴ OVINAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, I _{AA} Access Time From Chip Select, I _{AC} ² Output Valid From MRD, I _{AM} ² Write Operation Write Pulse Width, I _{WW}	0, 10	0, 5 0, 10 0 125°C, VD	5 10 nominal, 5 10 5 10 5 10 5		±1 ±1 5F, RL > 10 550 270 540 260 260 300 150	±1 ±1 Mn 710 320 690 310 690 310 425 180	_ _ _ _	550 540 540 300	710 — 690 — 690 —	n
3-State Output Leakage Current I _{QUT} ⁴ DVINAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, I _{AA} Access Time From Chip Select, I _{AC} ² Output Valid From MRD, I _{AM} ² Write Operation Write Pulse Width, I _{WW} Data Setup Time, I _{DS}	0,10 O,10 O,10	0, 5 0, 10 0 125°C, VD	5 10 nominat, 5 10 5 10 5 10 5 10 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 10 5 5 5 5		±1 ±1 5F, R _L > 10 550 270 540 260 540 260 300 150 300	#1 #1 mn 710	-	550 540 540 300	710 — 690 — 690 — 425 —	n n
3-State Output Leakage Current I _{QUT} ⁴ DVNAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, I _{AA} Access Time From Chip Select, I _{AC} ² Output Valid From MRD, I _{AM} ² Write Operation Write Pulse Width, I _{WW} Data Setup Time, I _{DS}	0,10 O,10 O,10	0, 5 0, 10 0 125°C, VD	5 10 p nominat, 5 10 5 10 5 10 5 10		±1 ±1 5F, R _L > 10 550 270 540 260 540 260 300 150 300 150	±1 ±1 Mn 710 320 690 310 690 310 425 180 425 180	-	550 	710 	n n:
3-State Output Leakage Current toUT 4 POTATION TO THE PROPERT OF	0,10 O,10 O,10	0, 5 0, 10 125°C, V _D	5 10 p nominat, 5 10 5 10 5 10 5 10 5		±1 ±1 5F, RL > 10 550 270 540 260 540 260 300 150 300 150 70	±1 ±1 100000000000000000000000000000000	- - - - - -	550 	710 	n n: n:
3-State Output Leakage Current I _{QUT} ⁴ DVNAMIC ELECTRICAL CHARACTERIST Read Operation Access Time From Address Change, I _{AA} Access Time From Chip Select, I _{AC} ² Output Valid From MRD, I _{AM} ² Write Operation Write Pulse Width, I _{WW} Data Setup Time, I _{DS}	0,10 O,10 O,10	0, 5 0, 10 125°C, V _D	5 10 p nominat, 5 10 5 10 5 10 5 10 5 10 5		±1 ±1 550, R _L > 10 550 270 540 260 540 260 300 150 300 150 70 30	#1 #1 #1 #1 #1 #1 #1 #1 #1	- - - - - -	550 540 	710 ————————————————————————————————————	n n: n:
3-State Output Leakage Current to_UT 4 OUTPUT OUTP	0,10 O,10 O,10	0, 5 0, 10 125°C, V _D	5 10 p nominat, 5 10 5 10 5 10 5 10 5 10 5 10 5 10		±1 ±1 5F, R _L > 10 550 270 540 260 540 260 300 150 300 150 30 30 30 30 30 30	#1 #1 Mn 710 320 690 310 425 180 425 180 70 425	- - - - - -	550 	710 	n n:
3-State Output Leakage Current toUT 4 POTATION TO THE PROPERT OF	0,10 O,10 O,10	0, 5 0, 10 125°C, V _D	5 10 p nominal, 5 10 5 10 5 10 5 10 5 10 5 10 5 10 5		±1 ±1 5F, RL > 10 550 270 540 260 540 260 540 150 300 150 300 150 300 150	#1 #1 Mn 710 320 690 310 425 180 70 35 425 215	- - - - - -	550 	710 — 690 — 690 — 425 — 425 — 425 — 425 — 425	n n:
3-State Output Leakage Current to_UT 4 OUTPUT OUTP	0,10 O,10 O,10	0, 5 0, 10 0 125°C, V _D	5 10 0 nominat, 5 10 5 10 5 10 5 10 5 10 5 10 5 10 5 1		±1 ±1 5F, R _L > 10 550 270 540 260 540 260 150 300 150 300 150 70 30 300 150 50 50 50 50 50 50 50 50 50 50 50 50 5	±1 ±1 Mn 710 320 690 310 690 310 425 180 425 180 70 35 425 215 660		550 	710 	

NOTE 1: Typical values are for TA = +25°C and nominal VDD.

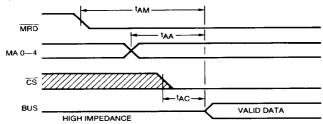
NOTE 2: tAC and tAM are given as minimum times for valid data outputs. Longer times will initiate an earlier but invalid input.

NOTE 3: Design assured but not tested.

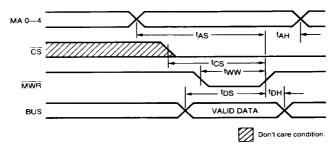
NOTE 4: Parameters guaranteed by other tests at -55°C.

TIMING DIAGRAMS H1824/1824C

Read Operation



Write Operation



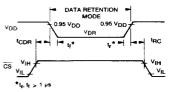
The dynamic characteristic table and the above timing diagrams represent maximum performance capability of the 1824. When used in direct system interface with the 1802A microprocessor, the timing relation will be determined by the clock frequency and timing signal generation of the microprocessor. In the latter case the following general timing conditions hold.

$$\begin{array}{ll} t_{WW}=2t_{C} & t_{AH}=1.0t_{C} & t_{AS}=4.5t_{C} \\ t_{DH}=1.0t_{C} & t_{DS}=5.5t_{C} \\ \end{array}$$
 Data transfers from 1802A to Memory

 $\overline{\text{MRD}}$ occurs one clock period (t_C) earlier than address bus MA 0-MA 7 t_C = 1/1802A clock frequency

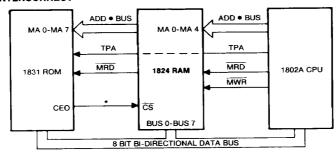
DATA RETENTION CHARACTERISTICS at TA = -55 to +125° C

	es de la composition	W					e de la constante de la consta
Data Retention Voltage, VDR	_	_	2.5	_	2.5	_	٧
Data Retention Quiescent Current, Ipp	V _{DR} = 2.5V	_	_	50	_	250	μА
Chip Deselect to Data Retention Time, tCDR	V _{DR} = 2.5V	5 10	600 300	_	600 —	-	ns
Recovery to Normal Operation Time, t _{RC}	V _{DR} = 2.5V	5 10	600 300		600		



Low $\mbox{V}_{\mbox{\scriptsize DD}}$ data retention waveforms and timing diagram.

SYSTEM INTERCONNECT



*Chip select may be derived through (1) address decode, (2) CEO signal from ROM, or (3) always enabled (GND) per system requirements.

For a microprocessor system requiring a minimal amount of writable storage, the 1824 can be used as an adequate scratch pad memory and as stack storage for a wide range of control applications. No additional interface elements are required.

SIGNAL DESCRIPTION

MA 0-MA 4: These five input address lines select one of 32 eight bit words. They are statically decoded on the chip to directly access the register array.

BUS 0-BUS 7: These eight bi-directional three state data lines form a data bus common with the 1802A microprocessor. Data is written into the RAM or read from the RAM through these lines.

MRD, MWR, CS: These three control signals determine chip selection bi-directional data control and operation of the chip when activated as follows:

MRD = Memory Read

MWR = Memory Write

CS = Chip Select (allows memory expansion)

FUNCTION	CS	MRD	MWR	DATA LINES
Read	0	0	×	Output Mode
Write	0	1	0	Input Mode
Not Selected	1	×	×	High Impedance Mode
Standby	0	1	1	High Impedance Mode

Logic 1 = High Logic 0 = Low X = Don't Care NOTE: MRD overrides MWR

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