H1856/1857
H1856C/1857C

1800 CMOS Microprocessor Family
4-Bit Bus Buffers/Separators

HUGHES
AIRCRAFT COMPANY
MICROELECTRONICS CENTER

DESCRIPTION

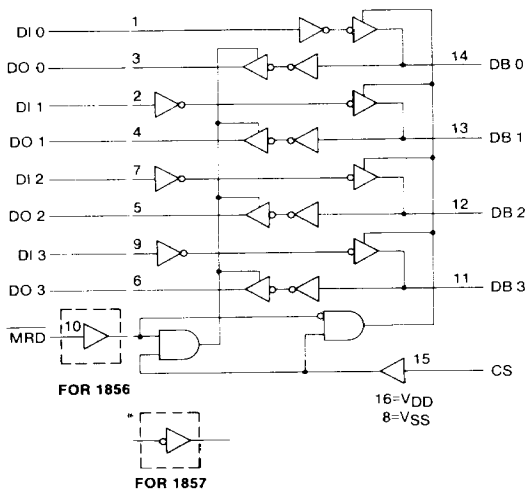
Hughes 1856 and 1857 are 4-bit bus buffer/separators to allow data to be split from a single bi-directional bus into separate input and output busses. The 1857 is intended for peripheral or I/O bus control while the 1856 is intended for memory bus control. The difference between the two devices is in the polarity of the input buffer for the Memory Read ($\overline{MRD}$) signal. This signal is inverted in the 1857, and enables the $\overline{MRD}$ signal to set the input mode in the 1856 or to set the output mode in the 1857. When $\overline{MRD} = V_{DD}$ the output mode is set in the 1856 and the input mode is set in the 1857.

The 1856 and 1857 operate over a 4-10.5 voltage range while the 1856C and 1857C operate over a 4-6.5 voltage range. The 1856 and 1857 are available in a 16 hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request.

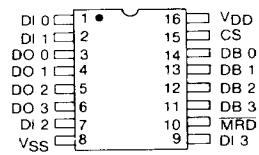
FEATURES

- Static Silicon Gate CMOS Circuitry
- Compatible with 1802A Microprocessor
- Provides easy connection of Memory or I/O Devices to 1802A Microprocessor Bus
- Provides Non-inverted Bi-directional Buffered Data Transfer
- Chip Select for Simple System Expansion
- Low Quiescent and Operating Power

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package ..... −55 to + 125°C
- Plastic Package ..... −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1856/1857 ..... −0.5 to + 11 Volts
- 1856C/1857C ..... −0.5 to + 7 Volts

Input Voltage Range ..... V_{SS} −0.3V to V_{DD} + 0.3V

Storage Temperature Range (T_{stg}) ..... −65 to + 150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range

Supply Voltage Range	—	4	10.5	4	6.5	V
Recommended Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

ELECTRICAL CHARACTERISTICS at T_A = −55° to 125°C Unless Otherwise Specified. .

Static Electrical Characteristics at T_A = −55° to 125°C, V_{DD} nominal Unless Otherwise Specified.										
Quiescent Device	—	—	5	—	1	10	—	5	50	µA
Current, I_L [4]	—	—	10	—	10	100	—	—	—	
Output Low Drive	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
(Sink) Current, I_{OL}	0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive	4.6	0, 5	5	−1.15	−2.3	—	−1.15	−2.3	—	mA
(Source) Current I_{OH}	9.5	0, 10	10	−2.6	−5.2	—	—	—	—	
Output Voltage	—	0, 5	5	—	0	0.1	—	0	0.1	V
Low Level V_{OL} [1, 3]	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage	—	0, 5	5	4.95	5	—	4.95	5	—	
High Level, V_{OH} [3]	—	0, 10	10	9.95	10	—	—	—	—	
Input Low Voltage	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	V
V_{IL}	1.0, 9.0	—	10	—	—	3	—	—	—	
Input High Voltage	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
V_{IH}	1.0, 9.0	—	10	7	—	—	—	—	—	
Input Leakage [4]	Any	0, 5	5	—	—	±1	—	—	±1	µA
Current, I_{IN}	Input	0, 10	10	—	—	±1	—	—	—	
Operating Current [3]	0, 5	0, 5	5	—	50	100	—	50	100	µA
I_{DD} [1,2]	0, 10	0, 10	10	—	150	300	—	—	—	
Input Capacitance, C_{IN} [3]	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT} [3]	—	—	—	—	10	15	—	10	15	pF
Dynamic Electrical Characteristics at T_A = −55° to 125°C, C_L = 50pF, V_{DD} nominal, V_{IH} = V_{DD}, V_{IL} = V_{SS}										
Propogation Delay Time:	—	—	5	—	150	225	—	150	225	ns
$\overline{MRD}$ or CS to DO, t_{ED}	—	—	10	—	75	125	—	—	—	
$\overline{MRD}$ or CS to DB,	—	—	5	—	150	225	—	150	225	ns
t_{EB}	—	—	10	—	75	125	—	—	—	
DI to DB,	—	—	5	—	100	150	—	100	150	ns
t_{IB}	—	—	10	—	50	75	—	—	—	
DB to DO,	—	—	5	—	100	150	—	100	150	ns
t_{DB}	—	—	10	—	50	75	—	—	—	

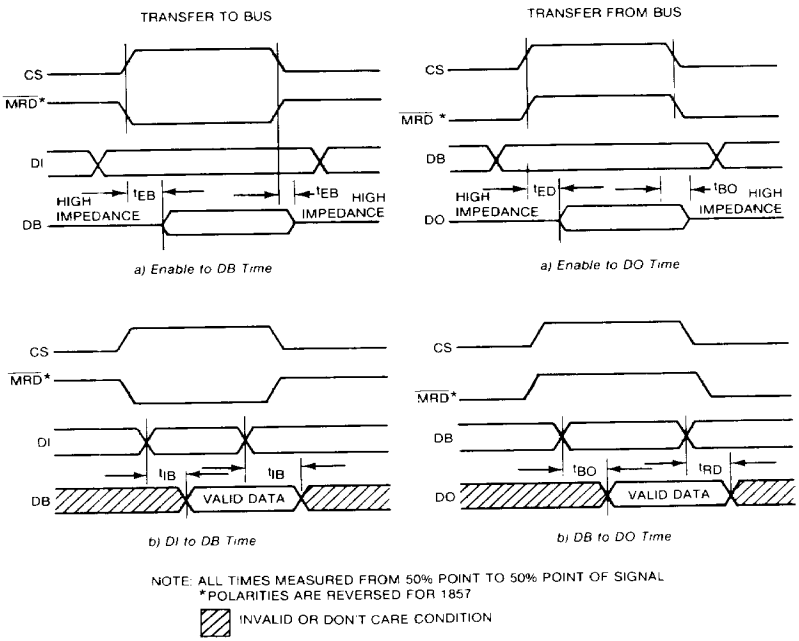
*Typical values are for T_A = +25°C and nominal voltage.

NOTE 1: I_{OL} = I_{OH} = 1 µA.

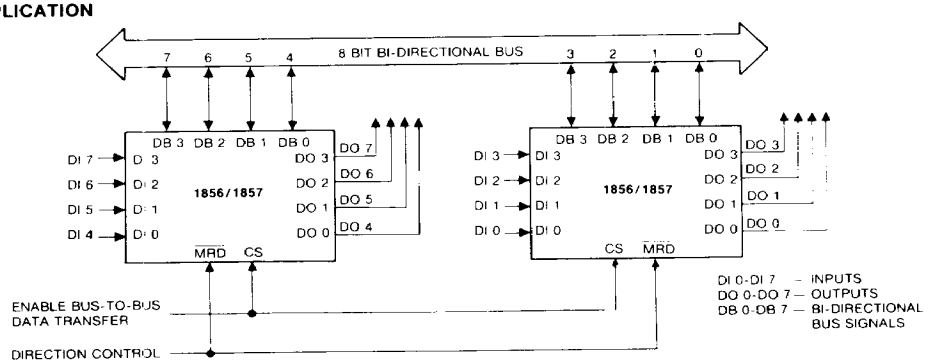
NOTE 2: Operating current measured in a 1802A at 2MHz with outputs floating.

NOTE 3: Design assured but not tested.

NOTE 4: Parameters guaranteed by other tests at −55°C.

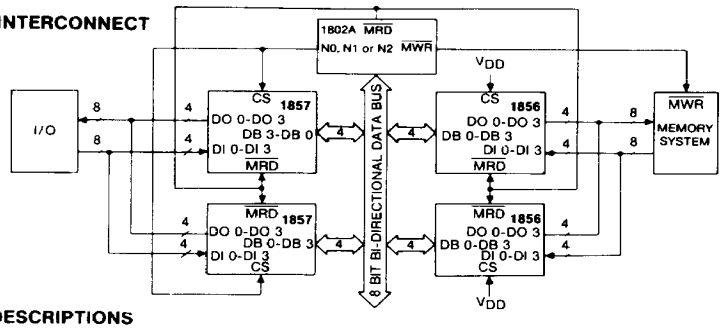


APPLICATION



The Figure shows how two 1856 or two 1857 can be used as bus buffers or separators between an 8 Bit Bi-directional Data bus and memories or between an 8 Bit Bi-directional Data bus and I/O devices. The chip select input signal enables the bus separator three-state output drivers. The direction of data flow, when enabled, is controlled by the state of the $\overline{MRD}$ input signal.

SYSTEM INTERCONNECT



SIGNAL DESCRIPTIONS

DB 0-DB 3: These four bi-directional signals can be used as data outputs or receiver inputs depending on the logic polarity of the $\overline{MRD}$ input signal. Data is non-inverted.

DI 0-DI 3: The four data inputs. They are enabled onto the corresponding DB lines when Chip Select (CS) and the Memory Read ($\overline{MRD}$) signals are activated.

DO 0-DO 3: The four receiver outputs reflect the data on the DB lines when the Chip Select and Memory Read signals are activated.

CS: The Chip Select signal along with $\overline{MRD}$ controls the activation of the 1856 and 1857 as indicated in the table below. CS is active when it is a logic high (V_{DD}).

$\overline{MRD}$: The Memory Read signal controls the direction of data flow when Chip Select is enabled. In the 1856, when $\overline{MRD}$ = 0, it enables the three state bus drivers (DB 0-DB 3), and outputs data from the driver inputs (DI 0-DI 3) to the data bus. When $\overline{MRD}$ = 1, it disables the three-state bus drivers and enables the three-state data output drivers (DO 0-DO 3), transferring data from the data bus to the data outputs.

In the 1857, when $\overline{MRD}$ = 1 it enables the three-state bus drivers (DB 0-DB 3) and transfers data from the driver inputs (DI 0-DI 3) onto the data bus. When $\overline{MRD}$ = 0, it disables the three-state bus drivers (DB 0-DB 3) and enables the three-state data output drivers (DO 0-DB 3), transferring data bus to the data outputs.

1856 FUNCTION TABLE
For Memory Data Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB 0-DB 3	DATA OUT DO 0-DO 3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	DATA IN	HIGH IMPEDANCE
1	1	HIGH IMPEDANCE	DATA BUS

1857 FUNCTION TABLE
For I/O Bus Separator Operation

CS	$\overline{MRD}$	DATA BUS OUT DB 0-DB 3	DATA OUT DO 0-DO 3
0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	HIGH IMPEDANCE	DATA BUS
1	1	DATA IN	HIGH IMPEDANCE

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