H1858/1859
H1858C/1859C

1800 CMOS Microprocessor Family
4-Bit Memory Latch/Decoder

HUGHES
MICROELECTRONICS CENTER

DESCRIPTION

Hughes 1858 and 1859 are 4-bit memory address latch/decoders which control 4K bytes of memory. The 1858 provides chip select outputs to control up to 32 H1822 (organized 256 x 4) RAMs. The 1859 provides chip select outputs to control RAMs organized 1024 x 1. The Enable input allows expansion of memory systems beyond 4K bytes of memory. The chip select outputs are a function of the memory address bits connected to the MA 0-MA 3 lines.

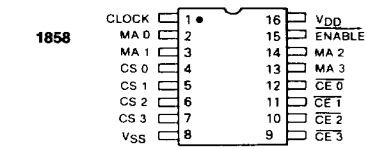
The 1858 and 1859 operate over a 4-10.5 voltage range while the 1858C and 1859C operate over a 4-6.5 voltage range. The 1858 and 1859 are available in a 16 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), or cerdip (Y suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

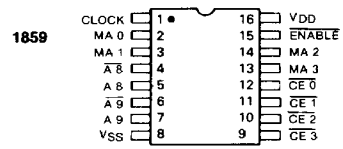
- Static Silicon Gate CMOS Circuitry
- Interfaces Directly with 1802A Microprocessor
- Chip Enable pin allows easy expansion above 4K Bytes of Memory
- Low Quiescent and Operating Power
- Allows direct control of 4K bytes of memory
- 1858 is designed for 256 x 4 Memory Configuration
- 1859 is designed for 1024 x 1 Memory Configuration

PIN CONFIGURATION

1858

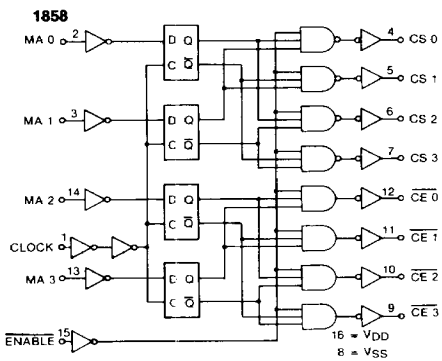


1859

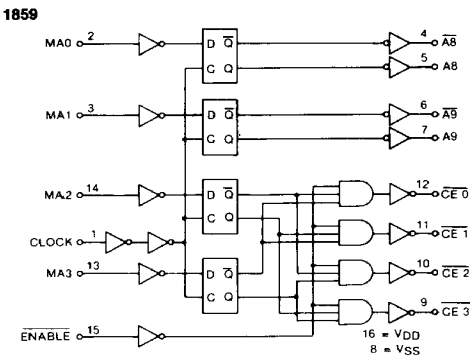


FUNCTIONAL DIAGRAM

1858



1859



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range (T_A)
- Ceramic Package . . . . . −55 to + 125°C
- Plastic Package . . . . . −40 to + 85°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- 1858/1859 . . . . . −0.5 to + 13V
- 1858C/1859C . . . . . −0.5 to + 7V

Input Voltage Range . . . . . V_{SS} −0.3V to V_{DD} + 0.3V

Storage Temperature Range (T_{stg}) . . . . . −65 to + 150°C

NOTE: Operating the device above the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS at T_A = Full Package Temperature Range

CHARACTERISTICS	CONDITIONS			LIMITS						UNITS
				1858 1859			1858C 1859C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Supply Voltage Range	–	–	–	4	–	10.5	4	–	6.5	V
Recommended Input Voltage Range	–	–	–	V_{SS}	–	V_{DD}	V_{SS}	–	V_{DD}	V
Minimum Clock Pulse Width, t_W[1]	–	–	5	–	50	75	–	50	75	ns
	–	–	10	–	25	40	–	–	–	
Minimum Data Setup Time, t_{DS}[1]	–	–	5	–	25	40	–	25	40	ns
	–	–	10	–	10	25	–	–	–	
Minimum Data Hold Time, T_{DH}[1]	–	–	5	–	0	25	–	0	25	ns
	–	–	10	–	0	10	–	–	–	
Static Electrical Characteristics at T_A = −55°C to 125°C Unless Otherwise Specified										
Quiescent Device Current, I_L[5]	–	0, 5	5	–	0.1	10	–	5	50	µA
	–	0, 10	10	–	1	100	–	–	–	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	0, 10	10	2.6	5.2	–	–	–	–	
Output High Drive (Source) Current, I_{OH}	4.6	0, 5	5	−1.15	−2.3	–	−1.15	−2.3	–	mA
	9.5	0, 10	10	−2.6	−5.2	–	–	–	–	
Output Voltage Low Level, V_{OL}[2,4]	–	0, 5	5	–	0	0.1	–	0	0.1	V
	–	0, 10	10	–	0	0.1	–	–	–	
Output Voltage High Level, V_{OH}[4]	–	0, 5	5	4.9	5	–	4.9	5	–	
	–	0, 10	10	9.9	10	–	–	–	–	
Input Low Voltage, V_{IL}	0.5, 4.5	–	5	–	–	1.5	–	–	1.5	V
	0.5, 9.5	–	10	–	–	3	–	–	–	
Input High Voltage, V_{IH}	0.5, 9.5	–	5	3.5	–	–	3.5	–	–	
	0.5, 9.5	–	10	7	–	–	–	–	–	
Input Leakage Current, I_{IN}[5]	Any	0, 5	5	–	10^{-4}	±1	–	10^{-4}	±1	µA
	Input	0, 10	10	–	10^{-4}	±2	–	–	–	
Operating Current, I_{DD}[3,5]	–	0, 5	5	–	50	400	–	50	400	µA
	–	0, 10	10	–	150	1000	–	–	–	
Input Capacitance, C_{IN}[4]	–	–	–	–	5	7.5	–	5	7.5	pF
Output Capacitance, C_{OUT}[4]	–	–	–	–	10	15	–	–	–	–

*Typical values are for T_A = 25°C and nominal voltage

Note 1: Maximum limits of minimum characteristics are the values above which all devices function.

Note 2: I_{OL} = I_{OH} = 1 µA.

Note 3: Measured in an 1802 system at 2 MHz with open outputs.

Note 4: Design assured but not tested.

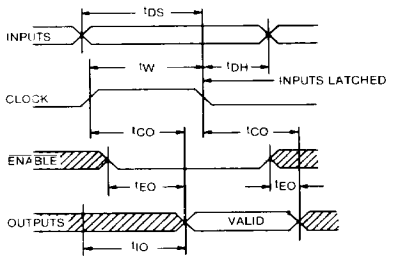
Note 5: Parameters guaranteed by other tests at −55°C.

OPERATING CONDITIONS, cont.

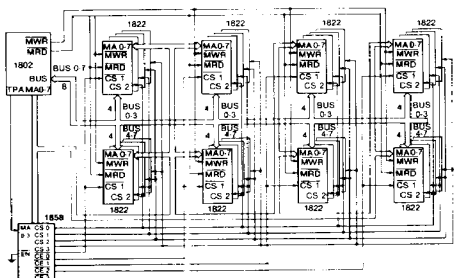
CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS 1859 Min.	1859 Typ.*	1859 Max.	1858C/1859C Min.	1858C/1859C Typ.*	1858C/1859C Max.	UNITS
Dynamic Electrical Characteristics at T_A = −55 to 125°C, R_L > 200MΩ, C_L = 50pF, V_{DD} nominal, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}										
Propogation Delay Times: Clock (Low-to-High) to Any Output, t_{CO}	$\overline{Enable}$ = 0		5	–	150	225	–	150	225	ns
			10	–	75	125	–	–	–	
$\overline{Enable}$ to Any Output, t_{EO} [4]	Clock = 1		5	–	125	225	–	125	225	ns
			10	–	65	100	–	–	–	
Memory Address to All Outputs, t_{IO}	Clock = 1		5	–	150	225	–	150	225	ns
	$\overline{Enable}$ = 0		10	–	75	125	–	–	–	
Propogation Delay Times: Clock (Low-to-high) to A8, A9, $\overline{A8}$, or $\overline{A9}$, t_{CO}			5	–	125	200	–	125	200	ns
			10	–	65	100	–	–	–	
Clock (Low-to-High) to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$, t_{CO}	$\overline{Enable}$ = 0		5	–	175	275	–	175	275	ns
			10	–	90	140	–	–	–	
Enable to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$, t_{EO} [4]			5	–	125	225	–	125	225	ns
			10	–	65	100	–	–	–	
MA0, MA1 to A8, A9, $\overline{A8}$, or $\overline{A9}$, t_{IO}			5	–	100	150	–	100	150	ns
			10	–	50	75	–	–	–	
MA2, MA3 to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$, or $\overline{CE3}$, t_{IO}	Clock = 1		5	–	150	225	–	150	225	ns
	$\overline{Enable}$ = 0		10	–	75	125	–	–	–	

*Typical values are for T_A = 25°C and nominal voltage

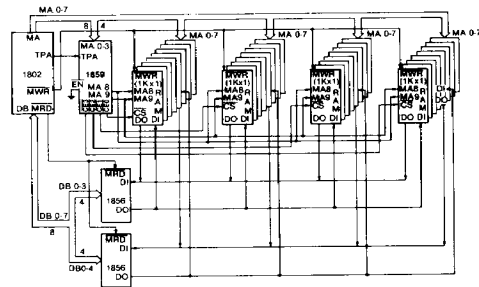
TIMING DIAGRAMS



APPLICATIONS



4K x 8 memory system using 1858 and 1822s



4K x 8 memory system design using 1859 and 1K x 1 RAMs

SIGNAL DESCRIPTION

MA 0 – MA 3: 4 Bit Address inputs. MA 0 is the least significant input address bit and MA 3 is the most significant input address bit.

CLOCK: The MA 0 – MA 3 address bits are latched at the high to low transition of Clock input (TPA) in the 1858 and the 1859.

The 1858 and the 1859 can also be used in general purpose memory system application with a non-multiplexed address bus by connecting the Clock input to V_{DD}.

$\overline{\text{ENABLE}}$: In the 1858, when $\overline{\text{Enable}}$ = V_{DD}, the CS outputs = V_{SS} and the $\overline{\text{CE}}$ outputs = V_{DD}. When $\overline{\text{Enable}}$ = V_{SS}, the outputs are enabled and correspond to the binary decode of the inputs. The $\overline{\text{Enable}}$ input can be used for memory system expansion.

In the 1859, when $\overline{\text{Enable}}$ = V_{DD}, the $\overline{\text{CE}}$ outputs = V_{DD}; when $\overline{\text{Enable}}$ = V_{SS}, $\overline{\text{CE}}$ outputs are enabled and correspond to the binary decode of the MA 3 and MA 2 inputs. Enable does not affect the latching or state of outputs A 8, $\overline{\text{A 8}}$, A 9, or $\overline{\text{A 9}}$.

A 8, $\overline{\text{A 8}}$, A 9, $\overline{\text{A 9}}$: These outputs represent the non-inverted and inverted state of the latched address inputs, MA 0 and MA 1, in the 1859.

$\overline{\text{CE 0}}$ – $\overline{\text{CE 3}}$, CS 0 – CS 3: Decoded outputs. The decoding is shown in the truth tables below.

TRUTH TABLES

1858 DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		CS0	CS1	CS2	CS3	$\overline{\text{CE0}}$	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{CE3}}$
	MA1	MA0								
0	0	0	1	0	0	0	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	0	0				
0	1	0	0	0	1	0				
0	1	1	0	0	0	1				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	0	0	0	0	1	1	1	1

X = MA0, MA1, MA2, MA3 DON'T CARE

1859 DECODE TRUTH TABLE

$\overline{\text{ENABLE}}$	DATA INPUTS		A8	A9	$\overline{\text{A8}}$	$\overline{\text{A9}}$	$\overline{\text{CE0}}$	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	$\overline{\text{CE3}}$
	MA0	MA1								
0	0	0	0	0	1	1	NOT AFFECTED BY MA1, MA0			
0	0	1	0	1	1	0				
0	1	0	1	0	0	1				
0	1	1	1	1	0	0				
	MA3	MA2								
0	0	0	NOT AFFECTED BY MA3, MA2				0	1	1	1
0	0	1					1	0	1	1
0	1	0					1	1	0	1
0	1	1					1	1	1	0
1	X	X	NOT AFFECTED BY ENABLE				1	1	1	1

X = MA0, MA1, MA2, MA3 DON'T CARE

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12/88
Printed in U.S.A.