HARRIS Semiconductor

HI-516

August 1997

16-Channel/Differential 8-Channel, CMOS High Speed Analog Multiplexer

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
  - $I_{S(OFF)}$ 10pA
  - $I_{D(OFF)}$ 30pA
- Low Capacitance (Max)
  - $C_{S(OFF)}$ 10pF
  - $C_{D(OFF)}$ 25pF
- Off Isolation at 500kHz . . . . . 55dB (Min)
- Low Charge Injection Error 20mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

The HI-516 is a monolithic, dielectrically isolated, high-speed, high-performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-Channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-Channel differential multiplexer by connecting A_3 to the V-supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_{DOFF} < 100pA at 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

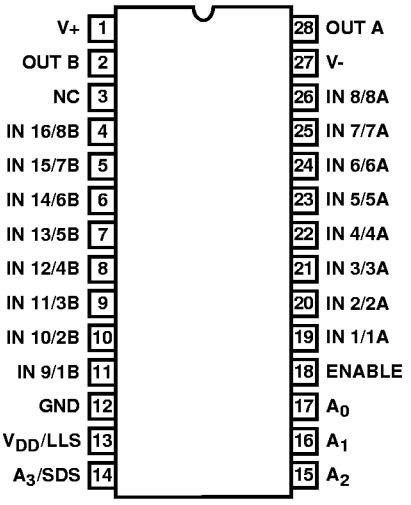
For MIL-STD-883 compliant parts, request the HI-516/883 data sheet.

Ordering Information

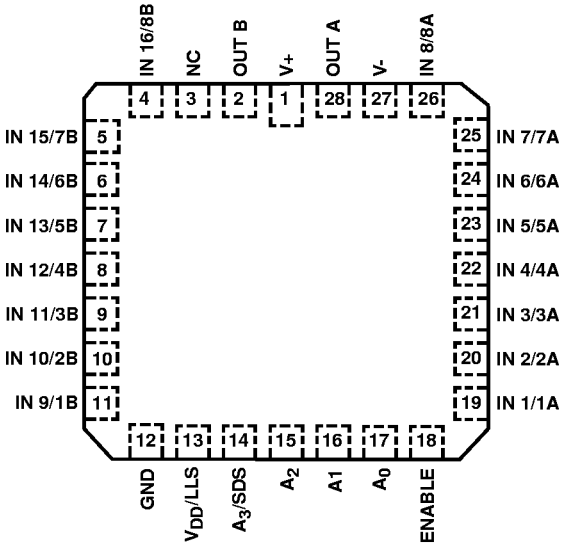
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI4P0516-5	0 to 75	28 Ld PLCC	N28.45
HI3-0516-5	0 to 75	28 Ld PDIP	E28.6
HI1-0516-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0516-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0516-8	-55 to 125	28 Ld CERDIP	F28.6
HI4-0516-8	-55 to 125	28 Ld CLCC	J28.A
HI1-0516/883	-55 to 125	28 Ld CERDIP	F28.6
HI4-0516/883	-55 to 125	28 Ld CLCC	J28.A

Pinouts

HI-516 (CERDIP, PDIP)
TOP VIEW



HI-516 (CLCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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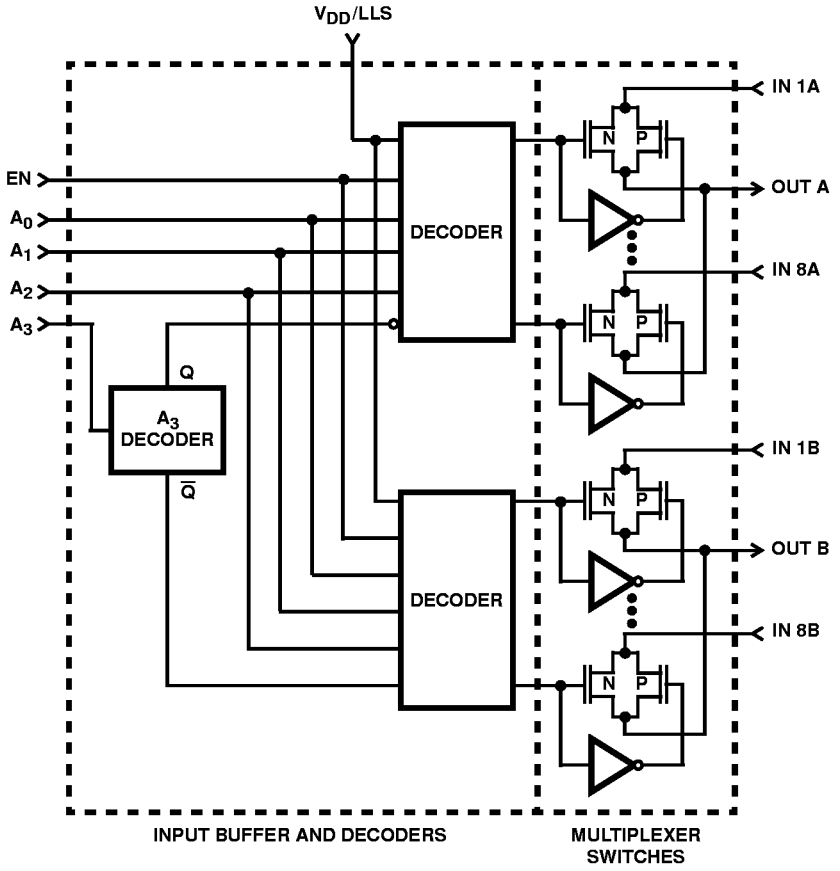
File Number **3146.1**

Functional Block Diagram



A_3 DECODE		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 33V
Analog Input Voltage
$+V_{IN}$ . . . . . $+V_{SUPPLY}$ +2V
$-V_{IN}$ . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
$+V_A$ . . . . . +6V
$-V_A$ . . . . . -6V
$+A_3$/SDS . . . . . $+V_{SUPPLY}$ +2V
$-A_3$/SDS . . . . . $-V_{SUPPLY}$ -2V
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
$+V_A$ . . . . . $+V_{SUPPLY}$ +2V
$-V_A$ . . . . . -2V

Operating Conditions

Temperature Ranges
HI-516-2,-8 . . . . . -55^oC to 125^oC
HI-516-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	60	N/A
PLCC Package	70	N/A
CERDIP Package	55	18
CLCC Package	70	20

Maximum Junction Temperature
CERDIP, CLCC Packages . . . . . 175^oC
PDIP, SOIC, PLCC Packages . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HI-516-2, -8			HI-516-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_I	Note 2	Full	-14	-	+14	-15	-	+15	V
On Resistance, r_{ON}	Note 3	25	-	620	750	-	620	750	Ω
		Full	-	-	1,000	-	-	1,000	Ω
Off Input Leakage Current, $I_{S(OFF)}$		25	-	0.01	-	-	0.01	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		25	-	0.03	-	-	0.03	-	nA
		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$		25	-	0.04	-	-	0.04	-	nA
		Full	-	-	100	-	-	100	nA
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL} (TTL)		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (TTL)		Full	2.4	-	-	2.4	-	-	V
Input Low Threshold, V_{AL} (CMOS)		Full		-	$0.3V_{DD}$	-	-	$0.3V_{DD}$	V
Input High Threshold, V_{AH} (CMOS)		Full	$0.7V_{DD}$	-	-	$0.7V_{DD}$	-	-	V
Input Leakage Current, I_{AH} (High)		Full	-	-	1	-	-	1	µA
Current, I_{AL} (Low)		Full	-	-	25	-	-	25	µA
SWITCHING CHARACTERISTICS									
Access Time, t_A		25	-	130	175	-	130	175	ns
		Full	-	-	225	-	-	225	ns
Break-Before-Make Delay, t_{OPEN}		25	10	20	-	10	20	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	120	175	-	120	175	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	140	175	-	140	175	ns
Settling Time 0.1%		25	-	250	-	-	250	-	ns
0.01%		25	-	800	-	-	800	-	ns

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-516-2, -8			HI-516-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Charge Injection Error	Note 4	25	-	-	20	-	-	20	mV
Off Isolation	Note 5	25	55	-	-	55	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	-	10	-	-	10	pF
Channel Output Capacitance, $C_{D(OFF)}$		25	-	-	25	-	-	25	pF
Digital Input Capacitance, C_A		25	-	-	10	-	-	10	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.02	-	-	0.02	-	pF
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	750	-	-	900	mW
I+, Current	Note 6	Full	-	-	25	-	-	30	mA
I-, Current	Note 6	Full	-	-	25	-	-	30	mA

NOTES:

1. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
2. At temperatures above 90°C, care must be taken to assure V_{IN} remains at least 1V below the V_{SUPPLY} for proper operation.
3. V_{IN} = ±10V, I_{OUT} = -100µA.
4. V_{IN} = 0V, C_L = 100pF, enable input pulse = 3V, f = 500kHz.
5. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1K, Pin 3 grounded.
6. V_{EN} = +2.4V.

TRUTH TABLE HI-516 Used as a 16-Channel Multiplexer or 8-Channel Differential Multiplexer (Note 1)

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

NOTE:

1. For 16-channel single-ended function, tie 'out A' to 'out B'; for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

TRUTH TABLE HI-516 Used as a DIfferential 8-Channel Multiplexer

A_3 CONNECT TO V- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

Test Circuits and Waveforms

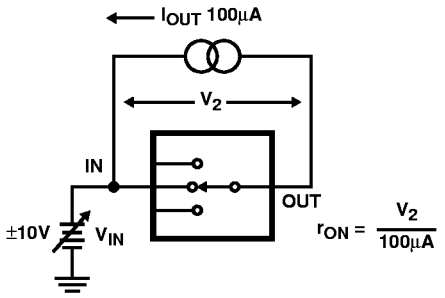


FIGURE 1. ON RESISTANCE vs INPUT SIGNAL LEVEL

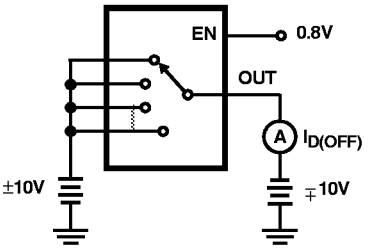


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

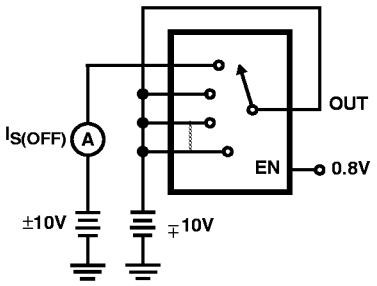


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

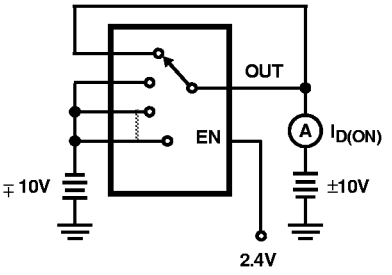


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

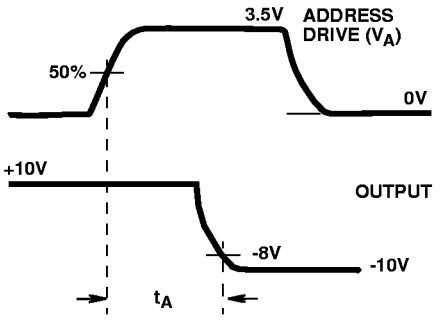


FIGURE 5A.

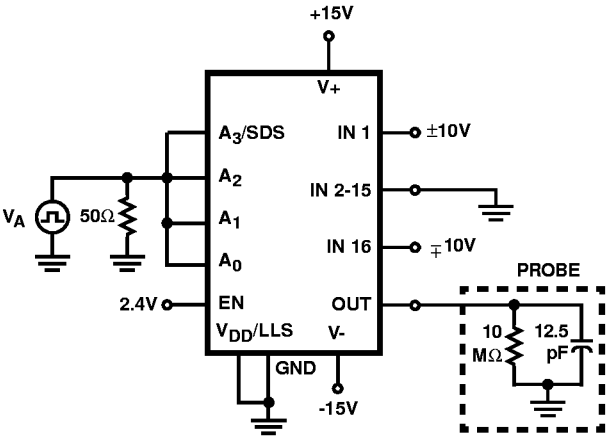


FIGURE 5B.

FIGURE 5. ACCESS TIME

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

Test Circuits and Waveforms (Continued)

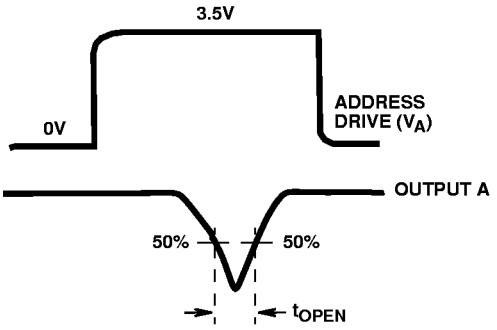


FIGURE 6A. ENABLE DRIVE

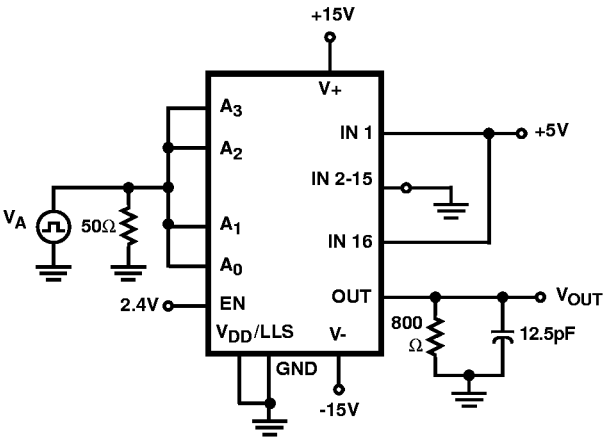


FIGURE 6B.

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

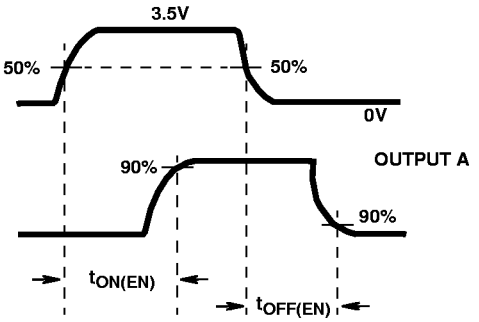


FIGURE 7A. ENABLE DRIVE

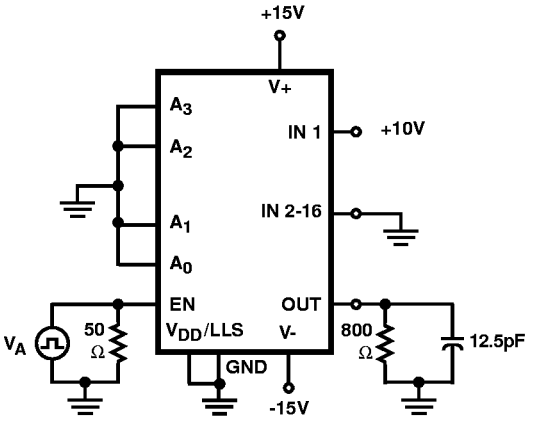


FIGURE 7B.

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

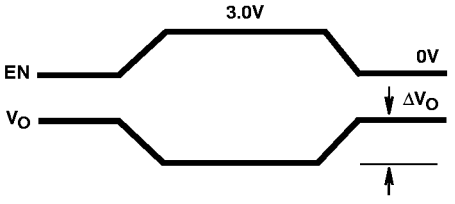


FIGURE 8A.

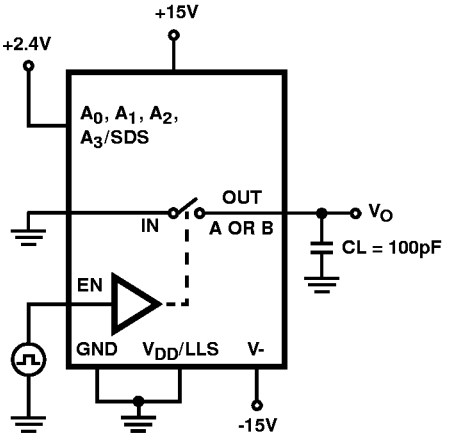


FIGURE 8B.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:

2250µm x 3720µm x 485µm ±25µm

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.64×10^5 A/cm^2

Metallization Mask Layout

HI-516