HI-REL DATA SHEET

HM 65162

2 k x 8
VERY LOW POWER CMOS SRAM

FEATURES

- ACCESS TIME : 70/85 ns
- VERY LOW POWER CONSUMPTION
  ACTIVE : 240 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

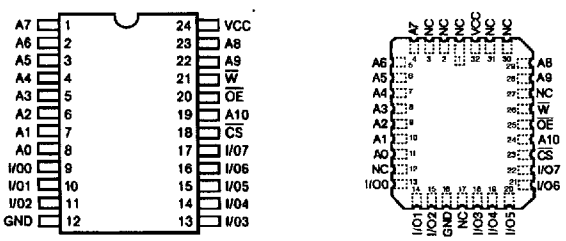
DESCRIPTION

The HM 65162 is a very low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.
The HM 65162 is a "Pure CMOS SRAM" utilizing an array of six transistor (6T) memory cell permitting the lowest possible standby supply current over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise and alpha particles, and in addition improves the tolerance of the RAM to cumulated dose radiation.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate thus making the HM 65162 "Latch-up immune".
All inputs and outputs of the HM 65162 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65162 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

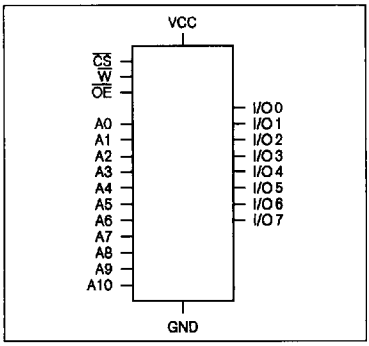
PACKAGES

Ceramic 600 mils, 24 pins, DIL. LCC, 32 pins.

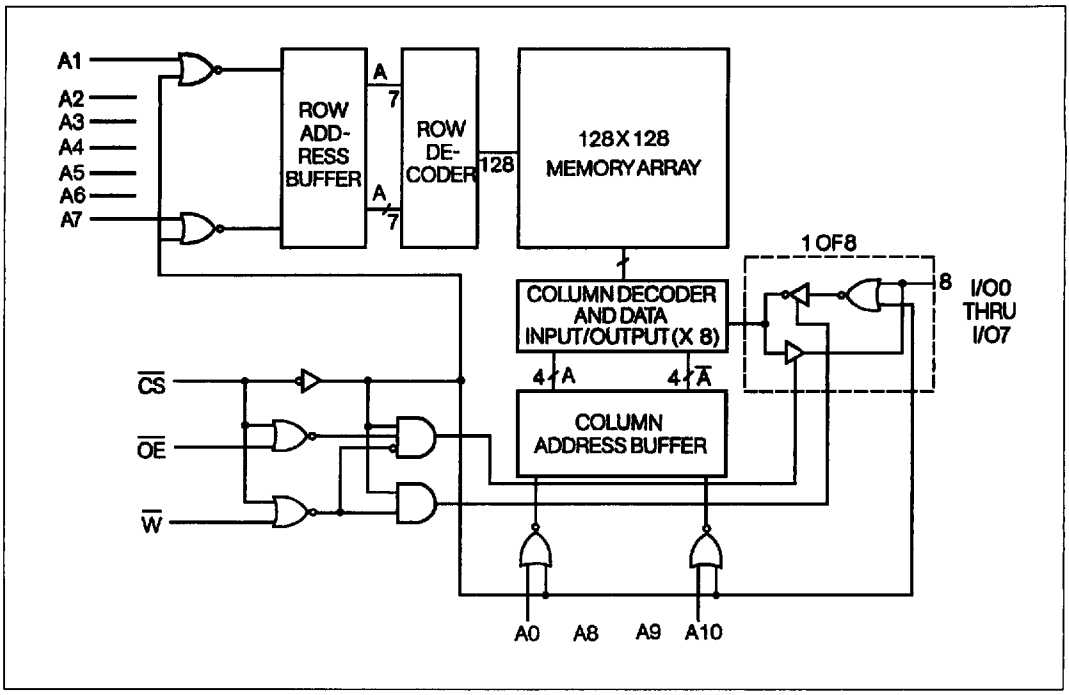
Pinout DIL 24 pins (top view) , **Pinout LCC 32 pins (top view)**



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A10 : Address inputs	$\overline{CS}$: Chip Select
I/O0-I/O7 : Input/Output	$\overline{OE}$: Output Enable
Vcc : Power	$\overline{W}$: Write enable
GND : Ground	

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	INPUTS/OUTPUTS	MODE
H	X	X	Z	Deselect/Power down
L	L	H	Data out	Read
L	X	L	Data in	Write
L	H	H	Z	Deselect

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
Input or Output voltage applied : (GND - 0.3 V) to (Vcc + 0.3 V)
Storage temperature : - 65°C to + 150°C
Electro static discharge voltage > 1500 V (MIL STD 883, METHOD 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	Vcc = 5 V ± 10 %	- 55°C to + 125°C
Industrial	Vcc = 5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65162 B	65162	65162 C	Unit	Value	Note 8
ICCSB (1)	Standby supply current	5	5	5	mA	Max	M
ICCSB1 (2)	Standby supply current	50	50	500	µA	Max	M
ICCOP (3)	Operating supply current	70	70	70	mA	Max	M
ICC (4)	Operating supply current	70	70	70	mA	Max	M
II/O (5)	Input/Output leakage current	+ / - 1	+ / - 1	+ / - 1	µA	Max	M
VIL (6)	Input low voltage	0.8	0.8	0.8	V	Max	T
VIH (6)	Input high voltage	2.2	2.2	2.2	V	Min	T
VOL (7)	Output low voltage	0.4	0.4	0.4	V	Max	M
VOH (7)	Output high voltage	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	pF	Max	G

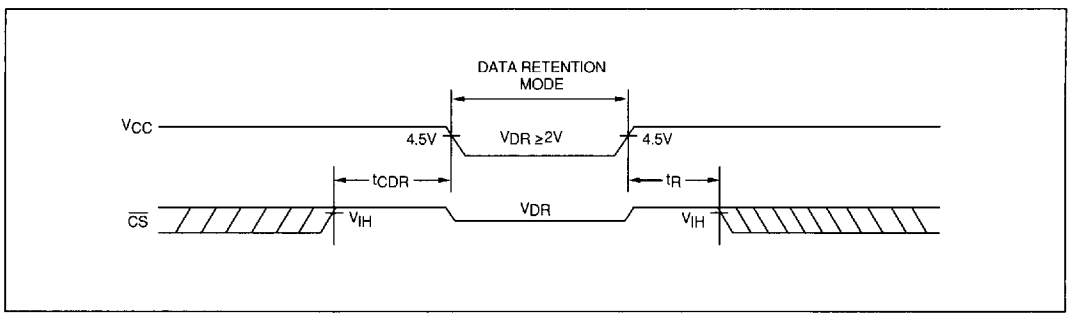
Notes :
1. $\overline{CS}$ > = VIH, I = Industrial temperature range, M = Military temperature range
2. $\overline{CS}$ > = Vcc - 0.3V, Output current = 0 mA
3. Vcc max, Iout = 0 mA, Duty cycle 100 %, F = 1 MHz and 5 mA / MHz, Vin = Vcc / Gnd
4. $\overline{CS}$ ≤ VIL, Iout = 0 mA, Vin = Gnd to Vcc
5. Vcc = 5.5V, Vin = Gnd to Vcc
6. VIH max = Vcc + 0.3V, VIL min = - 0.3V or - 1V pulse width 50 ns.
7. Vcc min, IOL = 4 mA, IOH = - 1 mA
8. Including open/short test or inputs clamp voltage.
   G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
   M - Measured : Parameter measured and data-log capability.
   T - Tested : Parameter verification during testing.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power down transitions.
4. The RAM can begin operation > 55 ns after Vcc reaches the minimum operating voltage (4.5V).

TIMING



DATA RETENTION MODE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM (I/M)	UNIT	NOTE 8
VCCDR	Vcc for data retention	2.0	—	—	V	T
TCDR	Chip deselect to data retention time	0.0	—	—	ns	
TR	Operation recovery time	TAVAV (10)	—	—	ns	
ICCDR1 (11)	Data retention current 2.0 V : HM-65162(B) 2.0 V : HM-65162C	 — —	 0.1 0.1	 3/20.0 30/200.0	 µA µA	 M M
ICCDR2 (11)	Data retention current 3.0 V : HM-65162(B) 3.0 V : HM-65162C	 — —	 0.3 0.3	 3/30 50/300.0	 µA µA	 G G

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

ELECTRICAL CHARACTERISTICS
AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

Conditions :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
VCC : 5 V ± 10 %

Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

WRITE CYCLE : Industrial and military specification

SYMBOL	PARAMETER *	65162 B	65162	65162 C	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	50	65	65	ns	min
TDVWH	Data set-up time	30	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	40	50	50	ns	max
TWLWH	Write pulse width	40	55	55	ns	min
TWHAX	Address hold to end of write	10	10	10	ns	min
TWHDX	Data hold time	10	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

READ CYCLE : Industrial and military specification

SYMBOL	PARAMETER *	65162 B	65162	65162 C	UNIT	VALUE
TAVAV	READ cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	50	50	ns	max
TGLQV	Output Enable access time	50	65	65	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	40	40	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

* : All parameters only tested and screened during full speed functional test.
For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = OV and VIH = 3V.

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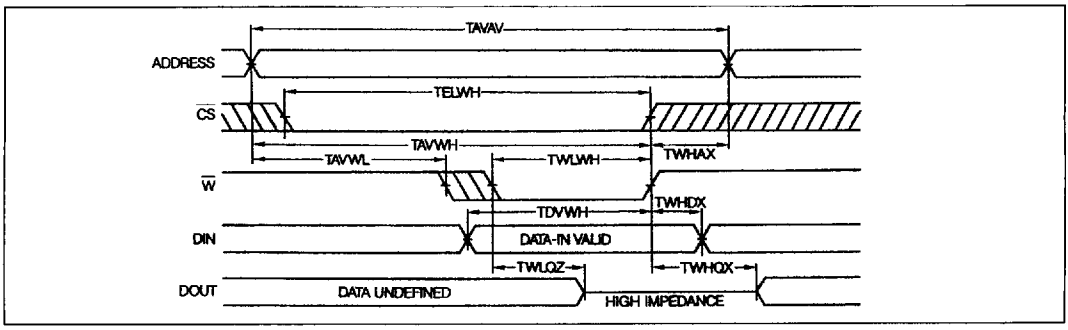
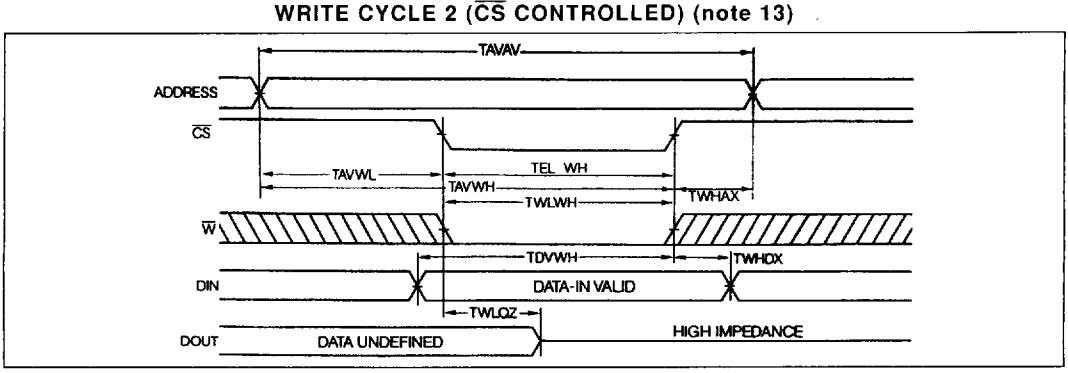
WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (note 13)

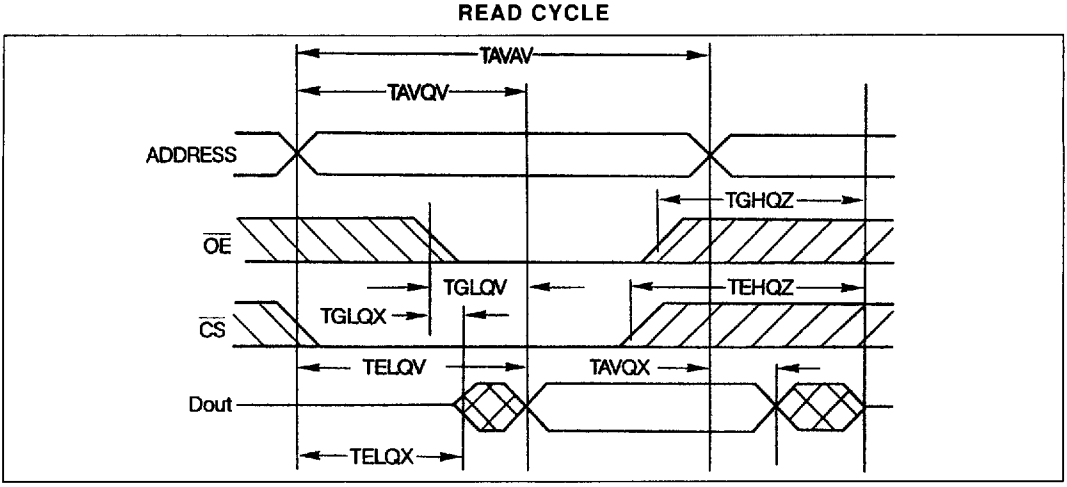


WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (note 13)



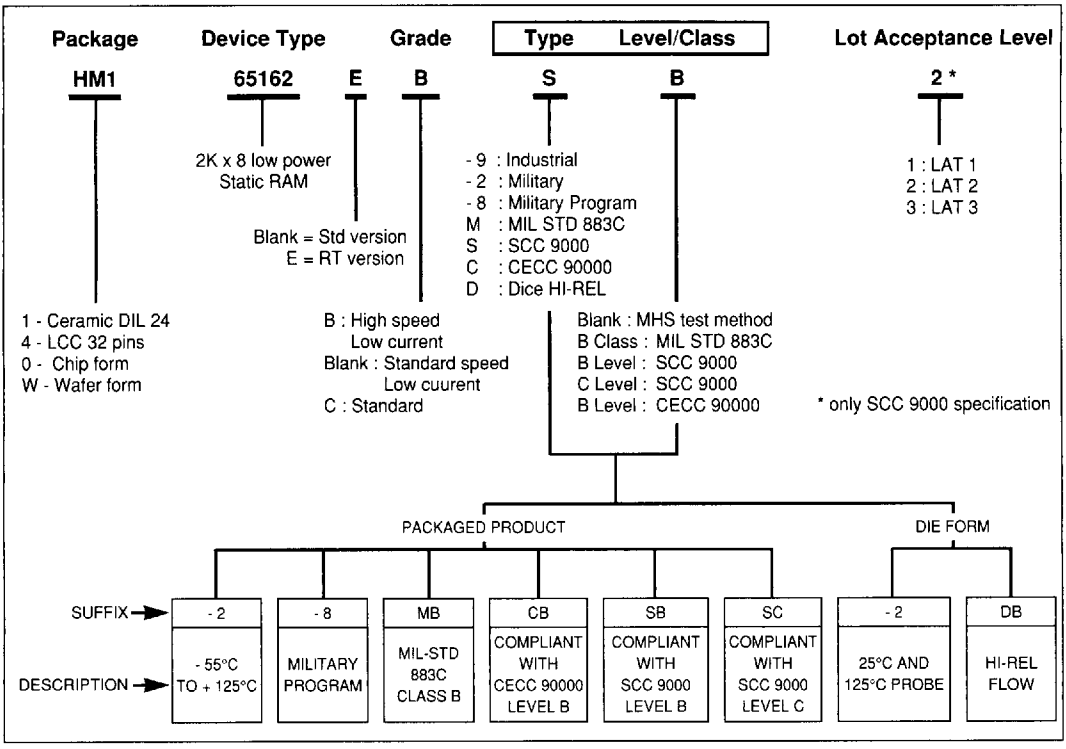
Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.

READ CYCLE

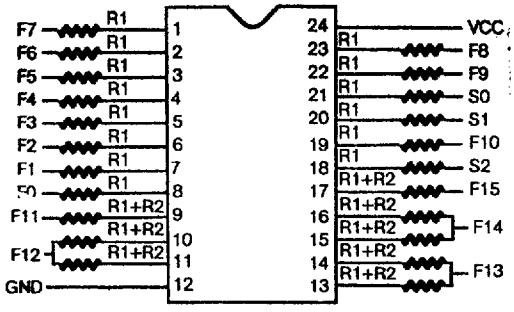


Addresses must remain stable for the duration of the read cycle. The read $\overline{OE}$ and $\overline{CS}$ must be < VIL and $\overline{W}$ VIH. The output buffers can be controlled independently by $\overline{OE}$ while $\overline{CS}$ is low. To execute consecutive read cycles. $\overline{CS}$ may be tied low continuously until all desired locations are accessed. When $\overline{CS}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

ORDERING INFORMATION



BURN IN SCHEMATICS



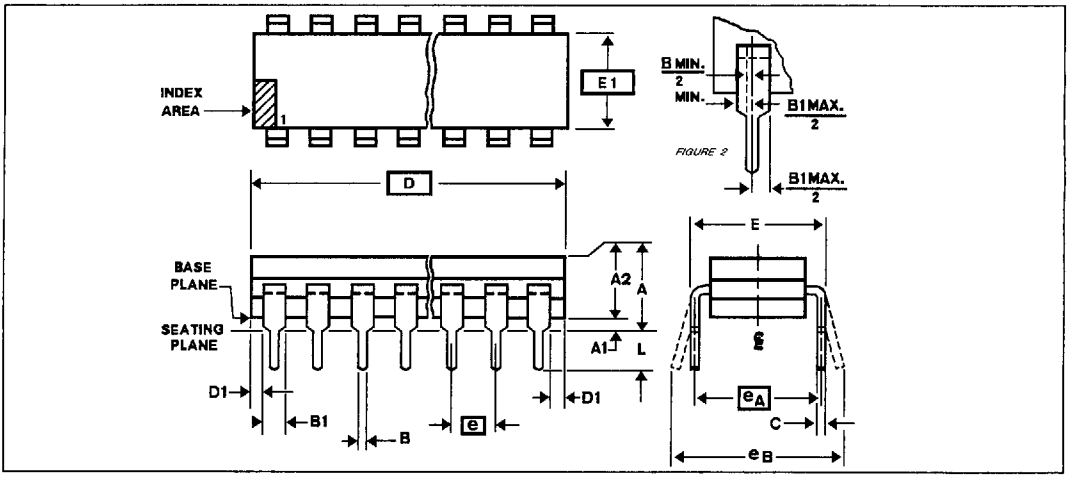
R1 = 1K Ω
R2 = 2.2K Ω

Fo = 25 HKz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write / read cycle

VCC = 5.5V

PACKAGE OUTLINES



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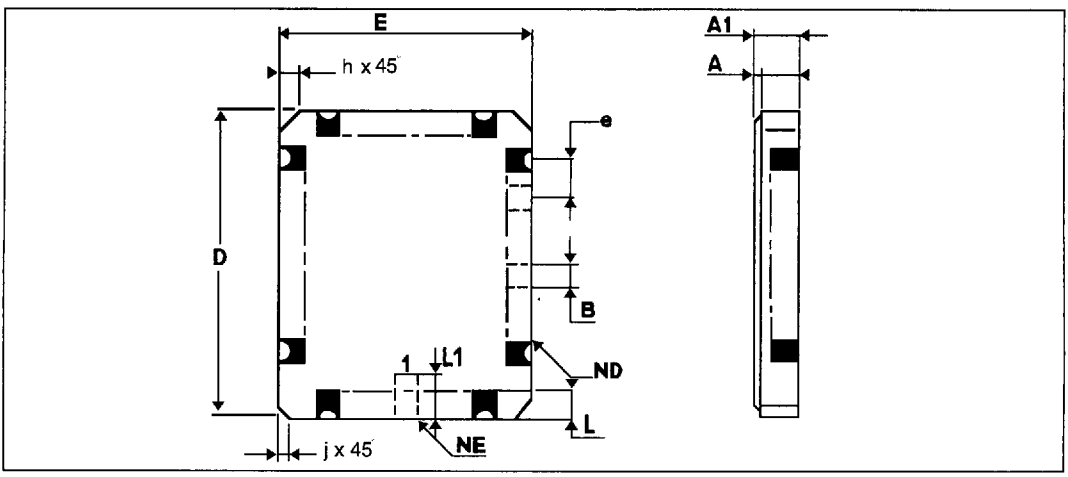
24 PINS CERDIP .600

		A	A1	A2	B	B1	C	D	E	E1	e	eA	eB	L	D1
MM	MIN	—	0.39	2.92	0.36	1.14	0.20	31.50	15.36	13.05	2.54	15.24	—	3.17	0.13
	MAX	5.33	—	4.95	—	1.78	0.38	32.51	15.62	13.66	BSC	BSC	17.27	5.08	—
INCHES	MIN	—	.015	.115	.014	.045	.008	1.240	.605	.514	.100	.600	—	.125	.005
	MAX	.210	—	.195	—	.070	.015	1.280	.615	.538	BSC	BSC	.680	.200	—



32 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	L	L1	ND	NE
MM	MIN	1.37	1.62	0.635	13.81	11.30	1.27	1.016	0.51	1.14	1.8	9	7
	MAX	1.93	2.23	TYP	14.22	11.63	BSC			1.4	2.11		
INCHES	MIN	.054	.064	.025	.544	.445	.050	.040	.020	.045	.077	9	7
	MAX	.076	.088	TYP	.560	.458	BSC			.055	.083		