MATRA M H S

January 1991

HI-REL DATA SHEET

HM 65664

8 k x 8
ULTIMATE CMOS SRAM

FEATURES

- ACCESS TIME : 35*/45/55 ns
- VERY LOW POWER CONSUMPTION
  ACTIVE : 175.0 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 AND 600 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPLLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

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* Preliminary

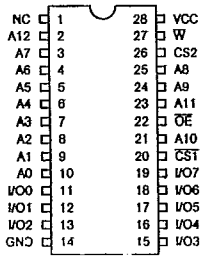
DESCRIPTION

The HM 65664 is a very low power CMOS static RAM organized as 8192 x 8 bits. It is manufactured using the MHS high performance CMOS technology named SCMOS.
With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics or the portable instruments or embarked systems. Utilizing an array of six transistors (6T) memory cells, the HM 65664 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.
The HM 65664 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

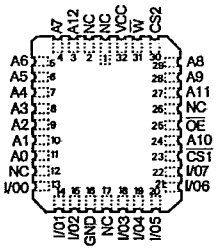
PACKAGES

Ceramic 300 & 600 mils, 28 pins, DIL. LCC, 32 pins.

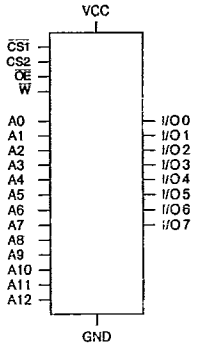
Pinout DIL 28 pins (top view)



Pinout LCC 32 pins (top view)



LOGIC SYMBOL



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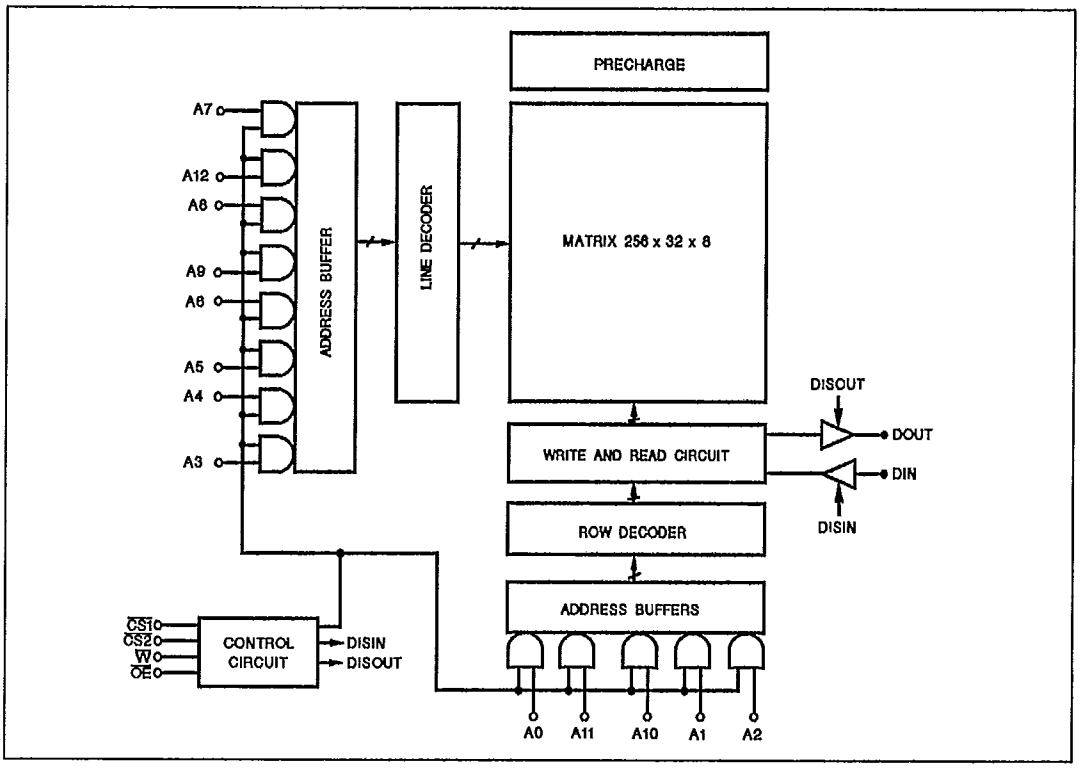
BLOCK DIAGRAM



PIN NAMES

A0-A12 : Address inputs	$\overline{CS1}$: Chip-Select 1
I/O0-I/O7 : Input/Output	CS2 : Chip-Select 2
Vcc : Power	$\overline{OE}$: Output Enable
Gnd : Ground	$\overline{W}$: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	INPUTS/OUTPUTS	MODE
H	X	X	X	Z	Deselect/Power down
L	H	L	H	Data out	Read
L	H	X	L	Data in	Write
L	H	H	H	Z	Output disable

L = low, H = high, X = H or L, Z = high impedance.

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ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)
Storage temperature : - 65°C to + 150°C
Electro static discharge voltage > 2000 V (MIL STD 883, METHOD 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	Vcc = 5 V ± 10 %	- 55°C to + 125°C
Industrial	Vcc = 5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65664 Q	65664 B	65664 S	65664	65664 C	Unit	Value	Note 8
ICCSB (1)	Standby supply current	20	15	20	15	20	mA	Max	M
ICCSB1 (2)	Standby supply current (I/M)	500	5/50	100/500	5/50	100/500	µA	Max	M
ICCOP (3)	Operating supply current	100	75/70	100	75	100	mA	Max	M
ICC (4)	Operating supply current	20	15	20	15	20	mA	Max	M
II/O (5)	Input/Output leakage current	± 1	± 1	± 1	± 1	± 1	µA	Max	M
VIL (6)	Input low voltage	0.8	0.8	0.8	0.8	0.8	V	Max	T
VIH (6)	Input high voltage	2.2	2.2	2.2	2.2	2.2	V	Min	T
VOL (7)	Output low voltage	0.4	0.4	0.4	0.4	0.4	V	Max	M
VOH (7)	Output high voltage	2.4	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	8	8	8	8	8	pF	Max	G
C OUT	Output capacitance	8	8	8	8	8	pF	Max	G

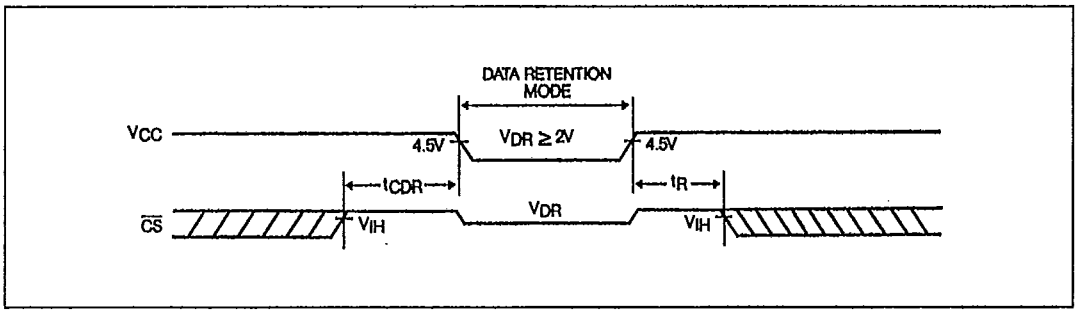
Notes :
1. $\overline{CS1}$ > = VIH, CS2 < VIL
2. $\overline{CS1}$ > = Vcc - 0.3V, CS2 < = 0,3V, Output current = 0 mA, I = Industrial / M = Military
3. Vcc max, Iout = 0 mA, Duty cycle 100 %, F = max, Vin = Vcc / Gnd
4. $\overline{CS1}$ < = VIL, CS2 > ≡ VIH, Iout = 0 mA, Vin = Gnd to Vcc
5. Vcc = 5.5V, Vin = Gnd to Vcc
6. VIH max = Vcc + 0.3V, VIL min = - 0.3V or - 1V pulse width 50 ns.
7. Vcc min, IOL = 4 mA, IOH = - 1 mA
8. Including open/short test or inputs clamp voltage.
   G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
   M - Measured : Parameter measured and data-log capability.
   T - Tested : Parameter verification during testing.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power down transitions.
4. The RAM can begin operation > 45 ns after Vcc reaches the minimum operating voltage (4.5V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM (12)	UNIT	NOTE 8
VCCDR	Vcc for data retention	2.0	—	—	V	T
TCDR	Chip deselect to data retention time	0.0	—	—	ns	
TR	Operation recovery time	TAVAV (10)	—	—	ns	
ICCDR1 (11)	Data retention current @ 2.0 V : HM-65664 (B)- HM-65664 S/C/Q	 — —	 0.1 0.1	 3/20.0 30/200.0	 µA µA	 M M
ICCDR2 (11)	Data retention current @ 3.0 V : HM-65664 (B)- HM-65664 S/C/Q	 — —	 0.3 0.3	 3/30 50/300.0	 µA µA	 G G

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.
12. I = Industrial / M = Military

ELECTRICAL CHARACTERISTICS
AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

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Conditions :

Input pulse levels : GND to 3.0 V
Input rise : 5 ns
VCC : 5 V ± 10 %

Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 30 pF

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER *	65664 Q	65664 B	65664 S	65664	65664 C	UNIT	VALUE
TAVAV	Write cycle time	35	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	35	45	45	55	55	ns	min
TDVWH	Data set-up time	22	25	25	25	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	35	45	45	55	55	ns	min
TEH2WH	CS2 low to write end	35	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	15	15	15	20	20	ns	max
TWLWH	Write pulse width	30	40	40	50	50	ns	min
TWHAX	Address hold to end of write	5	5	5	5	5	ns	min
TWHDX	Data hold time	3	3	3	3	3	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

* : All parameters only tested and screened during full speed functional test.
For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = OV and VIH = 3V.

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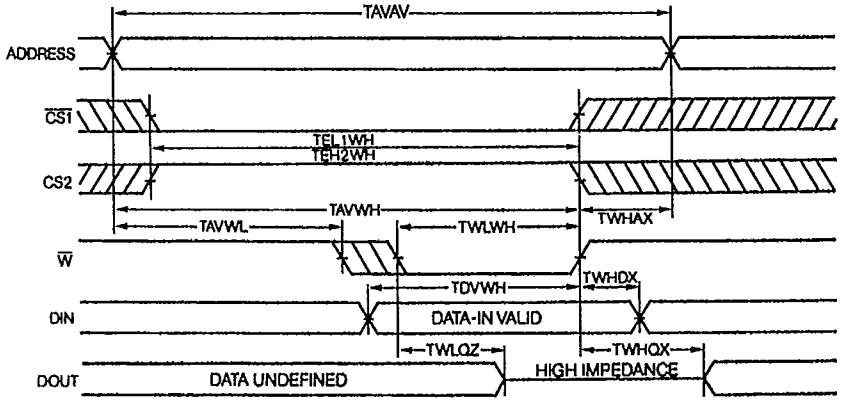
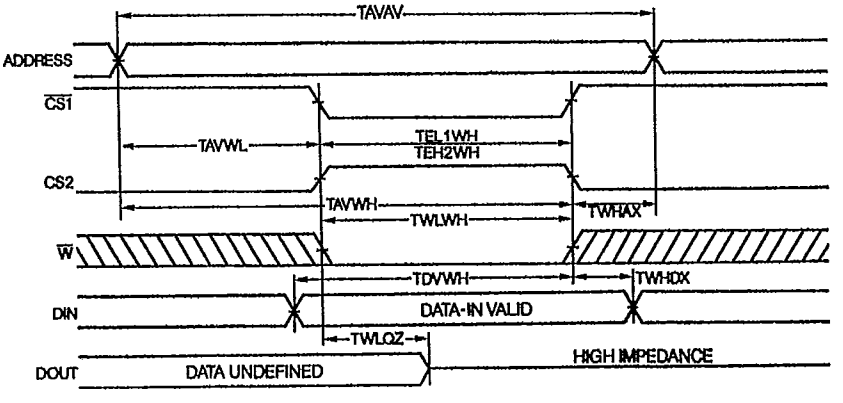
WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 13)



WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 13)



Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER *	65664 Q	65664 B	65664 S	65664	65664 C	UNIT	VALUE
TAVAV	Read cycle time	35	45	45	55	55	ns	min
TAVQV	Address access time	35	45	45	55	55	ns	max
TAVQX	Address Valid to low Z	3	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	35	45	45	55	55	ns	max
THL2QV	Chip-select 2 access time	35	45	45	55	55	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	5	ns	min
TEH2QX	CS2 high to low Z	5	5	5	5	5	ns	min
TEH1QZ	$\overline{CS1}$ high to high Z	35	45	45	55	55	ns	max
TEL2QZ	CS2 low to high Z	35	45	45	55	55	ns	max
TGLQV	Output Enable access time	15	15	15	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	15	15	15	20	20	ns	max

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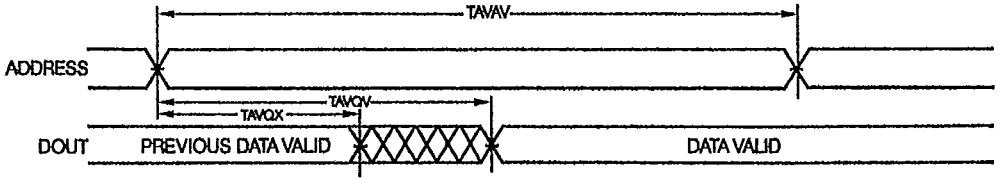
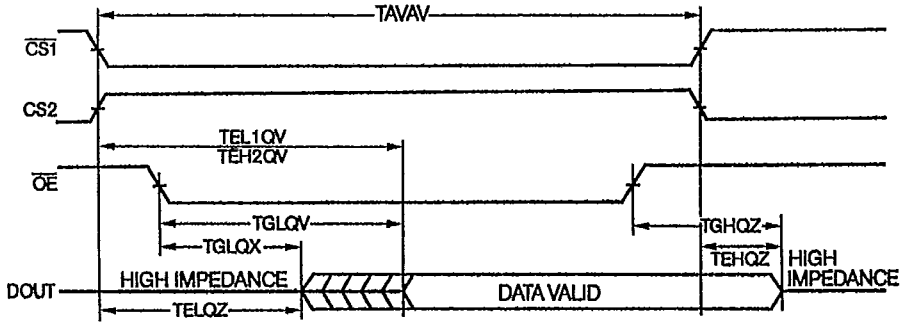
* : All parameters only tested and screened during full speed functional test.
For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = OV and VIH = 3V.

READ CYCLE nb 1 (notes 16, 17)



READ CYCLE nb 2 (notes 16, 18)



Notes : 16. $\overline{W}$ is high for read cycle
17. Device is continuously selected, $\overline{CS1}$ & $\overline{OE}$ = VIL and CS2 = VIH
18. Address valid prior to or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

PROCESS FLOW

Package	Device Type	Grade	Type	Level/Class	Lot Acceptance Level
HM1	65664	S	S	B	2 *

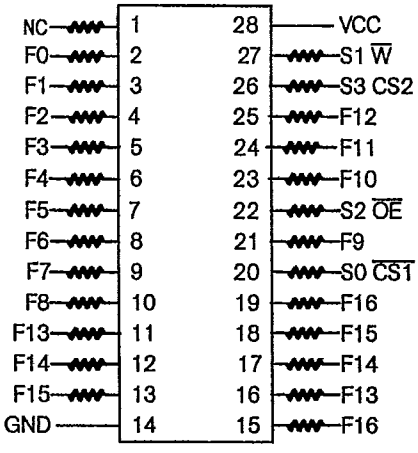
- Device Type 65664: 8K x 8 low power Static RAM
- Grade S:
  - 9 : Industrial
  - 2 : Military
  - 8 : Military Program
  - M : MIL STD 883C
  - S : SCC 9000
  - C : CECC 90000
  - D : Dice HI-REL
- Lot Acceptance Level 2 *:
  - 1 : LAT 1
  - 2 : LAT 2
  - 3 : LAT 3

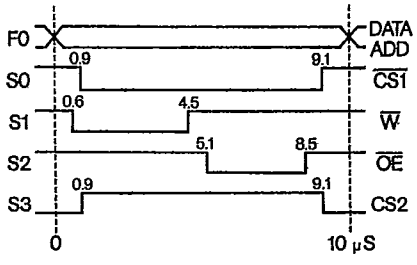
Package	Grade	Level/Class
1 - Ceramic DIL 28 300 mils	B : High speed / Low current	Blank : MHS test method
4 - LCC 32 pins	S : High speed / Medium current	B Class : MIL STD 883C
0 - Chip form	Blank : Medium speed / Low current	B Level : SCC 9000
W - Wafer form	C : Medium speed / Medium current	C Level : SCC 9000
1E - Ceramic DIL 28 600 mils	Q : Very high speed / Medium current	B Level : CECC 90000

* Only SCC 9000 specification

	PACKAGED PRODUCT						DIE FORM	
SUFFIX →	- 2	- 8	MB	CB	SB	SC	- 2	DB
DESCRIPTION →	- 55°C TO + 125°C	MILITARY PROGRAM	MIL-STD 883C CLASS B	COMPLIANT WITH CECC 90000 LEVEL B	COMPLIANT WITH SCC 9000 LEVEL B	COMPLIANT WITH SCC 9000 LEVEL C	25°C AND 125°C PROBE	HI-REL FLOW

BURN IN SCHEMATICS

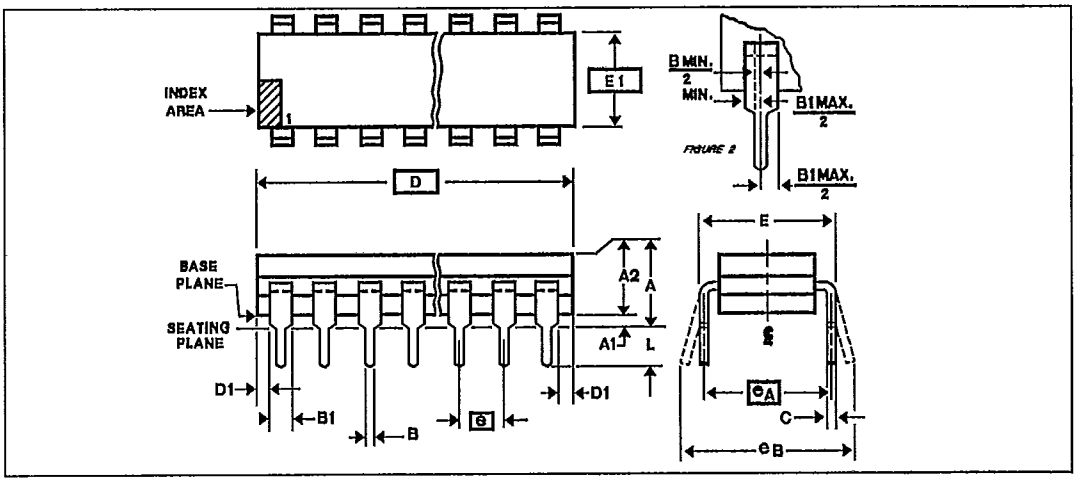




VCC = 5 V (- 0, + 0.5)
R = 1 KΩ per pin
Fo = 50 KHz ± 20 %

Fn = 1/2 F n-1
S0 to S3 : programmable signals for write / read cycles
NC = Not connected

PACKAGE OUTLINES



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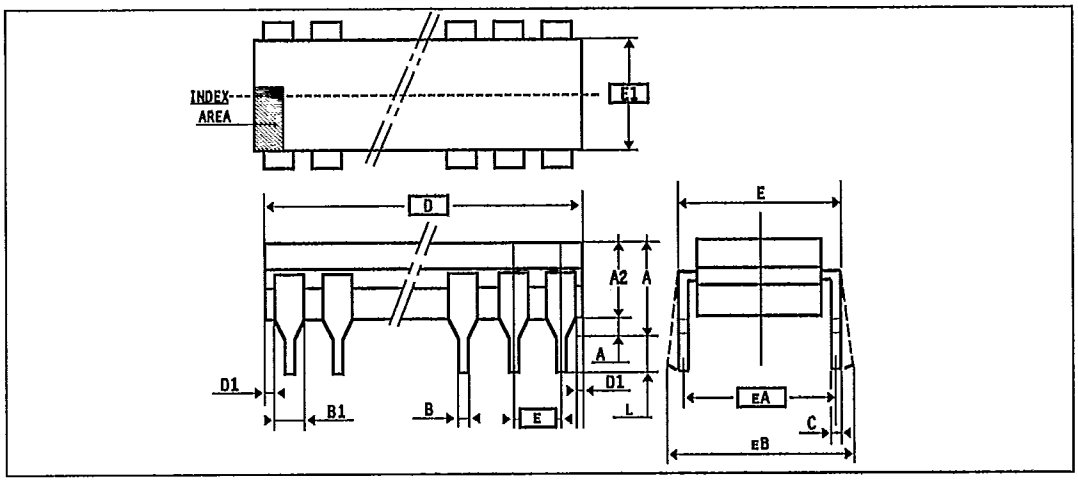
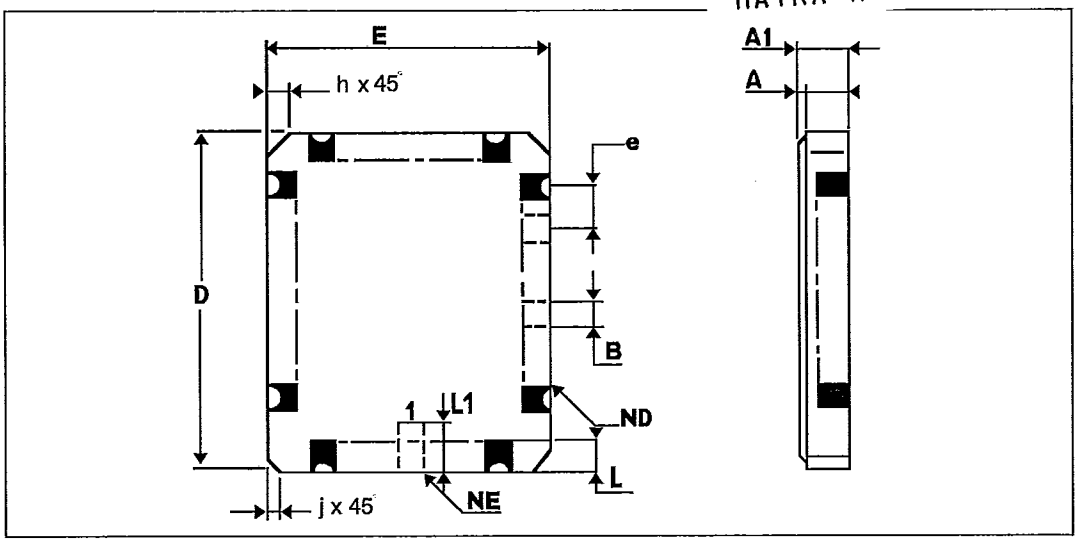
28 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.38	2.92	0.36	1.14	0.20	36.58	0.13	7.62	6.10	2.54	7.62	—	3.05
	MAX	5.84	—	4.95	0.58	1.78	0.38	37.50	—	8.25	7.87	BSC	BSC	11.43	5.08
INCHES	MIN	—	.015	.115	.014	.045	.008	1.440	.005	.300	.240	.100	.300	—	.125
	MAX	.230	—	.195	.023	.070	.015	1.476	—	.325	.310	BSC	BSC	.450	.200



28 LEADS CERDIP .600

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	4.31	0.51	—	0.38	1.27	0.20	36.90	0.25	15.24	13.05	2.54	15.54	—	3.17
	MAX	5.71	1.52	4.57	0.51	1.78	0.38	38.90	—	15.75	13.66	BSC	BSC	17.78	5.08
INCHES	MIN	.170	.020	—	.014	.050	.008	1.452	.010	.600	.514	.100	.600	—	.125
	MAX	.225	.060	.180	.020	.070	.015	1.531	—	.620	.538	BSC	BSC	.700	.200



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32 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	L	L1	ND	NE
MM	MIN	1.37	1.62	0.635	13.81	11.30	1.27	1.016	0.51	1.14	1.8	9	7
	MAX	1.93	2.23	TYP	14.22	11.63	BSC			1.4	2.11		
INCHES	MIN	.054	.064	.025	.544	.445	.050	.040	.020	.045	.077	9	7
	MAX	.076	.088	TYP	.560	.458	BSC			.055	.083		