ECL/TTL GATE ARRAY HM3500

PRELIMINARY PRODUCT DESCRIPTION

The HM3500 (Figure 1) is a 400 picosecond, 3500 equivalent gate density VLSI monolithic integrated circuit using Honeywell's ADB-II™ fabrication process. The array is composed of an uncommitted array of Current-Mode-Logic (CML) gates (Figures 2 and 3), with LSTTL, CML, and ECL 10K/KH and 100K compatible I/O cells.

The HM3500 offers the designer several power supply options (Table 2). This versatility allows the advantage of power programmability while aiding the designer with a more flexible and cost-effective applications fit. To accomplish this, programmable internal voltage reference regulators (8 total) are used to provide the correct internal source currents and signal swings. The programmation of these regulators is performed during the personalization of the gate array and is invisible to the user.

Designing with the HM3500 is easy and fast requiring only conventional logic design, logic simulation, and test pattern generation. The computer-aided-design and autorouting methodologies are similar to those used for printed circuit boards. Up to 3500 gates are autoroutable.

Logic functions are predefined by Honeywell and are implemented by automatically interconnecting the macrocells using three layers of metal routing. Both cell intraconnection and routing of power busses are invisible to the user.

The basic circuit technique used to implement logic functions is a two-level series gated CML structure. This technique gives maximum flexibility and performance in implementing a given function.

Compared to ECL internal gate arrays, the HM3500 with its lower power, higher component density and more efficiently built macrocells results in substantial performance improvement (circuit speed) and space reduction. The increased use of on-chip components reduces system cost.

The ultra-high packing density of the HM3500 offers up to a 150-to-1 reduction in system component count when compared to conventional SSI/MSI ECL or TTL logic functions. The user obtains a degree of optimization like that of a full custom design and the quick turnaround time of a semicustom part.

FEATURES

- **Customer programmable VLSI**
- **3500 equivalent (OR/NOR) gates**
- **Programmable power supply voltages**
- **Available radiation hardened to strategic levels**
- **120 LSTTL, CML, or ECL compatible I/O cells**
- **Internal gate delay: 0.40 ns typical**
- **Operating temperature ranges**
  - **—Commercial: 0 to +70°C (Ta)**
  - **—Military: -55 to +125°C (Tc)**
- **Power dissipation: 3.5 watts typical**
- **Series gated CML internal logic functions**
- **Available packaging includes:**
  - **—152 pin grid array**
  - **—High pincount surface mounted packages**

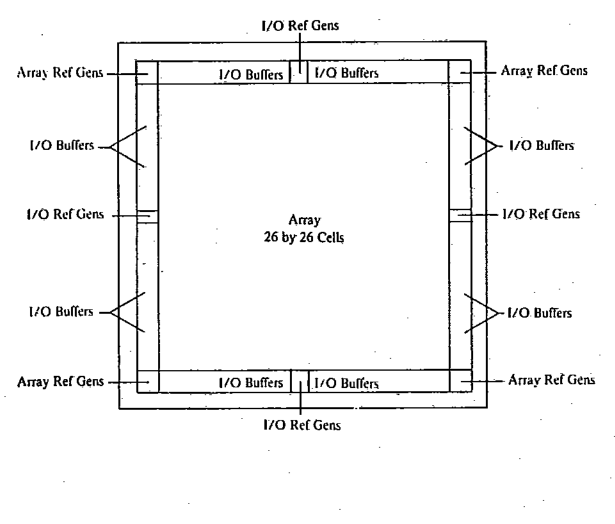

Figure 1. HM3500 Block Diagram

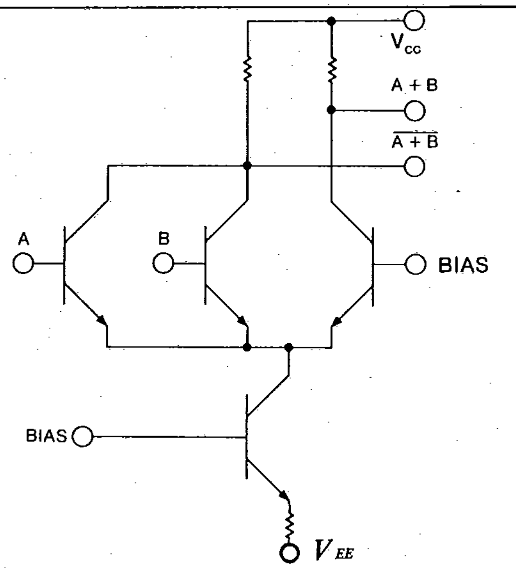

Figure 2. CML Collector Dotted Two-Input OR/NOR Gate

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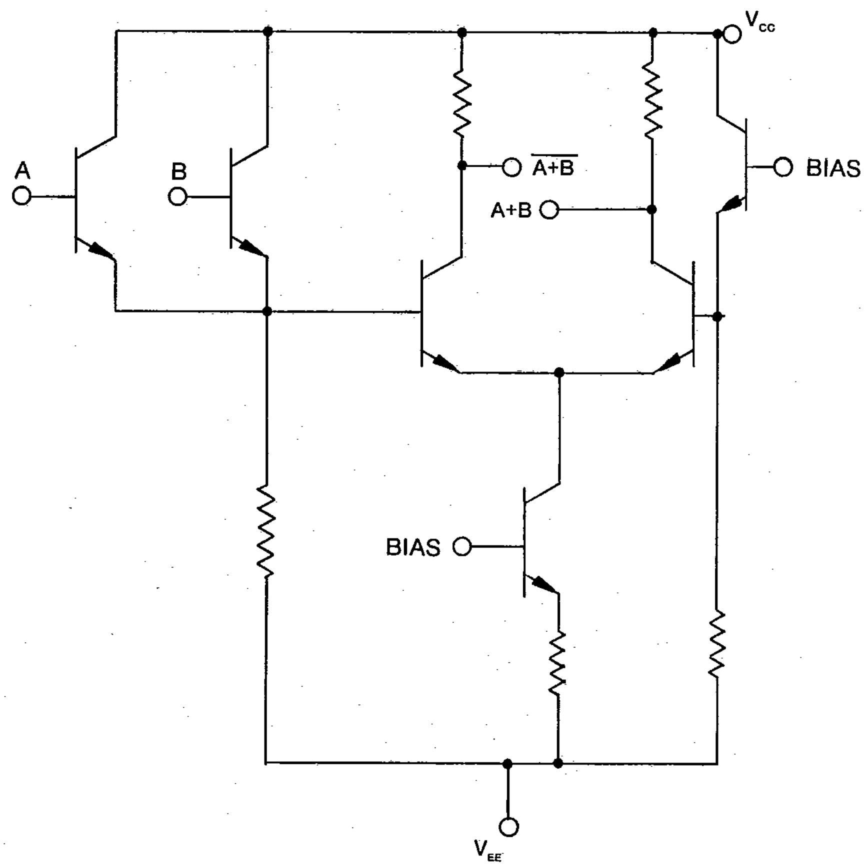

Figure 3. CML Emitter Dotted Two Input OR/NOR Gate

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RADIATION HARDENED CHARACTERISTICS

Honeywell's HM3500 Gate Array can also be used in radiation hardened applications. When ordering the HM3500 for use in such applications, specify the HM3500R Gate Array.

Honeywell's HM3500R Gate Array has been designed to operate in severe radiation environments. Special macrocells using emitter-dotted Current Mode Logic (Figure 3) have been designed to improve the transient upset radiation hardness. Consult your local Honeywell sales representative for descriptions of the macrocells designed for radiation hardened applications. Table 1 shows the radiation hardness design goals for the HM3500R.

RADIATION ENVIRONMENT	HARDNESS DESIGN GOAL
Total Dose	> 1E6 Rads Si
Neutron	> 1E15 N/cm squared
Dose Rate	
- long pulse	> 1E8 Rads Si/sec
- short pulse (upset)	> 1E9 Rads Si/sec
- short pulse (survival)	> 1E12 Rads Si/sec
Latch Up	None

Table 1. HM3500R Radiation Hardness Design Goals

POWER SUPPLY OPTIONS

The HM3500 operates using any one of the following combinations of power supply voltages.

MODE	CML V_{CC}	CML V_{EE}	I/O V_{CC}	I/O V_{EE}	I/O BUFFER OPTIONS
ECL (Reduced Pwr.)	0	–3.3	—	0	ECL 10K/100K, CML
ECL 10K	0	–5.2	—	0	ECL 10K/100K, CML
ECL 100K	0	–4.5	—	0	ECL 10K/100K, CML
TTL Only	+5.0	0	+5.0	0	TTL(1), CML
TTL Only (Reduced Pwr.)	+3.3	0	+5.0	0	TTL(1), CML
Mixed (Reduced Pwr.)	0	–3.3	+5.0	0	TTL(2), ECL 10K/100K, CML
Mixed	0	–4.5	+5.0	0	TTL(2), ECL 10K/100K, CML
Mixed	0	–5.2	+5.0	0	TTL(2), ECL 10K/100K, CML

TTL(1) and TTL(2) are separate designs.

Table 2. HM3500 Power Supply Requirements.

COMPUTER-AIDED-DESIGN SYSTEM

Honeywell's Software Toolkit™ for VLSI gate array design is built around industry standard software programs. Most importantly, a standardized design language, Mentor SIM™, is available for logic simulation. This language is used hierarchically to define complex logic functions in a computer readable data base. The data is then accessed by other software programs for simulation, analysis, autorouting, and array fabrication.

In addition to Mentor SIM, the Software Toolkit contains programs for schematic entry, netlist generation, timing verification, design statistic analysis, loading/fanout analysis, media delay feedback/analysis, and test program compilation. Industry standard programs are also available for automatic placement, automatic routing, and interactive graphics editing.

Honeywell supports the Software Toolkit for customers with a variety of in-house design automation capabilities. A set of tools hosted on popular workstations provides complete schematic-through-PG tape capability in the hands of the system designer. Customers can use the Software Toolkit at Honeywell's Colorado Springs Design Center or in their own facility.

FOR CUSTOMERS WITH MENTOR GRAPHICS ENGINEERING WORKSTATIONS

Mentor Graphics provides the following IDEA 1000™ programs as part of the Software Toolkit:

SYMED™ Mentor symbol generation package used with Honeywell-developed macrocell symbols. User may create new macrocell symbols using the macrocell library provided.

NETED™ Mentor schematic entry package used with Honeywell developed macrocells. User calls symbols from a library and interconnects them to implement his design.

SIM™ Mentor logic simulation package used with Honeywell developed macrocells. User provides input patterns to functionally debug the design.

EXPAND™ Mentor design expansion package used with Honeywell developed macrocells. Used for removing design hierarchy (nesting of macrocells) from design file prior to autoplacement.

Honeywell provides the following programs as part of the Software Toolkit:

LOADS™ Honeywell developed logic rules check and load modeling program. Informs the user of illegal loading or electrical violations. Also modifies macrocell propagation delays based on junction temperature, fanout, and power supply voltage.

STATS™ Honeywell developed design statistics report. Lists chip power, cell count and utilization. Informs user if either cell count or I/O count exceed maximums for the specific gate array.

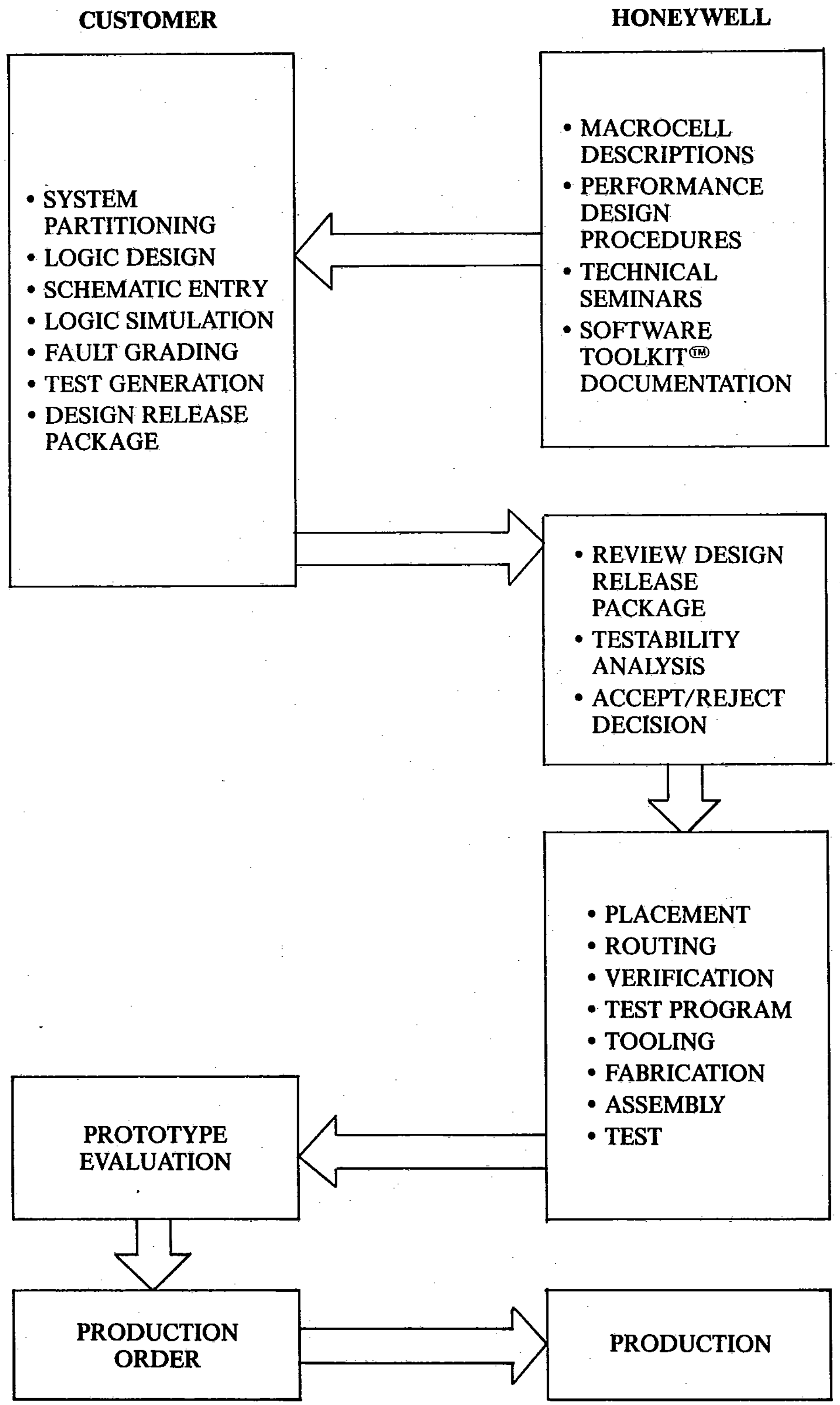
WIRES™ Honeywell developed wire delay calculation program. Lists all nets by line length and delay with error reporting for nets exceeding specified limits. Recomputes user design files with user specified temperature and actual wire delays.

TESTS™ Honeywell developed automatic test program compilation software. Takes functional test vectors from logic simulation and parametric test requirements to generate Series 20 compatible test tapes.

Ask your local Honeywell sales representative for further information on the Software Toolkit.

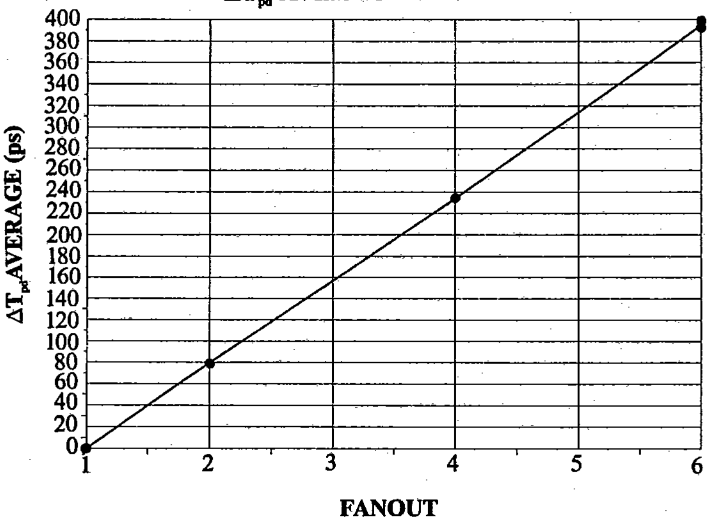
Honeywell

GATE ARRAY DEVELOPMENT FLOW

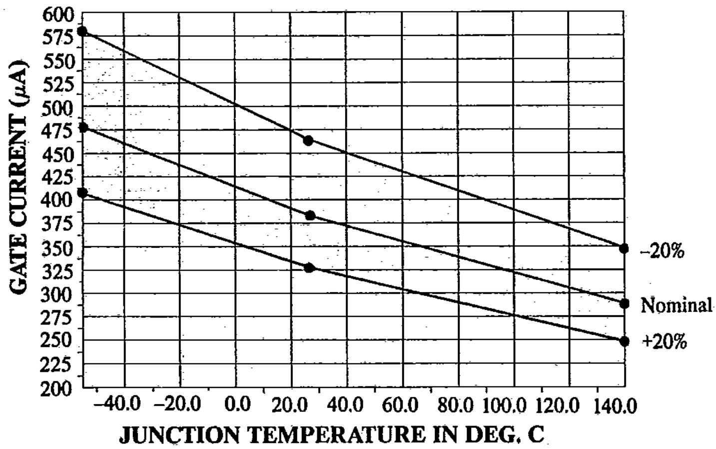


TYPICAL PERFORMANCE CHARACTERISTICS

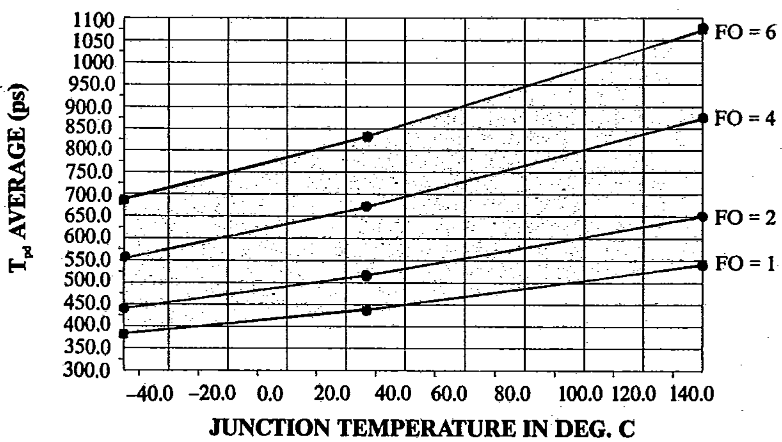
ΔT_{pd} AVERAGE VS FANOUT



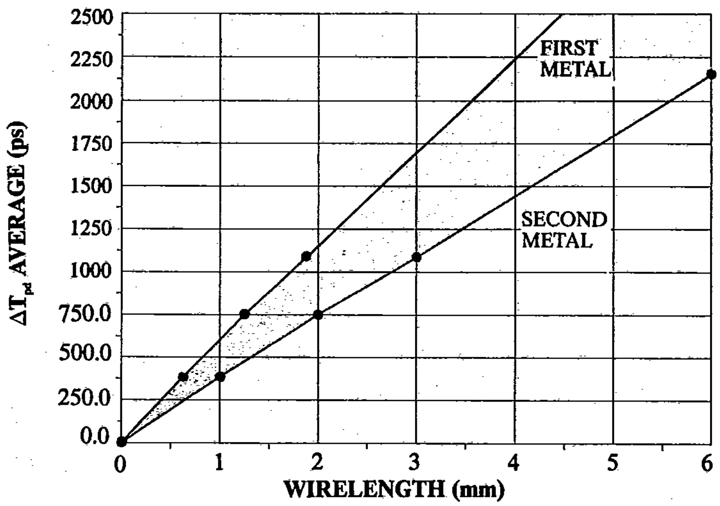
CML GATE CURRENT VS TEMPERATURE



CML GATE DELAY VS TEMPERATURE



ΔT_{pd} AVERAGE VS WIRELENGTHS



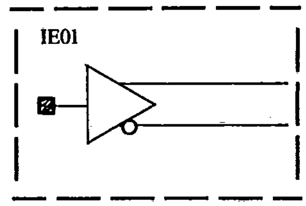
INPUT/OUTPUT CELLS—ECL AND CML INTERFACE

All signals within the array interface to external pins through I/O buffers located around the device perimeter. A description plus the logic for each I/O cell are shown in Figure 4.

INPUT BUFFERS

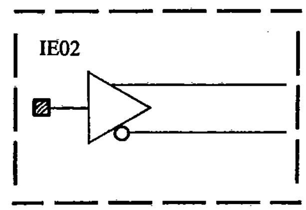
DESCRIPTION: ECL 10K/KH compatible input buffer with CML outputs.

LOGIC:



DESCRIPTION: ECL 100K compatible input buffer with CML outputs.

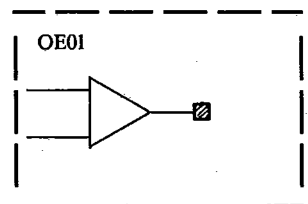
LOGIC:



OUTPUT BUFFERS

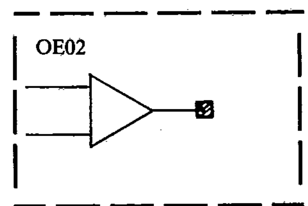
DESCRIPTION: ECL 10K/KH compatible output buffer with noninverting output. Capable of driving a 50Ω load.

LOGIC:



DESCRIPTION: ECL 100K compatible output buffer with noninverting output. Capable of driving a 50Ω load.

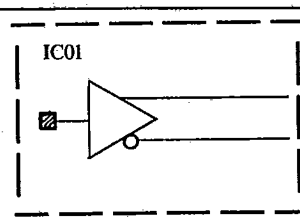
LOGIC:



INPUT BUFFERS

DESCRIPTION: CML compatible input buffer.

LOGIC:



OUTPUT BUFFERS

DESCRIPTION: CML compatible output buffer.

LOGIC:

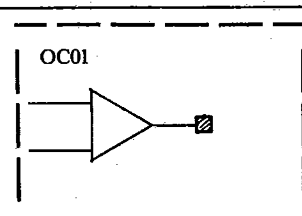


Figure 4. Input/Output Cells

ECL Mode

POWER DISSIPATION

The typical power dissipation for any implementation of the HM3500 Gate Array using ECL or CML I/0 is given by the following equation.

ECL 10K/100K, CML Power Dissipation (mW) = 1.14 mA x V_{EE} x # of ECL 10K/100K input buffers
\+ 1.0 mA x V_{EE} x # of CML input buffers
\+ 8.06 mA x V_{EE} x # of ECL 10K output buffers
\+ 9.24 mA x V_{EE} x # of ECL 100K output buffers
\+ 10.24 mA x V_{EE} x # of CML output buffers
\+ 0.40 mA x V_{EE} x # of CML current sources
\+ 86.9 mA x V_{EE} for voltage reference regulators.
NOTE: Use absolute values for V_{EE}.

Power dissipated in termination resistors must be calculated separately.

RECOMMENDED OPERATING CONDITIONS

Parameter	Description	Commercial			Military			Units
		Min	Nom	Max	Min	Nom	Max	
V_{EE} (Reduced)	Supply Voltage	-3.45	-3.30	-3.15	-3.60	-3.30	-3.00	V
V_{EE} (ECL 10K)	Supply Voltage	-4.95	-5.20	-5.45	-4.70	-5.20	-5.70	V
V_{EE} (ECL 100K)	Supply Voltage	-4.20	-4.50	-4.80	-4.00	-4.50	-4.90	V
T_A or T_C*	Operating free air temperature	0		70	-55		125	°C
F_{MAXT}	Maximum internal flip flop toggle frequency			600			600	MHz
F_{IN}	Maximum input frequency at standard package pin[1]			300			300	MHz

[1]Package selection will determine the maximum input frequency. Consult Honeywell.

ABSOLUTE MAXIMUM RATINGS[2]

Parameter	Description	Rating	Units
V_{EE}	Supply Voltage	-7.00	V
V_{IN}	Input Voltage	GND to VCC	V
T_A	Operating free-air temperature	-55° Ambient / 125° Case	°C
T_J	Operating junction temperature	160	°C

[2]COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL/TTL GATE ARRAY HM3500

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
CML GATE (Internal)									
I_{CC2G}	Power supply current per current source[1]	V_{CC1} = 0.0V, V_{EE} = −3.3V (See Notes below)	270	400	500	250	400	580	μA
ILF	Input load factor			1			1		Unit load
FO	Fanout		1		6	1		6	Unit load
t_{pdAV}	Average gate propagation delay	Fanout = one (1) CML gate	.40	.44	.50	.38	.44	.54	ns

[1]Typical applications estimate 2.5 gates current source.
Maximum current values at −55°C. Minimum current values at +125°C.
Consult Honeywell for CML gate performance at V_{EE} = −4.5V and V_{EE} = −5.2V.

CML INPUT/OUTPUT DC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER	COMMERCIAL LIMITS[2]			MILITARY LIMITS[2]			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH} Max	−0.005	−0.005	−0.005	−0.005	−0.005	−0.015	V
V_{OL} Max	−0.45	−0.465	−0.490	−0.410	−0.465	−0.510	V
V_{OL} Min	−0.515	−0.480	−0.565	−0.470	−0.480	−0.600	V

[2]Voltage levels referenced to V_{CC}.

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS—Over full ranges of recommended operating conditions

	$T_{ambient}$				T_{case}	
PARAMETER	-55°C	0°C	25°C	75°C	125°C	UNITS
VOH Max	−0.91	−0.84	−0.81	−0.73	−0.63	V
VIH Max			−0.81			V
VOH Min	−1.11	−1.02	−0.98	−0.91	−0.83	V
VIH Min	−1.26	−1.17	−1.13	−1.06	−0.98	V
VIL Max	−1.48	−1.48	−1.48	−1.48	−1.48	V
VOL Max	−1.63	−1.63	−1.63	−1.63	−1.63	V
VOL Min	−1.95	−1.95	−1.95	−1.95	−1.95	V
VIL Min			−1.85			V

ECL 10K INPUT/OUTPUT AC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS		LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFER										(IE01)
t_{PDLH}	Propagation delay, low to high	See Figure 5A	Fanout = 1		0.2	0.3		0.2	0.3	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	See Figure 5A	Fanout = 1		0.2	0.3		0.2	0.3	ns
			Fanout = 4							ns

ECL Mode

ECL 10K INPUT/OUTPUT AC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	COMMERCIAL LIMITS			MILITARY LIMITS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT BUFFER									**(OE01)**
t_{PDLH}	Propagation delay, low to high	See Figure 5B		0.9	1.5		0.9	1.5	ns
t_{PDHL}	Propagation delay, high to low	See Figure 5B		1.2	1.5		1.2	1.5	ns

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS	
V_{OH}	Output HIGH voltage	−1.025		−0.870	V	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW voltage	−1.830		−1.620	V		
V_{OHC}	Output HIGH voltage	−1.035			mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	
V_{OLC}	Output LOW voltage			−1.610	mV		
V_{IH}	Input HIGH voltage	−1.165		−0.880	mV	Guaranteed HIGH signal for all inputs	
V_{IL}	Input LOW voltage	−1.810		−1.475	mV	Guaranteed LOW signal for all inputs	
I_{IL}	Input LOW current	0.50			μA	$V_{IN} = V_{IL (Min)}$	

ECL 100K INPUT/OUTPUT AC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS		COMMERCIAL LIMITS			MILITARY LIMITS			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFER										**(IE02)**
t_{PDLH}	Propagation delay, low to high	See Figure 5A	Fanout = 1		0.2	0.3		0.2	0.3	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	See Figure 5A	Fanout = 1		0.2	0.3		0.2	0.3	ns
			Fanout = 4							ns
OUTPUT BUFFER										**(OE02)**
t_{PDLH}	Propagation delay, low to high	See Figure 5B			1.2	1.9		1.2	1.9	ns
t_{PDHL}	Propagation delay, high to low	See Figure 5B			1.2	1.6		1.2	1.6	ns

ECL/TTL GATE ARRAY HM3500

CML INPUT/OUTPUT AC CHARACTERISTICS—Over full ranges of recommended operating conditions

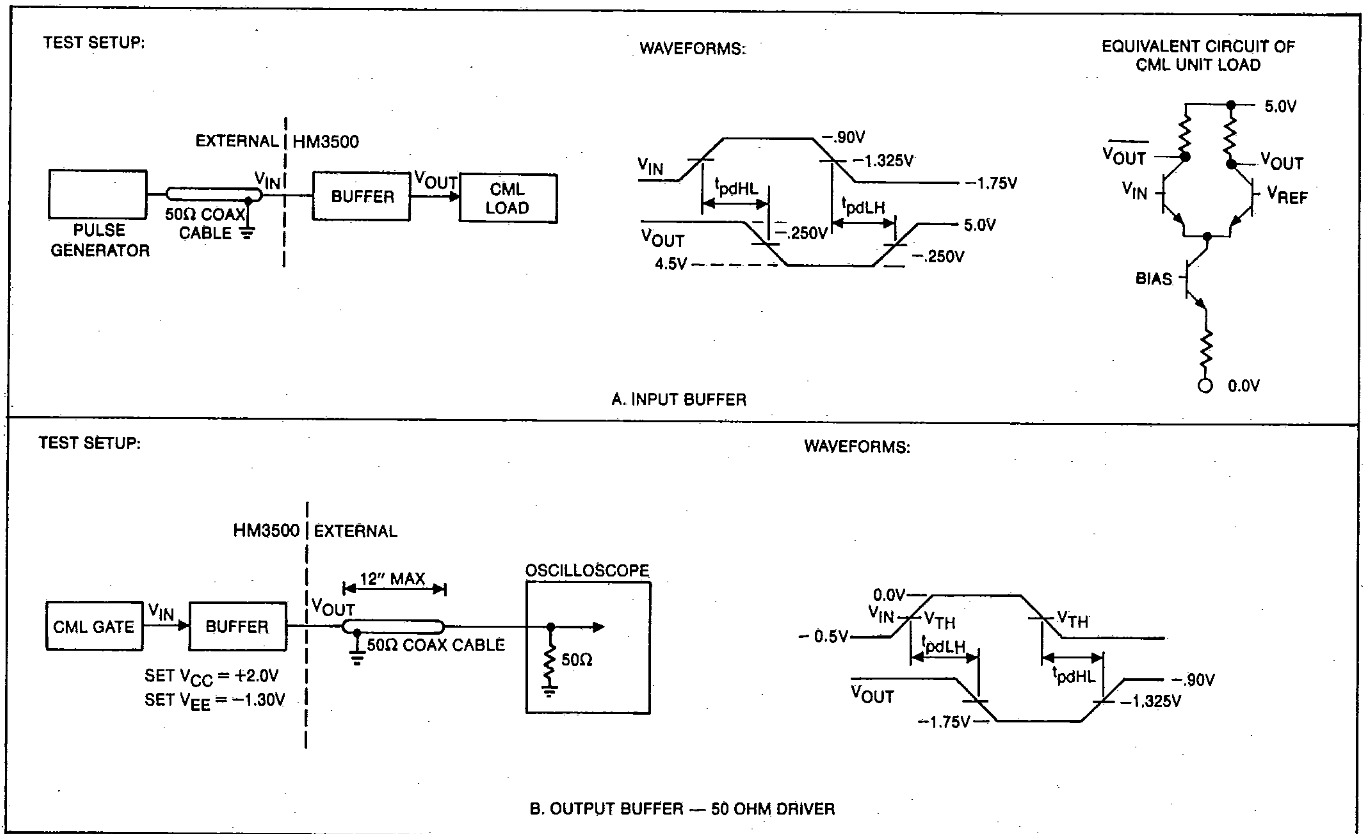
PARAMETER		TEST CONDITIONS		COMMERCIAL LIMITS			MILITARY LIMITS			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFER										**(IC01)**
t_{PDLH}	Propagation delay, low to high	1	Fanout = 1		0.4	0.4		0.4	0.4	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	1	Fanout = 1		0.5	0.6		0.5	0.6	ns
			Fanout = 4							ns

PARAMETER		TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	MILITARY MIN	MILITARY TYP	MILITARY MAX	UNITS
OUTPUT BUFFER										**(OC01)**
t_{PDLH}	Propagation delay, low to high	1	Fanout = 1		0.7	0.8		0.7	0.8	ns
										ns
t_{PDHL}	Propagation delay, high to low	1	Fanout = 1		0.8	1.2		0.8	1.2	ns
										ns

[1]Consult Honeywell for a description of test conditions.

ECL Mode

Honeywell



TESTING ECL COMPATIBLE OUTPUTS

To obtain results correlating with Honeywell specifications, specific testing techniques must be used.

All power leads and signal leads must be kept as short as possible. Equal length coaxial cables must be used between the test set and the scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended. Interconnect fittings should be 50-ohm GR, BNC, Selectro Conhex, or equivalent. Wire length should be less than ¼ inch from TPin to input and TPout to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times. In addition, the positive supply (V_{CC}) should be decoupled from the test board by an RF type 25μF capacitor to –3.3V. V_{CC} should be set to +2.0V and V_{EE} set to –1.3V. With this setup, the termination resistors may be connected to GND.

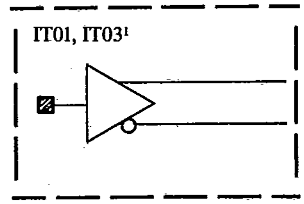
Figure 5. ECL Test Configurations

INPUT/OUTPUT CELLS—TTL INTERFACE

INPUT BUFFERS

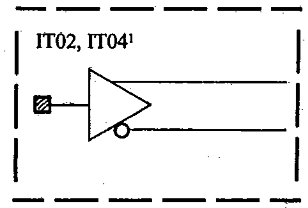
DESCRIPTION: LSTTL compatible input buffer with CML outputs.

LOGIC:



DESCRIPTION: LSTTL compatible Schmidt trigger buffer with CML outputs.

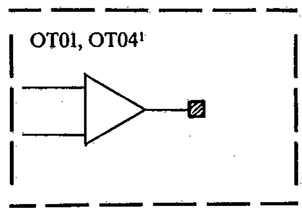
LOGIC:



OUTPUT BUFFERS

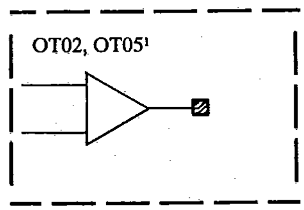
DESCRIPTION: LSTTL compatible output buffer with active pullup output.

LOGIC:



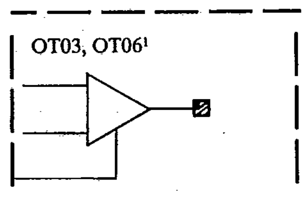
DESCRIPTION: LSTTL compatible output buffer with open collector output.

LOGIC:



DESCRIPTION: LSTTL compatible output buffer with three state output.

LOGIC:



[1] Input buffers IT03, IT04 and output buffers OT04, OT05, OT06 are used in ECL/TTL mixed mode operation.

Figure 4. (continued). Input/Output Cells

TTL Mode

POWER DISSIPATION

The typical power dissipation for any implementation of the HM3500 Gate Array using LSTTL I/O is given by the following equation.

TTL Only Power Dissipation (mW) = (3.05 mA x CML V_{cc} + 1.53 mA x TTL V_{cc}) x # of TTL A.P. output buffers
+ (4.46 mA x CML V_{cc} + 1.93 mA x TTL V_{cc}) x # of TTL 3-state output buffers
+ (3.05 mA x CML V_{cc} + 1.25 mA x TTL V_{cc}) x # of TTL O.C. output buffers
+ 10.24 mA x CML V_{cc} x # of CML output buffers
+ 1.67 mA x CML V_{cc} x # of TTL Schmidt input buffers
+ 0.91 mA x CML V_{cc} x # of TTL input buffers
+ 1.0 mA x CML V_{cc} x # of CML input buffers
+ 0.4 mA x CML V_{cc} x # of CML current sources
+ 86.9 mA x CML V_{cc} for voltage reference regulators.
+ .5V x load current (mA)
NOTE: Use absolute values for V_{cc}.

Load Current = Maximum I_{OL} for selected temperature range x total number of output buffers/transceivers that can be at a low output state simultaneously.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	DESCRIPTION	COMMERCIAL			MILITARY			UNITS
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
V_{CC1}	TTL I/O Supply voltage (Reduced Power)	4.75	5.00	5.25	4.50	5.00	5.50	V
V_{CC2}	CML Logic Supply voltage (Reduced Power)	3.15	3.30	3.45	3.00	3.30	3.60	V
V_{CC1}	TTL I/O Supply voltage	4.75	5.00	5.25	4.50	5.00	5.50	V
V_{CC2}	CML Logic Supply voltage	4.75	5.00	5.25	4.50	5.00	5.50	V
T_A or T_C	Operating free-air temperature	0		70	−55		125	°C
F_{MAXT}	Maximum internal flip flop toggle frequency			150			150	MHz
F_{IN}	Maximum input frequency at package pin[1]			100			100	MHz

[1]Package selection will determine the maximum input frequency. Consult Honeywell.

ABSOLUTE MAXIMUM RATINGS[2]

PARAMETER	DESCRIPTION	RATING	UNITS	PARAMETER	DESCRIPTION	RATING	UNITS
V_{CC1}	Supply voltage	+7.0	V	V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
V_{CC2}	Supply voltage	+4.6	V				
E_{IN}	Input voltage continuous	−0.5 to +5.5	V				
I_{IN}	Input current continuous	−30 to +1.0	mA	T_J	Junction temperature	+175	°C

[2]Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TTL Mode

Honeywell

ECL/TTL GATE ARRAY HM3500

DC AND AC ELECTRICAL CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
CML GATE (Internal)									
I_{CC2G}	Power supply current per current source[1]	$V_{CC1} = 3.3V$	270	400	500	250	400	580	μA
ILF	Input load factor			1			1		Unit load
FO	Fanout		1		6	1		6	Unit load
T_{pdAV}	Average gate propagation delay	Fanout = One (1) CML gate	.40	.44	.50	.38	.44	.54	ns

[1]Typical applications estimate 2.5 gates current source.

Maximum current values at –55°C. Minimum current values at +125°C.

LSTTL INPUT/OUTPUT DC CHARACTERISTICS—Over full ranges of recommended operating conditions

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}[2]	Input High voltage	Guaranteed input High voltage for all inputs	2.6			2.6			V
V_{IL}[2]	Input Low voltage	Guaranteed input Low voltage for all inputs			0.8			0.8	V
V_{OH}	Output High voltage	$IV_{CC} = Min, I_{OH} = -1mA$	2.7	3.4		2.5	3.4		V
V_{OL}	Output Low voltage	$V_{CC} = Min, I_{OL} = 12mA$			0.5			0.5	V
I_{OZH}	Output "off" current High (3-state)	$V_{CC} = Max, V_{OUT} = 2.7V$			20			20	μA
I_{OZL}	Output "off" current Low (3-state)	$V_{CC} = Max, V_{OUT} = 0.4V$			–20			–20	μA
I_{IH}	Input High current	$V_{CC} = Max, V_{IN} = 2.7V$			20			20	μA
I_I	Input High current at max input voltage	$V_{CC} = Max, V_{IN} = 5.5V$			100			100	μA
I_{IL}	Input Low current	$V_{CC} = Max, V_{IN} = 0.4V$			–.04			–0.4	mA

TTL Mode

LSTTL INPUT/OUTPUT AC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS		COMMERCIAL LIMITS			MILITARY LIMITS			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFER										**(IT01)**
t_{PDLH}	Propagation delay, low to high	See Figure 6A	Fanout = 1		1.2	1.5		1.2	1.5	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	See Figure 6A	Fanout = 1		0.2	0.3		0.2	0.3	ns
			Fanout = 4							ns
INPUT BUFFER										**(IT02)**
t_{PDLH}	Propagation delay, low to high	See Figure 6A	Fanout = 1		2.4	2.6		2.4	2.6	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	See Figure 6A	Fanout = 1		1.8	2.4		1.8	2.4	ns
			Fanout = 4							ns

OUTPUT BUFFER										**(OT02)**
t_{PDLH}	Propagation delay, low to high	See Figure 6C			5.4	6.9		5.4	6.9	ns
										ns
t_{PDHL}	Propagation delay, high to low	See Figure 6C			4.6	5.8		4.6	5.8	ns
										ns
OUTPUT BUFFER										**(OT01)**
t_{PDLH}	Propagation delay, low to high	See Figure 6B			5.4	6.9		5.4	6.9	ns
										ns
t_{PDHL}	Propagation delay, high to low	See Figure 6B			4.6	5.8		4.6	5.8	ns
										ns
OUTPUT BUFFER										**(OT03)**
t_{PDLH}	Propagation delay, low to high	See Figure 6D			5.4	6.9		5.4	6.9	ns
t_{PDHL}	Propagation delay, high to low	See Figure 6D			4.6	5.8		4.6	5.8	ns

TTL Mode

Honeywell

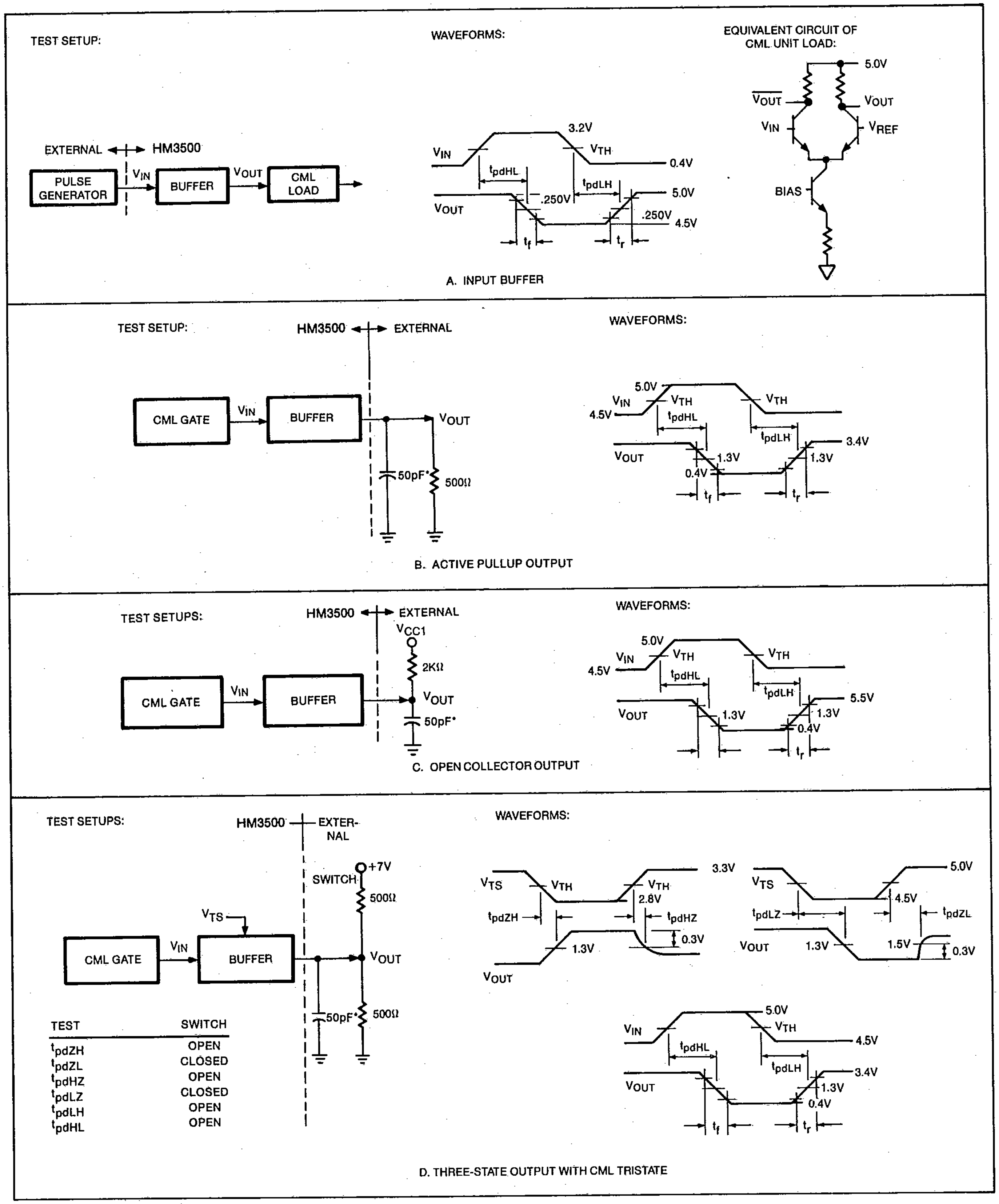


Figure 6. LSTTL Test Configurations

POWER DISSIPATION

The typical power dissipation for any implementation of the HM3500 Gate Array using mixed ECL and TTL I/O is given by the following equation.

Power Dissipation (mW) =

1.14 mA x V_{EE} x # of ECL 10K/100K input buffers
\+ 1.0 mA x V_{EE} x # of CML input buffers
\+ 8.06 mA x V_{EE} x # of ECL 10K output buffers
\+ 9.24 mA x V_{EE} x # of ECL 100K output buffers
\+ 10.24 mA x V_{EE} x # of CML output buffers
\+ (1.28 mA x CML V_{EE} + 0.82 mA x TTL V_{CC}) x # of TTL input buffers
\+ (2.56 mA x CML V_{EE} + 0.49 mA x TTL V_{CC}) x # of TTL Schmidt input buffers
\+ (3.83 mA x CML V_{EE} + 1.23 mA x TTL V_{CC}) x # of TTL A.P. output buffers
\+ (3.81 mA x CML V_{EE} + 0.93 mA x TTL V_{CC}) x # of TTL O.C. output buffers
\+ (4.48 mA x CML V_{EE} + 2.7 mA x TTL V_{CC}) x # of TTL 3-state output buffers
\+ .5V + load current (mA)

NOTE: Use absolute values for V_{CC} and V_{EE}.

Load Current = Maximum I_{OL} for selected temperature range x total number of output buffers/transceivers that can be at a low output state simultaneously.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	DESCRIPTION	COMMERCIAL			MILITARY			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
TTL V_{CC}	Supply Voltage (Reduced Power)	+4.75	+5.00	+5.25	+4.50	+5.00	+3.50	V
CML V_{EE}	Supply Voltage (Reduced Power)	–3.45	–3.30	–3.15	–3.60	–3.30	–3.00	V
TTL V_{CC}	Supply Voltage	+4.75	+5.00	+5.25	+4.50	+5.00	+5.50	V
CML V_{EE}	Supply Voltage (ECL 100K)	–4.20	–4.50	–4.80	–4.00	–4.50	–4.90	V
CML V_{EE}	Supply Voltage (ECL 10K)	–4.95	–5.20	–5.45	–4.70	–5.20	–5.70	V
T_A	Operating free air temperature	0		70	–55		125	C
F_{MAXT}	Maximum internal flip flop toggle frequency			600			600	MHz
F_{IN}	Maximum input frequency at standard package pin[1]			100			100	MHz

[1]Package selection will determine the maximum input frequency. Consult Honeywell.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNITS
TTL V_{CC}	Supply Voltage	+7.0V	V
CML V_{EE}	Supply Voltage	–7.0V	V
V_{IN}	Input Voltage	–0.5 to +5.5	V
T_A or T_C	Operating free-air temperature	–55 Ambient / 125 Case	°C
T_J	Operating junction temperature	175	°C

Mixed Mode

Honeywell

ECL/TTL GATE ARRAY HM3500

LSTTL INPUT/OUTPUT DC CHARACTERISTICS—Over full ranges of recommended operating conditions

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	Input High voltage	Guaranteed input High voltage for all inputs	2.6			2.6			V
V_{IL}	Input Low voltage	Guaranteed input Low voltage for all inputs			0.8			0.8	V
V_{OH}	Output High voltage	IV_{CC} = Min, I_{OH} = –1mA	2.7	3.4		2.5	3.4		V
V_{OL}	Output Low voltage	V_{CC} = Min, I_{OL} = 12mA			0.5			0.5	V
I_{OZH}	Output "off" current High (3-state)	V_{CC} = Max, V_{OUT} =			20			20	μA
I_{OZL}	Output "off" current Low (3-state)	V_{CC} = Max, V_{OUT} =			–20			–20	μA
I_{IH}	Input High current	V_{CC} = Max, V_{IN} = 2.7V			20			20	μA
I_I	Input High current at max input voltage	V_{CC} = Max, V_{IN} = 5.5V			100			100	μA
I_{IL}	Input Low current	V_{CC} = Max, V_{IN} = 0.4V			–0.4			–0.4	mA

Mixed Mode

Honeywell

LSTTL INPUT/OUTPUT AC CHARACTERISTICS—Over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS		COMMERCIAL LIMITS			MILITARY LIMITS			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BUFFER										**(IT03)**
t_{PDLH}	Propagation delay, low to high	See Figure 6A	Fanout = 1		1.5	2.7		1.5	2.7	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	See Figure 6A	Fanout = 1		1.1	1.2		1.1	1.2	ns
			Fanout = 4							ns
INPUT BUFFER										**(IT04)**
t_{PDLH}	Propagation delay, low to high	See Figure 6A	Fanout = 1		2.2	5.2		2.2	5.2	ns
			Fanout = 4							ns
t_{PDHL}	Propagation delay, high to low	See Figure 6A	Fanout = 1		1.6	2.1		1.6	2.1	ns
			Fanout = 4							ns

OUTPUT BUFFER										**(OT05)**
t_{PDLH}	Propagation delay, low to high	See Figure 6C			6.5	9.1		6.5	9.1	ns
										ns
t_{PDHL}	Propagation delay, high to low	See Figure 6C			3.5	5.2		3.5	5.2	ns
										ns
OUTPUT BUFFER										**(OT04)**
t_{PDLH}	Propagation delay, low to high	See Figure 6B			6.5	9.1		6.5	9.1	ns
										ns
t_{PDHL}	Propagation delay, high to low	See Figure 6B			3.5	5.2		3.5	5.2	ns
										ns
OUTPUT BUFFER										**(OT06)**
t_{PDLH}	Propagation delay, low to high	See Figure 6D			6.5	9.1		6.5	9.1	ns
t_{PDHL}	Propagation delay, high to low	See Figure 6D			3.5	5.2		3.5	5.2	ns

Mixed Mode

Honeywell

UNDERSTANDING CURRENT MODE LOGIC

From the earliest days of bipolar technology, circuit designers noted that current switches are faster than their voltage counterparts. A logic family based on steering currents, without altering their values, is intrinsically faster than one based on voltage-switching techniques. That is the reason ECL and CML circuits are generally faster than TTL.

Both ECL and CML use a differential pair of NPN transistors for switching current. Circuit diagrams of the basic gates look similar (Figure 7), but they differ in operation.

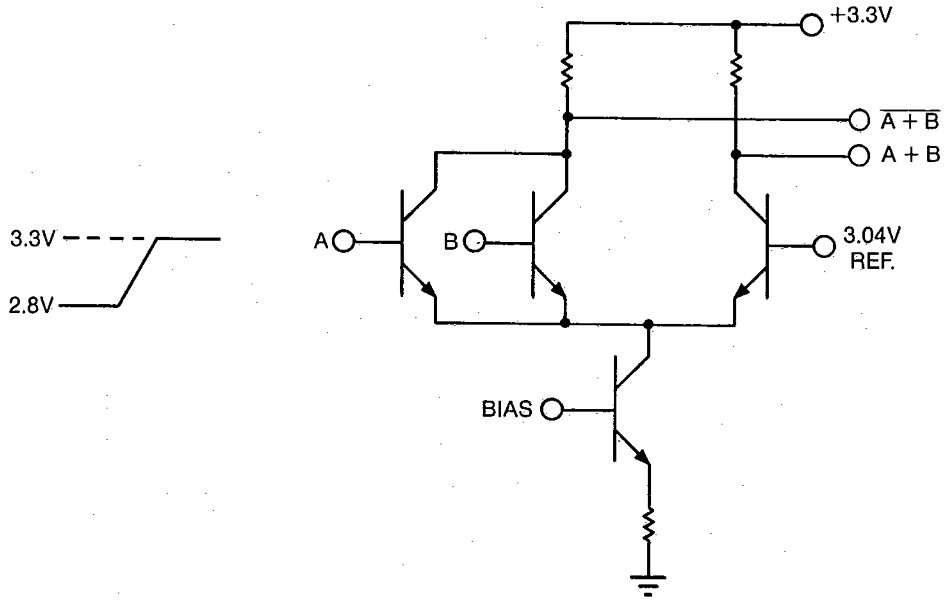
The reference voltages represent the center point of the logic swing. In ECL, with a –1.29 volt reference and a nominal collector voltage swing of .85 volt, the collector-base junction on the signal input side goes to 0 volts under worst case conditions. On the reference side, that junction always remains reverse-biased by .44 volt. Thus, the transistors never saturate. However, the emitter-follower is always on, increasing power consumption. The use of the emitter follower output dictates the ECL operating levels. Rather than rising all the way to the positive power supply voltage, the ECL output high level stays a diode drop below.

In contrast, CML employs a reference voltage of .25 volt below the positive supply and a signal swing of .5 volt. The collector-base junction of the input transistor then becomes forward-biased by .5 volt at most, a condition termed soft saturation because negligible forward injection across the junction takes place. With almost no excess charge stored in the base in soft saturation, switching speed is comparable with that of ECL. At the same time, an off transistor cuts off completely. The additional power of ECL's emitter-follower driver is eliminated.

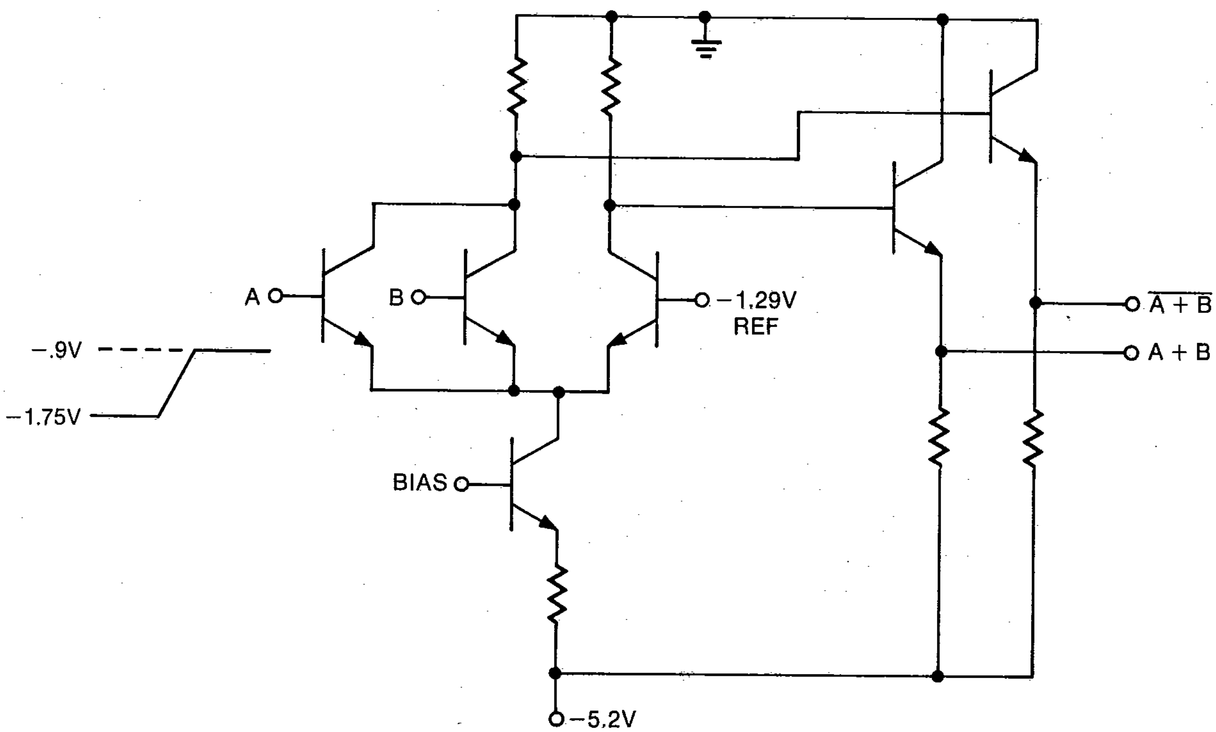
The single differential pair of a CML gate drives following gates directly from either collector. Both true and complement outputs are available with nearly equal speed. Gate delays are essentially a single transistor delay because most logic functions are implemented with a single differential pair as the primary switch. Series gating generates many useful logic functions with a single logic-gate delay, as in the Master Slave D Flip Flop shown in Figure 8. The 3.3 volt supply is the minimum voltage that supports the series-gating logic structure, so CML power consumption is at an absolute minimum without sacrificing any speed.

In CML circuits intended for gate array or VLSI custom chip use, currents are set on chip by a voltage and temperature compensated reference regulator. Reliable operation over commercial and military temperature ranges is achieved.

For further information, ask your Honeywell representative for the article reprints entitled "Honeywell High Speed Digital Technology".



(A) BASIC CML OR/NOR LOGIC GATE



(B) BASIC ECL OR/NOR LOGIC GATE

Figure 7. Basic Gates

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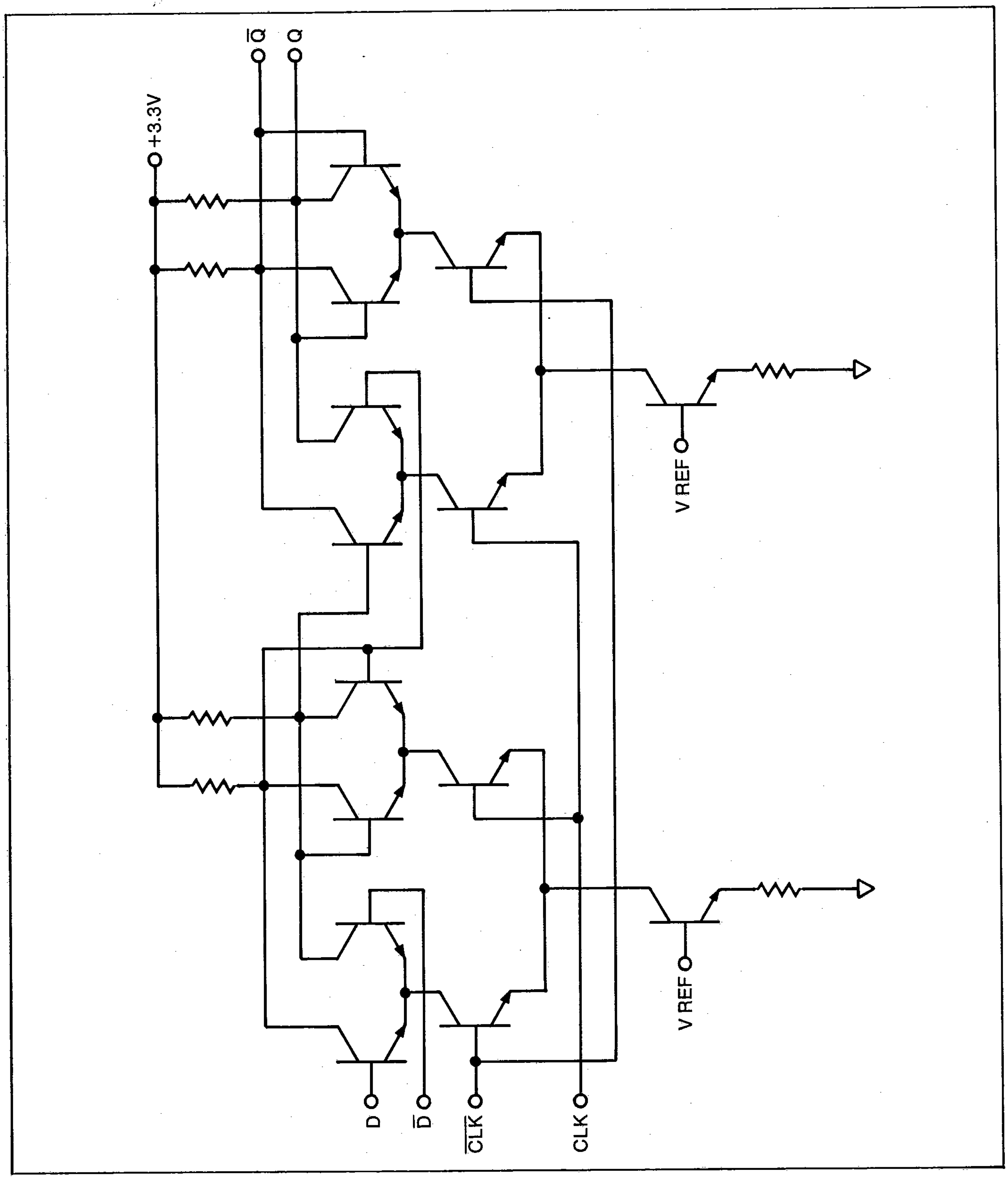

Figure 8. CML Master Slave D Flip Flop

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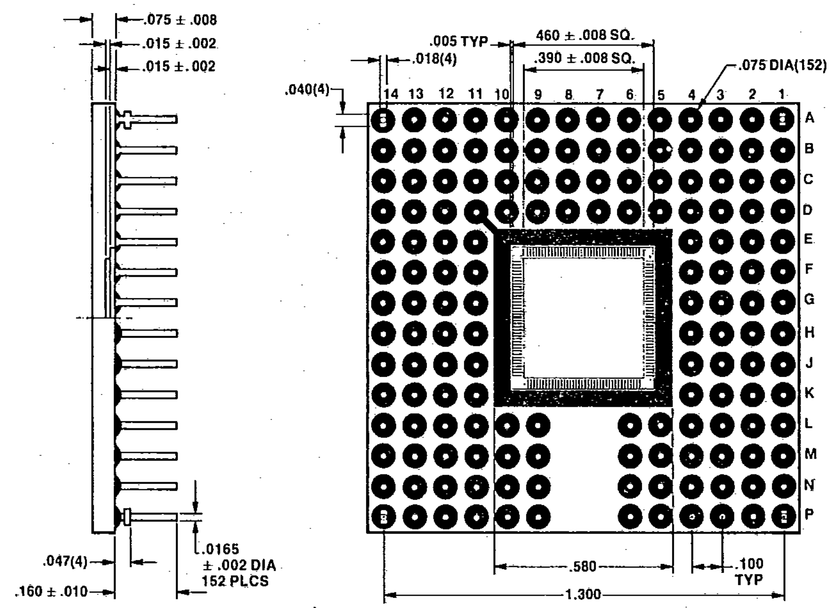

NOTES:

- Pins D4, D11, L4, and L11 are connected to Die Attach Area
- TTL GND Pins: L5, L6, L9, D9, D7, D6
  TTL VCC1 Pins: D5, K4, K11, D10
  CML GND Pins: G4, D4, D11, L4, L11, G11
  CML VCC Pins: F4, J4, J11, H11, F11, E11, E4
- Tolerance: ±0.005 unless otherwise specified
- Pins brazed to metallized ceramic using Ag/Cu Eutectic
- Pin Material: Kovar or Alloy 42 + Nickel + Gold (60 Microinch minimum)
- Metallization: Refractory Metal + Nickel + Gold (60 Microinch minimum)
- Material: Ceramic, Al_2O_3 Black

Figure 9. PGAB Package Dimensions

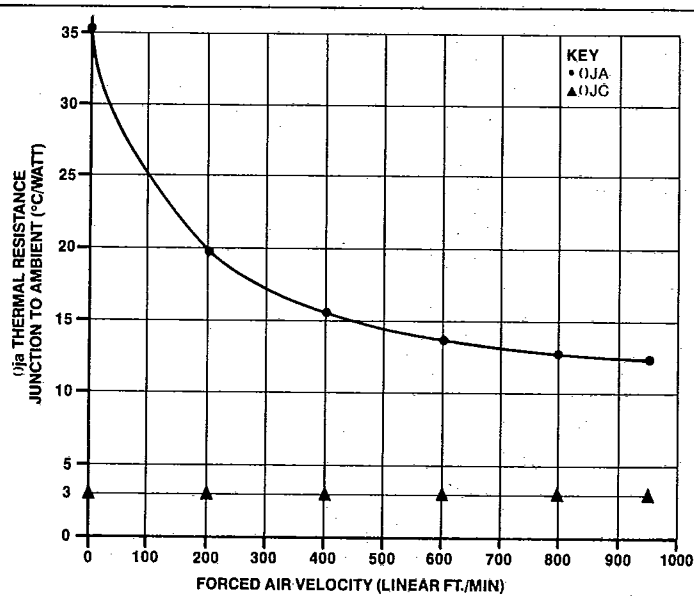

Figure 10. Thermal Characteristics of PGAB Package

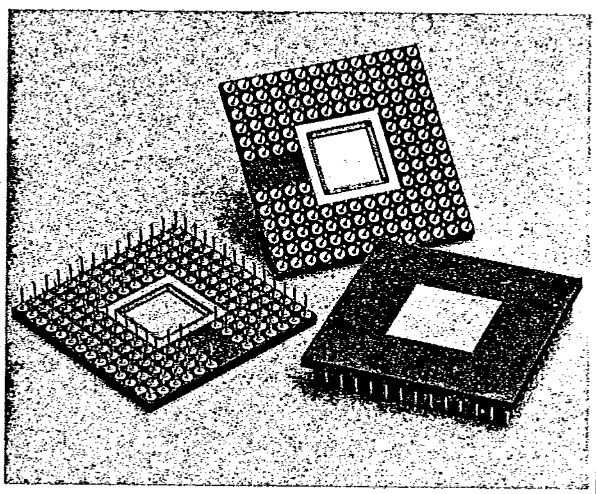

Figure 11. HM3500 PGAB Package

Honeywell

ECL/TTL GATE ARRAY HM3500

PACKAGING

For commercial applications, the HM3500 is offered in a 152 pin grid array shown in Figure 9. The die is mounted cavity down to provide an elevated primary heat conducting surface ideally suited to forced-air cooling. The central die cavity is square to provide matched lead lengths and voltage drops. Hermeticity is provided with a solder-sealed lid.

The package has 120 I/O pins and 28 power and ground pins. All pins are positioned in a uniform rectangular grid on 100 mil centers. The HM3500 die is attached to the ceramic substrate using a eutectic die attach to provide a low thermal resistance path.

Consult Honeywell for the appropriate packaging to use in military applications.

HEAT SINKING

The HM3500 Gate Array was designed to be used in either forced-air cooled or convection cooled systems. Maximum junction temperatures of 175 degrees C are allowed. Junction to case thermal resistance is typically less than 5 degrees C/watt, while the junction to ambient thermal resistance is a function of heat sink mounting technique, air flow, and surrounding electronics.

Honeywell