2K x 8 Very Low Power CMOS SRAM

Description

The HM 65162 is a very low power CMOS static RAM organized as 2048 × 8 bits. It is manufactured using the MHS high performance CMOS technology.

The HM 65162 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible stadby supply current (typical value = 0.1 µA) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Easy memory expansion is provided be an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.

All inputs and outputs of the HM-65162 are TTL compatible and operate from single 5 V supply thus simplifying system design.

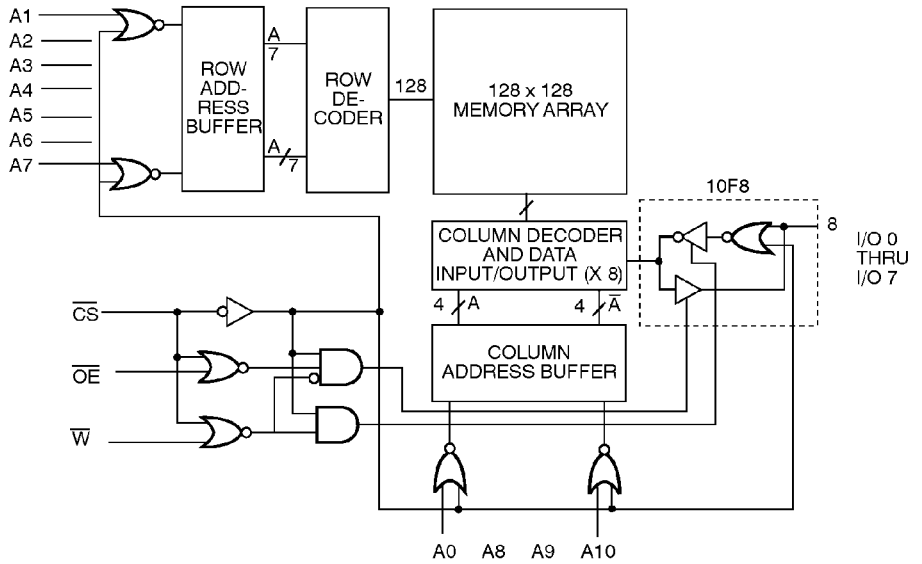
The HM 65162 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

Features

- Access Time
  Commercial : 70 ns (max)
  Automotive/Military/Industrial : 70/85 ns (max)
- Very Low Power Consumption
  Active : 240 mW (typ)
  Standby : 2.0 µW (typ)
  Data Retention : 0.8 µW (typ)
- Wide Temperature Range : –55 to +125°C
- 600 Mils Width Package
- TTL Compatible Inputs and Outputs
- Asynchronous
- Single 5 Volt Supply
- Equal Cycle and Access Time
- Gated Inputs : No Pull-up/Down Resistors Are Required

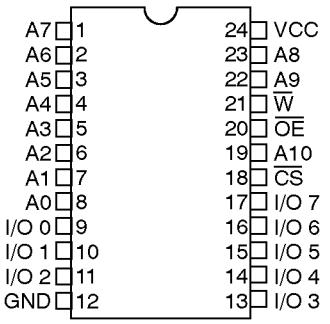
Interface

Block Diagram



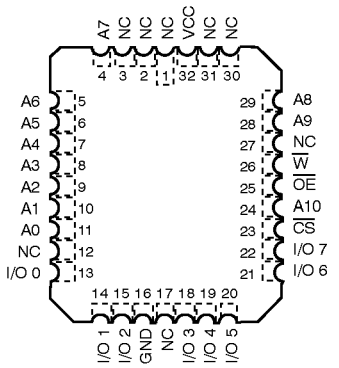
Pin Configuration

Plastic 600 mils, 24 pins, DIL.
Ceramic 600 mils, 24 pins, DIL.



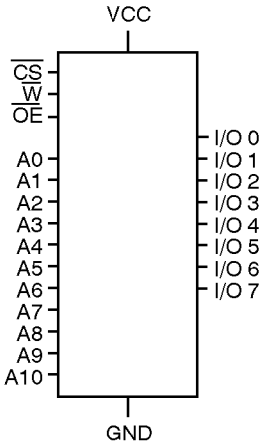
Pinout DIL 24 pins (top view)

LCC, 32 pins.



Pinout LCC 32 pins (top view)

Logic Symbol



Pin Names

A0–A10 :	Address inputs	$\overline{CS}$:	Chip Select
I/O0–I/O7 :	Input/Output	$\overline{OE}$:	Output Enable
VCC :	Power	$\overline{W}$:	Write enable
GND :	Ground		

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	DATA–IN	DATA–OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : . . . . . –0.5 V to + 7.0 V
Input or Output voltage applied : . . . . . (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : . . . . . –65°C to + 150°C

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military (– 2)	V_{CC} ± 10 %	– 55°C to + 125°C
Automotive (– A)	V_{CC} ± 10 %	– 40°C to + 125°C
Industrial (– 9)	V_{CC} ± 10 %	– 40°C to + 85°C
Commercial (– 5)	V_{CC} ± 10 %	0°C to 70°C

Recommended DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	V_{CC} + 0.3 V	V

Note : 1. VIL min = –0.3 V or –1.0 V pulse width 50 ns.

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	5	pF
Cout (2)	Output capacitance	–	–	7	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	– 1.0	–	1.0	µA
IOZ (3)	Output leakage current	– 1.0	–	1.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Note : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4.0 mA, IOH = –1.0 mA.

Consumption for Commercial (–5) Specification

SYMBOL		PARAMETER	65162 –5	65162C–5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	2.0	mA	max
ICCSB1	(6)	Standby supply current	1.0	100.0	µA	max
ICC	(7)	Operating supply current	70.0	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	70.0	mA	max

Consumption for Industrial (–9) Specification

SYMBOL		PARAMETER	65162 B–9	65162 –9	65162 C–9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	3.0	3.0	mA	max
ICCSB1	(6)	Standby supply current	5.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP	(8)	Dynamic operating current	70.0	70.0	70.0	mA	max

Consumption for Automotive (–A) & Military (–2) Specifications

SYMBOL		PARAMETER	65162 B–2	65162 –2	65162 C–2	UNIT	VALUE
ICCSB	(5)	Standby supply current	5.0	5.0	5.0	mA	max
ICCSB1	(6)	Standby supply current	50.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	70.0	70.0	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	70.0	70.0	mA	max

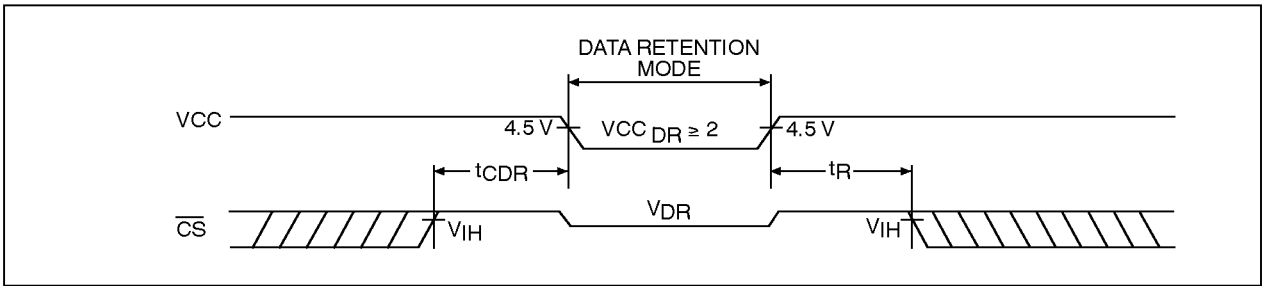
Notes : 5. $\overline{CS} \geq$ VIH.
6. $\overline{CS} \geq$ Vcc – 0.3 V, Iout = 0 mA.
7. $\overline{CS} \leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

Data Retention Mode

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc -0.2 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begin operation > 55 ns after Vcc reaches the minimum operating voltage (4.5 V).

Timing



Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1(11)	Data retention current				
	2.0 V HM–65162B–9	–	0.1	2.0	µA
	HM–65162B–2/–A	–	0.1	20.0	µA
	HM–65162C–5	–	0.1	30.0	µA
	HM–65162C–9	–	0.1	30.0	µA
	HM–65162C–2/–A	–	0.1	200.0	µA
ICCDR2(11)	Data retention current				
	3.0 V HM–65162B–9	–	0.3	3.0	µA
	HM–65162B–2/–A	–	0.3	30.0	µA
	HM–65162C–5	–	0.3	50.0	µA
	HM–65162C–9	–	0.3	50.0	µA
	HM–65162C–2/–A	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

AC Parameters

AC Conditions :

Input pulse levels : . . . . . Gnd to 3.0 V
Input timing reference levels : . . . . . 1.5 V
Input rise : . . . . . 5 ns
Output load : . . . . . 1 TTL gate + 100 pF

Write Cycle : Commercial (–5) Specification

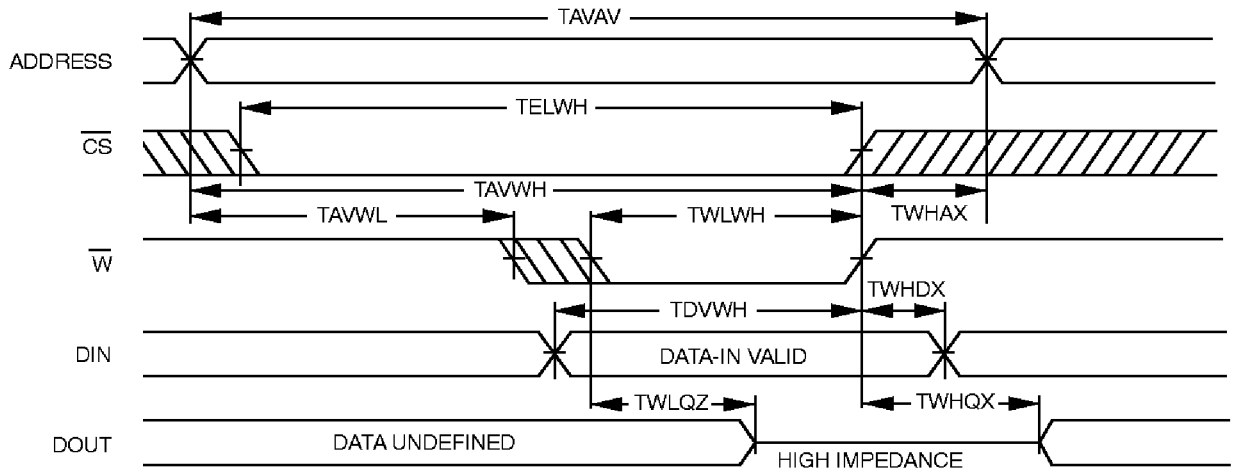
SYMBOL	PARAMETER	65162–5	65162C–5	UNIT	VALUE
TAVAV	Write cycle time	70	70	ns	min
TAVWL	Address set–up time	0	0	ns	min
TAVWH	Address valid to end of write	50	50	ns	min
TDVWH	Data set–up time	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	45	45	ns	min
TWLQZ(12)	Write low to high Z	40	40	ns	max
TWLWH	Write pulse width	40	40	ns	min
TWHAX	Address hold to end of write	10	10	ns	min
TWHDX	Data hold time	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	ns	min

Write Cycle : Industrial (–9), Automotive (–A) and Military (–2) Specifications

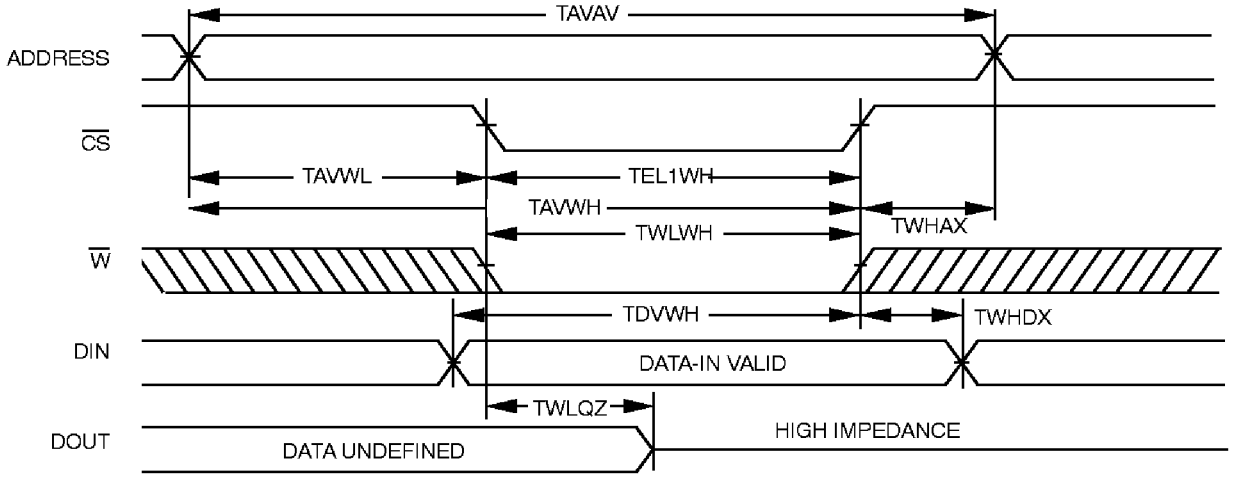
SYMBOL	PARAMETER	65162 B–9/2/A	65162 –9/2/A	65162 C–9/2/A	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set–up time	0	0	0	ns	min
TAVWH	Address valid to end of write	50	65	65	ns	min
TDVWH	Data set–up time	30	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	45	55	55	ns	min
TWLQZ(12)	Write low to high Z	40	50	50	ns	max
TWLWH	Write pulse width	40	55	55	ns	min
TWHAX	Address hold to end of write	10	10	10	ns	min
TWHDX	Data hold time	10	10	10	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Write Cycle 1 ($\overline{W}$ Controlled) (note 13)



Write Cycle 2 ($\overline{CS}$ Controlled) (note 13)



Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data I/O Pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.

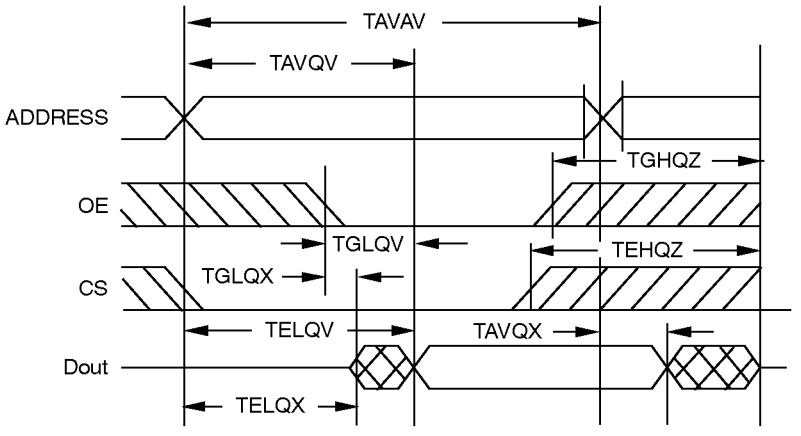
Read Cycle : Commercial (–5) Specification

SYMBOL	PARAMETER	65162 –5	65162 C–5	UNIT	VALUE
TAVAV	Read cycle time	70	70	ns	min
TAVQV	Address access time	70	70	ns	max
TAVQX	Address valid to low Z	5	5	ns	min
TELQV	Chip–select access time	70	70	ns	max
TELQZ	$\overline{CS}$ low to low Z	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	50	50	ns	max
TGLQV	Output enable access time	50	50	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	40	40	ns	max

Read Cycle : Industrial (–9), Automotive (–A) and Military (–2) Specifications

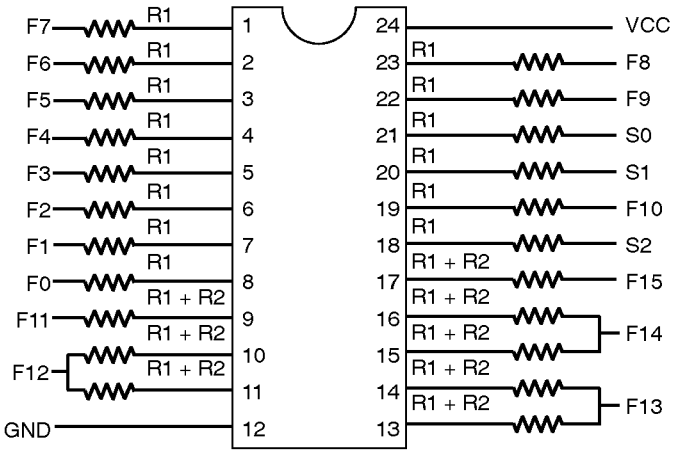
SYMBOL	PARAMETER	65162 B–9/2/A	65162 –9/2/A	65162 C–9/2/A	UNIT	VALUE
TAVAV	Read cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip–select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	50	50	ns	max
TGLQV	Output Enable access time	50	65	65	ns	max
TGLQX	$\overline{OE}$ low to low Z	5	5	5	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	40	40	ns	min

Read Cycle



Addresses must remain stable for the duration of the read cycle. To read $\overline{OE}$ and $\overline{CS}$ must be < VIL and $\overline{W}$ VIH. The output buffers can be controlled independently by $\overline{OE}$ while $\overline{CS}$ is low. To execute consecutive read cycles. $\overline{CS}$ may be tied low continuously until all desired locations are accessed. When $\overline{CS}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

Burn-in Schematics



R1 = 1 KΩ
R2 = 2.2 KΩ
Fo = 25 KHz ± 20 %
Fn = 1/2 F n – 1
S0, S1, S2 : programmable signals for write / read cycles
VCC = 5.5 V

Ordering Information

PACKAGE		DEVICE TYPE	GRADE	LEVEL
HM	3 —	65162	B	–5 : R

0 –Chip form
1 –Ceramic 24 pins 600 mils
3 –Plastic 24 pins 600 mils
4 –LCC 32 pins

2 k × 8 very low power static RAM

B = high speed/low current
Blank : standard speed/low current
C : standard

–A : Automotive
–2 : Military
–5 : Commercial
–6 : 100% 25°C Probe
–9 : Industrial
/883 : MIL STD 883 Class B or S
DB : Dice Military program
R : Tape & Reel option
RD : Tape & Reel/Dry pack option
D : Dry pack option

Military and Space Versions

The following table gives package/consumption/access time/process flow available combinations

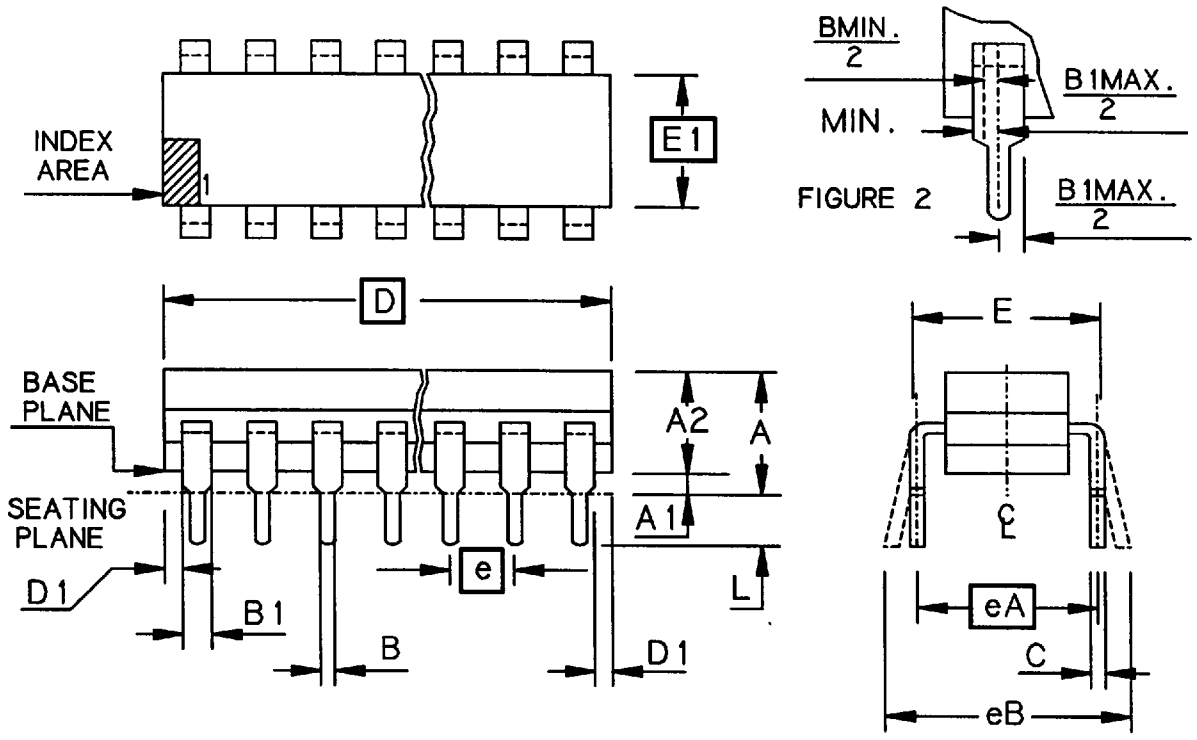
Temp. range	Packages	Access Time (ns) Iccsb (µA)			Std process 65162	RT process 65162		
		B 70 50	S 85 50	C 85 500	Mil flows	Std	/883	ESA / SCC
M	1 C 4 0	● ● ● X	● ● ● X	● ● ● ●	● ● ● ●			
S	C 4 0	● ● X	● ● X	 ●		● ● ●	● ● ●	● ● ●

● = product in production

X = call sales office for availibility

M H S	MECHANICAL OUTLINE DICTIONARY	TEMIC

24 PINS PLASTIC .600



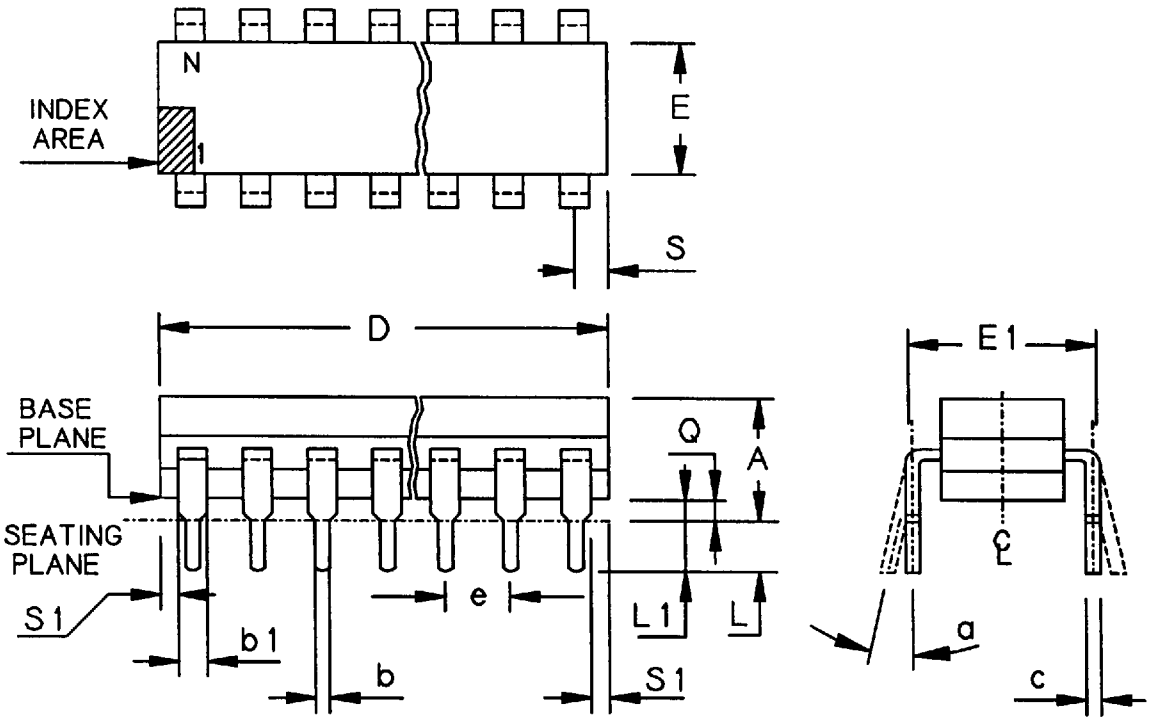
	MM		INCH	
A	-	6.35	-	.250
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	29.21	32.77	1.150	1.290
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54	B.S.C	.100	B.S.C
eA	15.24	B.S.C	.600	B.S.C
eB	-	17.78	-	.700
L	2.93	5.08	.115	.200
D1	0.13	-	.005	-
PKG STD		02		

CODE : 3

REV :F | DATE : 12-05-95

M H S	MECHANICAL OUTLINE DICTIONARY	TEMIC

24 LEADS CERDIP .600



	MM		INCH	
	min	max	min	max
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b1	0.96	1.65	.038	.065
c	0.20	0.38	.008	.015
D	-	32.77	-	1.290
E	12.70	15.50	.500	.610
E1	14.99	15.75	.590	.620
e	2.54 B.S.C		.100 B.S.C	
L	3.18	5.08	.125	.200
L1	3.81	-	.150	-
Q	0.38	1.90	.015	.075
S	-	2.49	-	.098
S1	0.13	-	.005	-
a	0° - 15°		0° - 15°	
N	24			

COMPLIANT MIL-M-38510H (D-3).

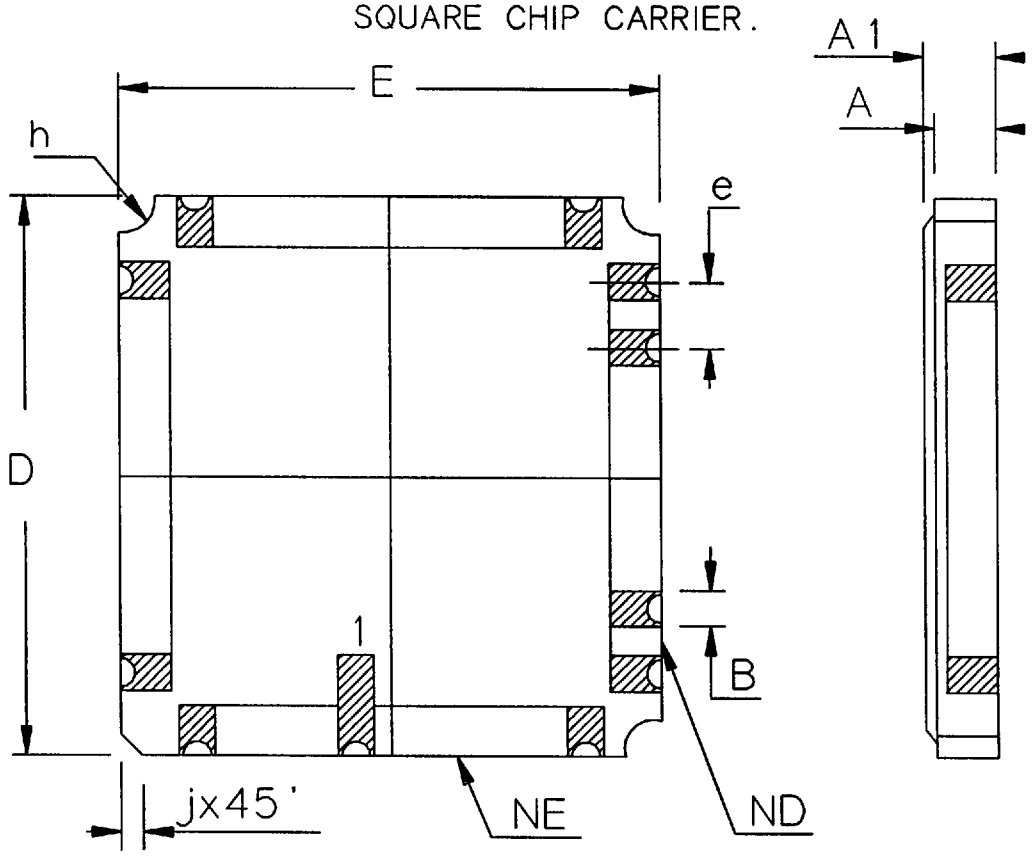
CODE : 1

REV :F	DATE : 17-11-93

M H S	MECHANICAL OUTLINE DICTIONARY

TEMIC

32 LDS .040 CENTER LEADLESS SQUARE CHIP CARRIER.



	MM		INCH	
A	1.47	1.83	.058	.072
A1	1.60	2.03	.063	.080
B	0.51	TYP	.020	TYP
D	10.54	10.92	.415	.430
E	10.54	10.92	.415	.430
e	1.02	BSC	.040	BSC
h	0.19	RAD	.008	RAD
j	0.51		.020	
ND	8		8	
NE	8		8	
PKG STD	- 01 -			

CODE : 4J

REV :D DATE : 25-03-91