DATA SHEET HM 65231

2K x 8 CMOS DUAL PORT RAM

FEATURES

- **HIGH SPEED, FAST ACCESS TIME:**
  COMMERCIAL: 80 ns max
  INDUSTRIAL: 100 ns max
  MILITARY: 120 ns max
- **STANDBY CURRENT: 3 mA**
- **OPERATING SUPPLY CURRENT: 60 mA max**
- **BATTERY BACK UP OPERATION:**
  2V DATA RETENTION
- **ONE SEPARATE ADDRESS/DATA PORT, ONE MULTIPLEXED ADDRESS/DATA PORT**
- **3 PROGRAMMABLE ARBITRATION MODES ON CHIP**
- **INT AND BUSY OUTPUTS**
- **FULLY STATIC OPERATION**
- **TTL COMPATIBLE INPUT/OUTPUT**
- **SINGLE 5V+/-10% POWER SUPPLY**

DESCRIPTION

The HM 65231 is a CMOS 2K x 8 high-speed Dual Port Static RAM. This state of the art technology used to fabricate it, combined with innovative circuit design techniques provides high speed access times together with excellent low power performance.

The HM 65231 provides two ports with controls, address and I/O. Port X is compatible with general purpose buses with separate address and data; Port Y is directly compatible with a CPU providing multiplexed address and data. It is then possible to interconnect a CPU (type 8088 or 6809) or a microcontroller (type 8051) with a general purpose bus or a local bus without additional logic. Due to input buffers with gated inputs, the $\overline{CE}$ control pin permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high).

Three programmable arbitration modes are available to resolve any contention with the maximum of efficiency. This allows the interconnection of two buses using READY signals or a bus with a READY signal to a bus without wait state capability (8051). In both cases, the access arbitration is totally software transparent.

The third mode is a general purpose mode based on a software controlled flag.

Depending upon the programmed mode, the memory locations 7FE and 7FF are defined as standard memory words or as two 8-bit flag registers. It is then possible to implement up to 16 concurrent communication channels with error free handshaking.

Two internal interrupt request flags are provided. Each flag is set or reset when memory locations 7FE or 7FF are accessed.

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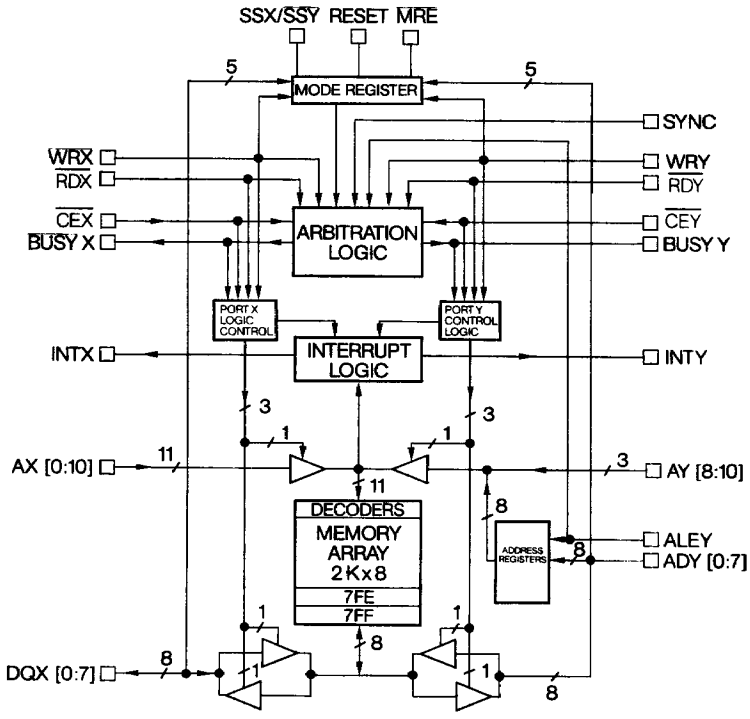
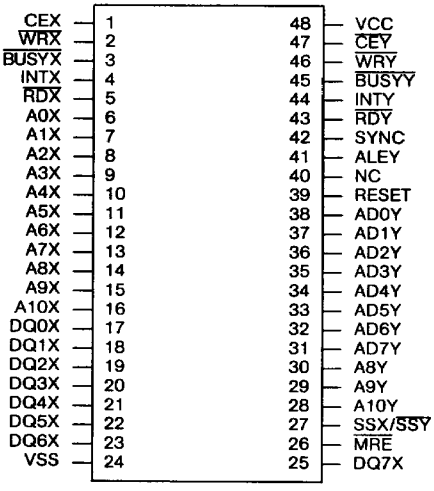
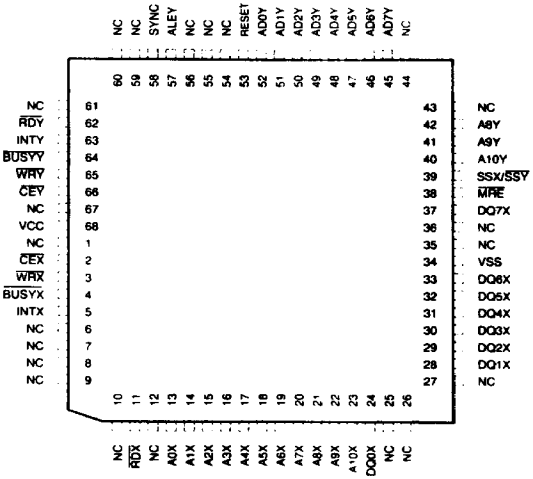
FUNCTIONAL DIAGRAM



Pinout





PIN DEFINITION

$\overline{CEX}$	:	Port X is selected when $\overline{CEX}=0$
ALEY	:	Port Y address latch enable
$\overline{CEY}$	:	Port Y is selected when $\overline{CEY}=0$
$\overline{WRX}$, $\overline{WRY}$	:	Port X and Port Y write strobe
$\overline{RDX}$, $\overline{RDY}$	:	Port X and Port Y read strobe
INTX, INTY	:	Port X and Port Y interrupt request controlled by memory locations 7FE/7FF
$\overline{BUSYX}$	:	In mode 1 and mode 2, when enabled ($\overline{CEX}=0$), this output is low if the Port X access must be delayed. When disabled ($\overline{CEX}=1$), this output is high. In mode 3, this output always reproduces SSF state.
$\overline{BUSYY}$	:	In mode 1, this output has the same function than $\overline{BUSYX}$ (not used in mode 2). In mode 3, this output always reproduces $\overline{SSF}$ state
$\overline{MRE}$	:	The internal mode register is selected when $\overline{MRE}=0$
SSX/$\overline{SSY}$	:	The mode register is programmed from Port X (resp Port Y) when SSX/$\overline{SSY}$=VSS (resp SSX/$\overline{SSY}$=VSS)
RESET	:	After the power-on, the internal mode register must be cleared by RESET which is an active high input.
AX (0 : 10)	:	Port X address bus
DQX (0 : 7)	:	Port X input/output bus
ADY (0 : 7)	:	Port Y multiplexed address and data bus
AY (8 : 10)	:	Port Y non multiplexed address bus
SYNC	:	Clock input to synchronize the Dual Port RAM when in mode 2. May be directly connected to 8088 system clock
VCC	:	Power
VSS	:	Ground
NC	:	No Connection

TRUTH TABLE

$\overline{CE}$	$\overline{RD}$	$\overline{WR}$	$\overline{MRE}$	MODE
1	X	X	1	Standby
0	0	1	1	Memory read operation
0	1	0	1	Memory write operation
1	X	0	0	Mode register programming

MODE REGISTER

The internal 5-bit mode register MR0... MR4 can be written either from DQX (0 : 4) or ADY (0 : 4) according to the SSX/$\overline{SSY}$ value, SSX/$\overline{SSY}$ = VCC : Port X, SSX/$\overline{SSY}$=VSS : Port Y (*see figure 1*).

Regardless of the arbitration mode, the mode register has to the programmed prior to the first memory access.

The mode register is a write only register.

ARBITRATION

The memory array cannot be accessed simultaneously from the two ports. To allow correct memory access, 3 programmed modes are provided (2 bits of the mode register are used to define the current arbitration mode).

Mode 1 : Asynchronous mode

If, during a memory access, the other port makes a request, this new request must be delayed until the present operation is completed.

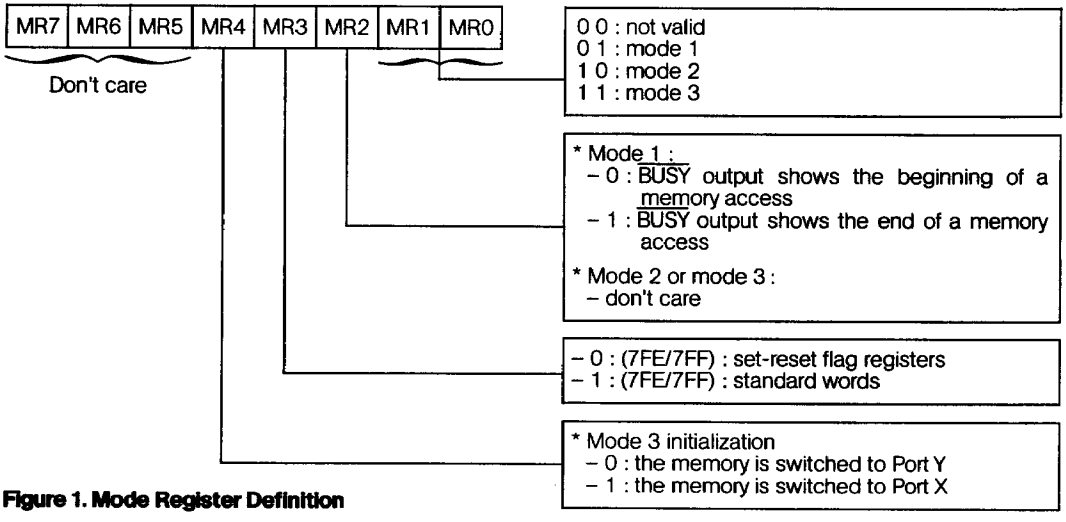


Figure 1. Mode Register Definition

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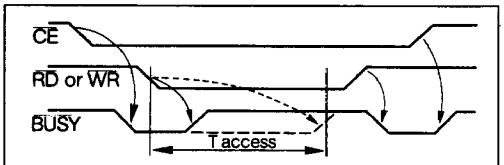
In asynchronous mode, the $\overline{BUSY}$ output indicates either the beginning or the end of a memory access according to the mode, *see fig. 2.*



Dotted line : $\overline{BUSY}$ output shows the end of memory access.
Sold line : $\overline{BUSY}$ output shows the beginning of memory access.

Figure 2. BUSY output when in mode 1

Mode 2 : SYNCHRONOUS mode

This feature allows direct interconnection of a bus having READY signal (8088 or similar) on Port X to another without wait state capability (8051 or similar). Operating conditions are in *fig. 3.*

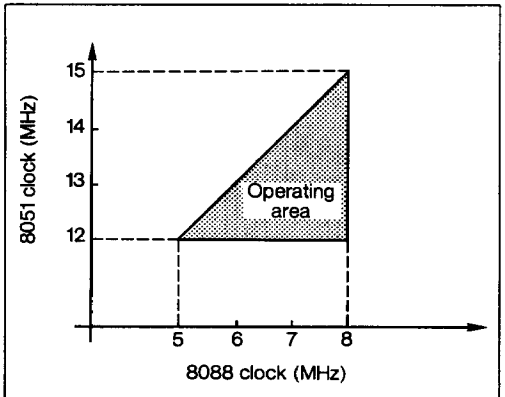


Figure 3. Relation between 8051/8088 system clock when in mode 2

Mode 3 : Software controlled switch

An internal flag SSF (Side Select Flag) is used to define which port is able to access the memory

- when a port is selected, a write operation from this port to the memory location 7FE or 7FF (both may be used by each port) switches the memory to the opposite port.
- the initial value of SSF is programmed in the mode register. Port X is selected by MR4 = 1 and Port Y by MR4 = 0.

INTERRUPT REQUEST

a) Two internal interrupt request flags are provided, INTX for Port X, INTY for Port Y. The flags are set or reset when the memory location 7FF or 7FE are accessed *(see figure 4).*

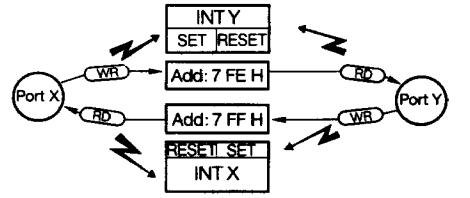


Figure 4. Interrupts set and reset

- writing to memory location 7FF from Port Y sets INTX
- reading memory location 7FF from Port X resets INTX
- reading location 7FF from Port Y or writing to it from Port X does not change the state of INTX
- the same method is used to set or reset INTY. That is writing 7FE from Port X and reading it from Port Y.

b) One bit of the mode register programs the memory locations 7FE and 7FF to be standard memory words or 8 bit flag registers:

- when "standard words" are selected, the locations behave as normal RAM.
- when "flag register" is selected, reading one of the locations clears all the bits. Writing to it, sets the bits for which the corresponding data bit is **1**, otherwise the bit remains unchanged *(see figure 5).*

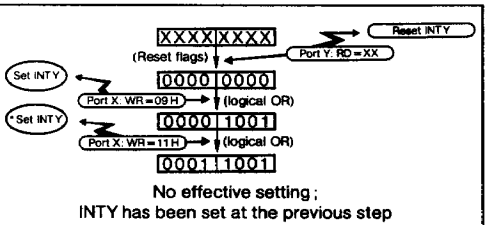
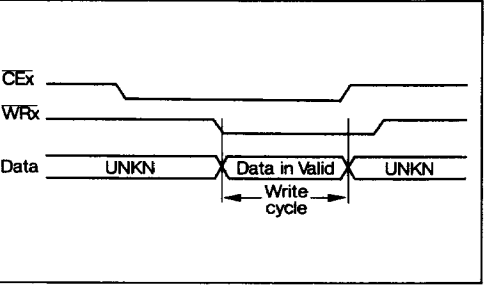


Figure 5. Flag registers option (ex.: memory location 7 FEH)

*** Warning:**

When a write access is done to one of these "flag registers". The data has to be stable from the beginning to the end of the write cycle.



The arbitration mechanism also applies to interrupt flag access; thus avoiding contention. However, when the third mode is used with "standard word", it is possible to set the interrupt flag from an unvalidated port by carring out a dummy write to 7FF from Port Y or 7FE from Port X.

So, the corresponding interrupt output may be used as a memory request signal to the other processors.

In this mode, the $\overline{BUSY}$ pin reproduces the state of SSF. This feature can be used to inform the processor whether or not it has control of the memory. It is then the responsibility of the designer to avoid contention.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VCC-GND) – 0.3V* to 7 V

Input or output voltage applied: GND – 0.3V* to VCC + 0.3V

Storage temperature: – 65 °C to 150 °C

* – 1 V pulse width 50 ns.

OPERATING RANGE	Operating Voltage	Operating Temperature
Military – 2	5V ± 10%	– 55 °C to + 125 °C
Industrial – 9	5V ± 10%	– 40 °C to + 85 °C
Commercial – 5	5V ± 10%	0 °C to + 70 °C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS

SYMBOL		PARAMETER	– 5	– 9	– 2	Unit	Value
ICCSB	(1)	Standby supply current	6	8	10	mA	max
ICCSB1	(2)	Standby supply current	100	350	1000	µA	max
ICCOP	(3)	Average operating supply current	60	65	70	mA	max
ICC	(4) (5)	Power supply current	60 8	65 10	70 15	mA mA	max max
II/O	(6)	Input/output leakage current	±1	±1	±2	µA	max
VIL	(7)	Input low voltage	0.8	0.8	0.8	V	max
VIH	(7)	Input high voltage	2.2	2.2	2.2	V	min
VOL	(8)	Output low voltage	0.4	0.4	0.4	V	max
VOH	(8)	Output high voltage	2.4	2.4	2.4	V	min
CI	(9)	Input capacitance	8	8	8	pF	max
CO	(9)	Input/output capacitance	108	10	10	pF	max

Note 1 : $\overline{CEX}$=VIH, $\overline{CEY}$=VIH, $\overline{MRE}$=VIH, ALE=0, IOUT=0.

Note 2 : $\overline{CEX}$=VCC – 0.3 V, CEY=VCC – 0.3 V, $\overline{MRE}$=VCC – 0.3 V, ALE=0, IOUT=0.

Note 3 : ICCOP with a duty cycle = 100%, VI=VCC or GND, Ii/io=0, f=1 MHz
typical derating = 5 mA/MHz.

Note 4 : $\overline{CEX}$=VIL or $\overline{CEY}$=VIL, IOUT=0
addresses and data inputs level=VCC or GND, RDX or WRX=0 or RDY or WRY=0.

Note 5 : $\overline{CEX}$=VIL or $\overline{CEY}$=VIL, IOUT=0
addresses and data inputs level=VCC or GND, $\overline{RDX}$ and $\overline{WRX}$=1 and $\overline{RDY}$ and $\overline{WRY}$=1.

Note 6 : VCC=5.5 V, VIN=GND to VCC.

Note 7 : VIH max=VCC + 0.3 V; VIL min=– 0.3 V or – 1 V pulse width 50 ns.

Note 8 : IOL=3.2 mA; IOH=– 1 mA.

Note 9 : This parameter is sampled and not 100% tested, TA=25°C, f=1 MHz.

MODE 1: ASYNCHRONOUS MODE

AC PARAMETERS

AC test Conditions:
- VCC = 5 V ± 10%
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

MODE 1: READ CYCLE

SYMBOL		PARAMETER	-5	-9	-2	Unit	Value
TAVEL	(3)	Address set up time	0	0	0	ns	min
TAVRL	(4)	Address set up time	0	0	0	ns	min
TELBUH	(1) (3) (2) (3)	$\overline{BUSY}$ high after $\overline{CE}$ low	65 125	70 130	70 130	ns ns	max max
TRLBUH	(1) (4) (2) (4)	$\overline{BUSY}$ high after $\overline{RD}$ low	65 125	70 130	70 135	ns ns	max max
TBUHQX	(1) (2)	$\overline{BUSY}$ high to output active	25 -45	30 -60	35 -75	ns ns	min max
TBUHQV	(1) (2)	Data valid after $\overline{BUSY}$ high	75 -45	90 -25	95 -15	ns ns	max min
TBUHEH	(1) (2)	$\overline{CE}$ high after $\overline{BUSY}$ high	45 0	60 0	75 0	ns ns	min min
TBUHRH	(1) (2)	$\overline{RD}$ high after $\overline{BUSY}$ high	45 0	60 0	75 0	ns ns	min min
TEHBUH	(5)	$\overline{BUSY}$ high after $\overline{CE}$ high	30	35	35	ns	max
TRHBUL	(6)	$\overline{BUSY}$ low after $\overline{RD}$ high	35	40	40	ns	max
TEHAX	(5)	Address hold time	0	0	0	ns	min
TRHAX	(6)	Address hold time	0	0	0	ns	min
TEHQZ	(5)	Chip select disable time	25	30	35	ns	max
TRHQZ	(6)	$\overline{RD}$ high to output in HZ	25	30	35	ns	max
TAVLL		Address set up to ALE	15	20	25	ns	min
TLLAX		Address hold time	10	15	20	ns	min
TEHBUHC	(1) (5) (2) (5)	$\overline{BUSY}$ high after $\overline{CE}$ high when contention	25 95	30 120	35 145	ns ns	max max
TRHBUHC	(1) (6) (2) (6)	$\overline{BUSY}$ high after $\overline{RD}$ high when contention	45 95	50 120	50 145	ns ns	max max
TLLRL		ALE to $\overline{RD}$ low	10	15	20	ns	min

Note 1: Mode 1 with "beginning" option
Note 2: Mode 1 with "end" option
Note 3: $\overline{RD}$ low prior to $\overline{CE}$
Note 4: $\overline{CE}$ low prior to $\overline{RD}$
Note 5: $\overline{CE}$ high prior to $\overline{RD}$
Note 6: $\overline{RD}$ high prior to $\overline{CE}$

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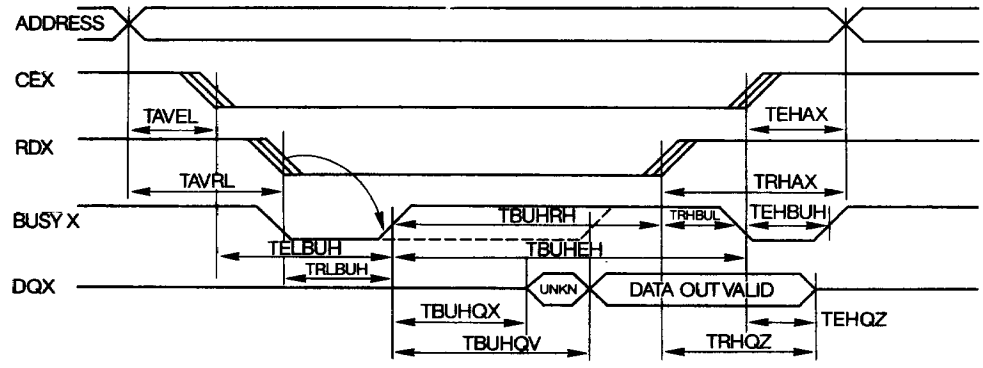
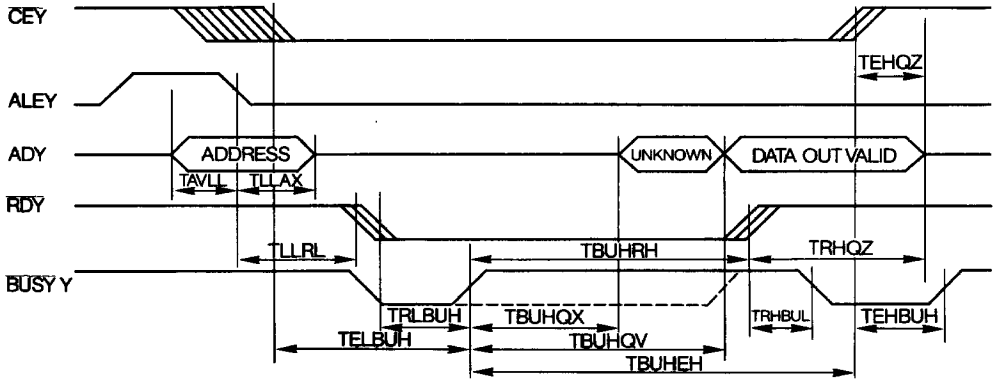
MODE 1: READ CYCLE

TIMING DIAGRAM OF READ OPERATION FROM PORT X WITHOUT CONTENTION



TIMING DIAGRAM OF READ OPERATION FROM PORT Y WITHOUT CONTENTION



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MODE 1: ASYNCHRONOUS MODE

AC PARAMETERS

AC test Conditions:

- VCC = 5 V ± 10 %
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

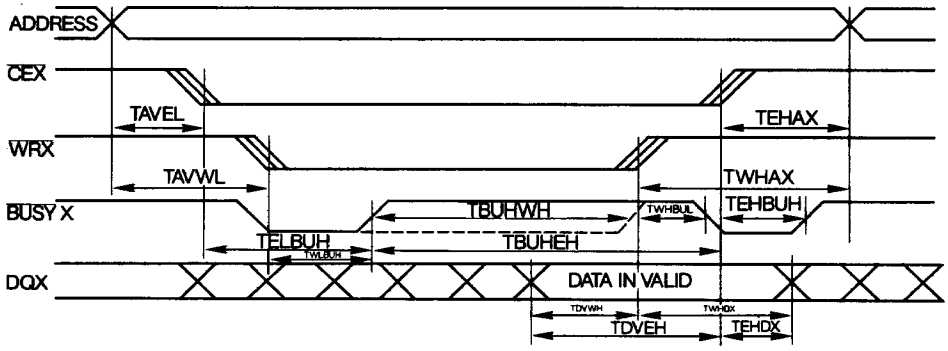
MODE 1: WRITE CYCLE

SYMBOL		PARAMETER	-5	-9	-2	Unit	Value
TAVEL	(3)	Address set up time	0	0	0	ns	min
TAVWL	(4)	Address set up time	0	0	0	ns	min
TELBUH	(1) (3) (2) (3)	$\overline{BUSY}$ high after $\overline{CE}$ low	65 130	70 140	70 140	ns ns	max max
TWLBUH	(1) (4) (2) (4)	$\overline{BUSY}$ high after $\overline{WR}$ low	65 130	70 140	70 140	ns ns	max max
TBUHEH	(1) (2)	$\overline{CE}$ high after $\overline{BUSY}$ high	20 0	30 0	35 0	ns ns	min max
TBUHWH	(1) (2)	$\overline{WR}$ high after $\overline{BUSY}$ high	20 0	30 0	35 0	ns ns	min min
TEHBUH	(5)	$\overline{BUSY}$ high after $\overline{CE}$ high	30	35	35	ns	max
TWHBUL	(6)	$\overline{BUSY}$ low after $\overline{WR}$ high	25	30	35	ns	max
TEHAX	(5)	Address hold time	0	0	0	ns	min
TWHAX	(6)	Address hold time	0	0	0	ns	min
TEHDX	(5)	Data hold time	25	30	35	ns	min
TWHDX	(6)	Data hold time	15	15	15	ns	min
TAVLL		Address set up to ALE	15	20	25	ns	min
TLLAX		Address hold time	10	15	20	ns	min
TEHBUHC	(1) (5) (2) (5)	$\overline{BUSY}$ high after $\overline{CE}$ high when contention	25 95	30 120	35 145	ns ns	max max
TWHBUHC	(1) (6) (2) (6)	$\overline{BUSY}$ high after $\overline{WR}$ high when contention	25 95	45 120	50 145	ns ns	max max
TLLWL		ALE to $\overline{WR}$ low	10	15	20	ns	min
TDVEH	(5)	Input data valid to end of chip select	25	30	35	ns	min
TDVWH	(5)	Input data valid to end of write	20	30	30	ns	min

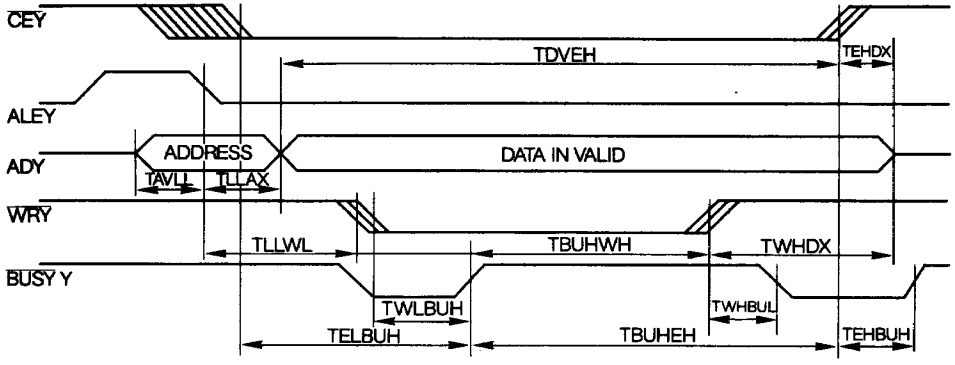
Note 1: Mode 1 with "beginning" option
Note 2: Mode 1 with "end" option
Note 3: $\overline{WR}$ low prior to $\overline{CE}$
Note 4: $\overline{CE}$ low prior to $\overline{WR}$
Note 5: $\overline{CE}$ high prior to $\overline{WR}$
Note 6: $\overline{WR}$ high prior to $\overline{CE}$

MODE 1: WRITE CYCLE

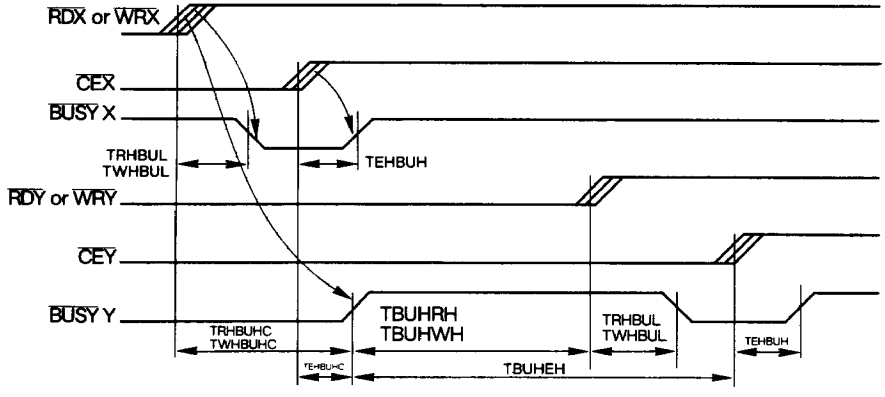
TIMING DIAGRAM OF WRITE OPERATION FROM PORT WITHOUT CONTENTION



TIMING DIAGRAM OF WRITE OPERATION FROM PORT Y WITHOUT CONTENTION



TIMING DIAGRAM OF READ OR WRITE OPERATION WITH CONTENTION (PORT X VALID FIRST)



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MODE 2: SYNCHRONOUS MODE

AC PARAMETERS

AC test Conditions :

- VCC = 5 V ± 10%
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

MODE 2: READ CYCLE

SYMBOL	PARAMETER	-5	-9	-2	Unit	Value
T	Period	80	100	120	ns	min
TELLL	$\overline{CE}$ set up to ALE	10	15	20	ns	min
TEHQZ (1)	Chip select disable time	25	30	35	ns	max
TRHQZ (2)	$\overline{RD}$ high to output in HZ	25	30	35	ns	max
TLLAX	Address hold time	10	15	20	ns	min
TAVLL	Address set up time	15	20	25	ns	min
TLLRL	ALE to $\overline{RD}$ low	10	15	20	ns	min
TEHBUH (1)	$\overline{BUSY}$ high after $\overline{CE}$ high	30	35	35	ns	max
TRHBUH (2)	$\overline{BUSY}$ high after $\overline{RD}$ high	45	50	50	ns	max
TELQX (3)	$\overline{CE}$ low to output in low Z	50	60	70	ns	min
TELQV (3)	$\overline{CE}$ access time	80	100	120	ns	max
TRLQX (4)	$\overline{RD}$ low to output in low Z	50	60	70	ns	min
TRLQV (4)	$\overline{RD}$ access time	80	100	120	ns	max
TBUHQX	$\overline{BUSY}$ high to output active	25	30	35	ns	min
TBUHQV	Data valid after $\overline{BUSY}$ high	55	70	85	ns	max
TBUHEH (1)	$\overline{CE}$ high after $\overline{BUSY}$ high	55	70	85	ns	min
TBUHRH (2)	$\overline{RD}$ high after $\overline{BUSY}$ high	55	70	85	ns	min
TCLEH (1)	$\overline{CE}$ high delay	80	100	120	ns	min
TCLRH (2)	$\overline{RD}$ high delay	80	100	120	ns	min
TCLQV	Port Y access time	80	100	120	ns	max

Note 1 : $\overline{CE}$ high prior to $\overline{RD}$
Note 2 : $\overline{RD}$ high prior to $\overline{CE}$
Note 3 : $\overline{RD}$ low prior to $\overline{CE}$
Note 4 : $\overline{CE}$ low prior to $\overline{RD}$

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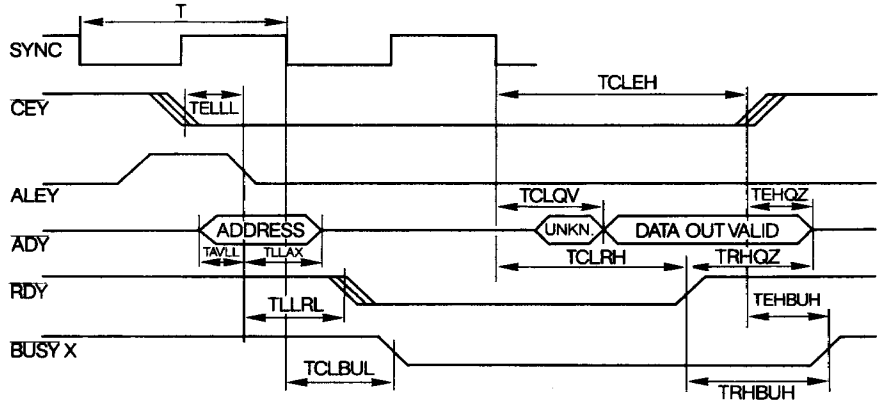
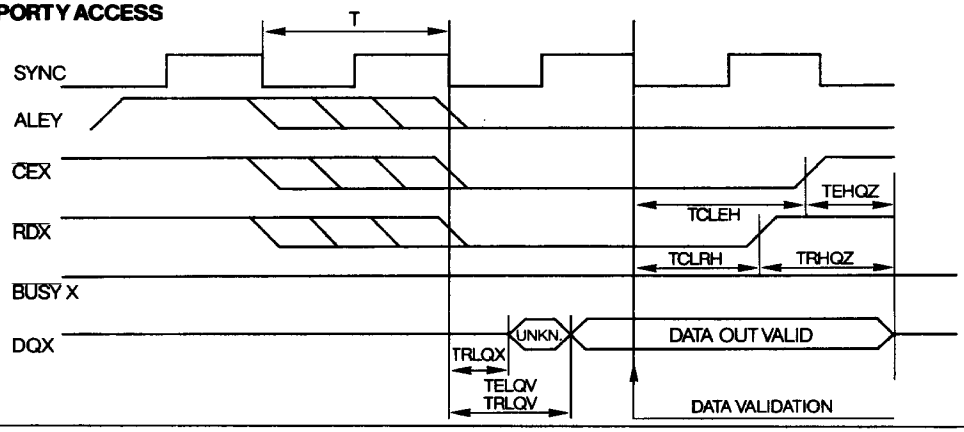
MODE 2: READ CYCLE

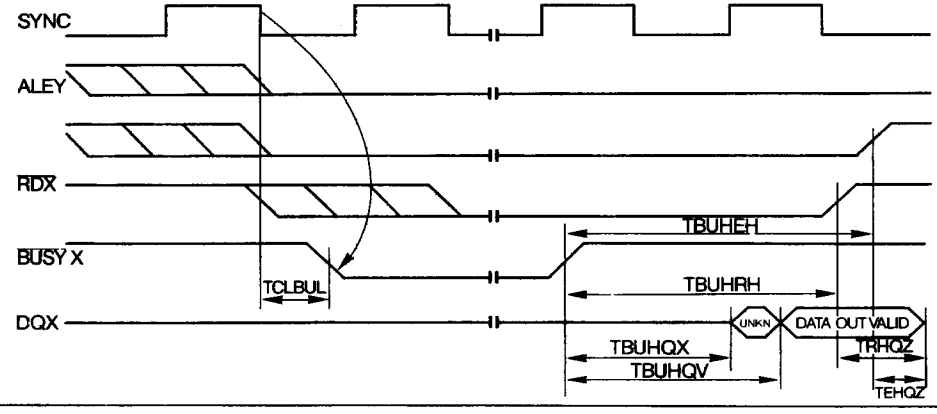
TIMING DIAGRAM OF READ OPERATION FROM PORT Y



TIMING DIAGRAM WHEN A READ OPERATION IS COMPLETED FROM PORT X PRIOR TO PORT Y ACCESS



TIMING DIAGRAM WHEN A READ OPERATION IS NOT COMPLETED FROM PORT X PRIOR TO PORT Y ACCESS



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MODE 2: SYNCHRONOUS MODE

AC PARAMETERS

AC test Conditions :

- VCC = 5 V ± 10 %
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

MODE 2: WRITE CYCLE

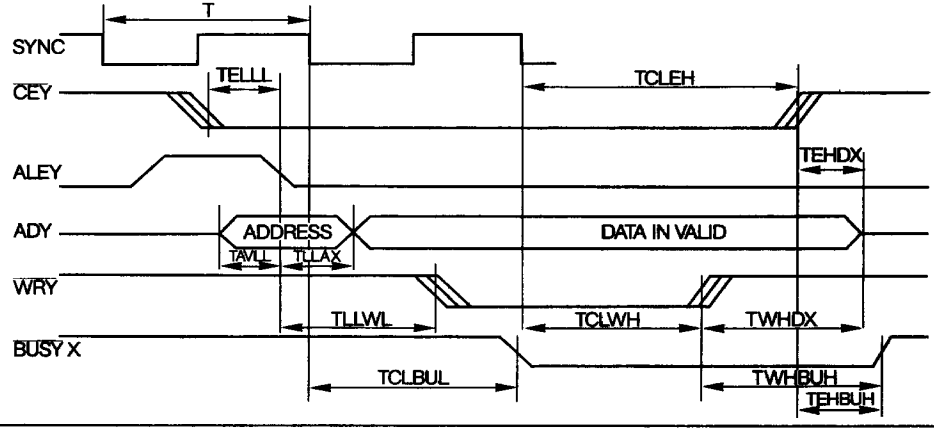
SYMBOL	PARAMETER	-5	-9	-2	Unit	Value
T	Period	80	100	120	ns	min
TELLL	$\overline{CE}$ set up to ALE	10	15	20	ns	min
TLLAX	Address hold time	10	15	20	ns	min
TAVLL	Address set up time	15	20	25	ns	min
TLLWL	ALE to $\overline{WR}$ low	10	15	20	ns	min
TEHBUH (1)	$\overline{BUSY}$ high after $\overline{CE}$ high	30	35	35	ns	max
TWHBUH (2)	$\overline{BUSY}$ high after $\overline{WR}$ high	25	45	50	ns	max
TCLBUL	$\overline{BUSY}$ Low delay	50	50	55	ns	max
TCLEH (1)	$\overline{CE}$ high delay	80	100	120	ns	min
TCLWH (2)	$\overline{WR}$ high delay	80	100	120	ns	min
TBUHEH (1)	$\overline{CE}$ high after $\overline{BUSY}$ high	55	70	85	ns	min
TBUHWH (2)	$\overline{WR}$ high after $\overline{BUSY}$ high	55	70	85	ns	min
TDVCL	Input data valid time	25	30	35	ns	min
TDVEH (1)	Input data valid to end of chip select	25	30	35	ns	min
TDVWH (2)	Input data valid to end of write	25	30	35	ns	min
TCLDX	Input data hold time	25	30	35	ns	min
TEHDX (1)	Input data hold time	25	30	35	ns	min
TWHDX (2)	Input data hold time	15	15	15	ns	min

Note 1 : $\overline{CE}$ high prior to $\overline{WR}$
Note 2 : $\overline{WR}$ high prior to $\overline{CE}$

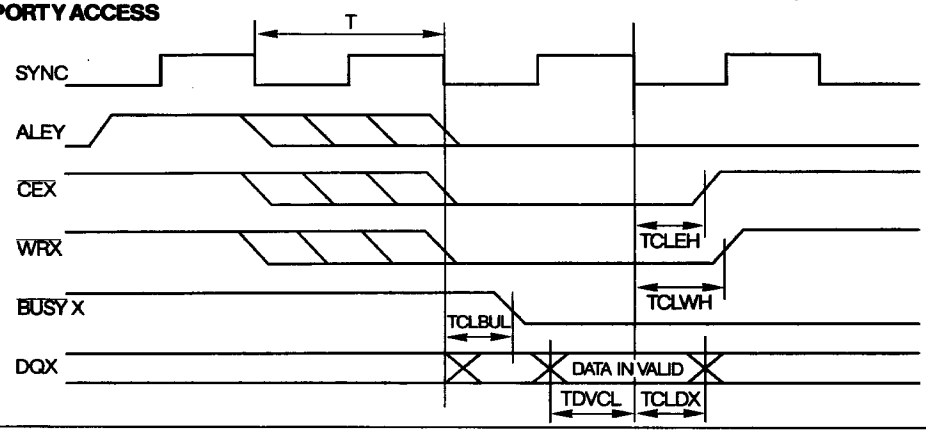
7

MODE 2: WRITE CYCLE

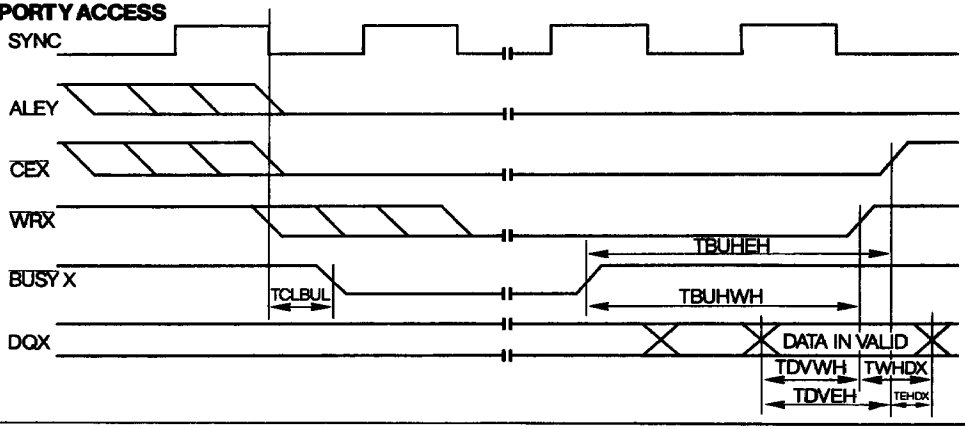
TIMING DIAGRAM OF WRITE OPERATION FROM PORT Y



TIMING DIAGRAM WHEN A WRITE OPERATION IS COMPLETED FROM PORT X PRIOR TO PORT Y ACCESS



TIMING DIAGRAM WHEN A WRITE OPERATION IS NOT COMPLETED FROM PORT X PRIOR TO PORT Y ACCESS



7

MODE 3: SOFTWARE CONTROLLED SWITCH

AC PARAMETERS

AC test Conditions :

- VCC = 5 V ± 10 %
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

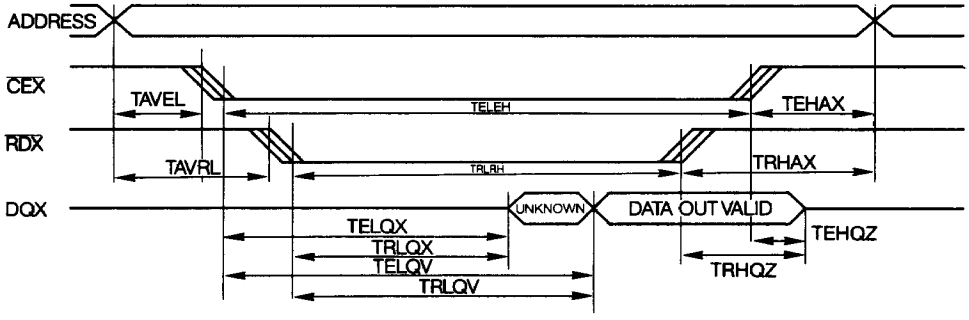
MODE 3: READ CYCLE

SYMBOL		PARAMETER	-5	-9	-2	Unit	Value
TAVEL	(3)	Address set up time	0	0	0	ns	min
TAVRL	(2)	Address set up time	0	0	0	ns	min
TELEH	(1) (3)	$\overline{CE}$ pulse width	80	100	120	ns	min
TRLRH	(1) (4)	$\overline{RD}$ pulse width	95	100	100	ns	min
TELQX	(1)	$\overline{CE}$ low to active output	50	60	70	ns	min
TRLQX	(2)	$\overline{RD}$ low to active output	50	60	70	ns	min
TELQV	(1)	$\overline{CE}$ access time	105	110	110	ns	max
TRLQV	(2)	$\overline{RD}$ access time	105	110	110	ns	max
TEHAX	(3)	Address hold time	0	0	0	ns	min
TRHAX	(4)	Address hold time	0	0	0	ns	min
TEHQZ	(3)	$\overline{CE}$ disable time	25	30	35	ns	max
TRHQZ	(4)	$\overline{RD}$ disable time	25	30	35	ns	max
TAVLL		Address set up to ALE	15	20	25	ns	min
TLLAX		Address hold time	10	15	20	ns	min
TLLRL	(2)	ALE to $\overline{RD}$ low	10	15	20	ns	min

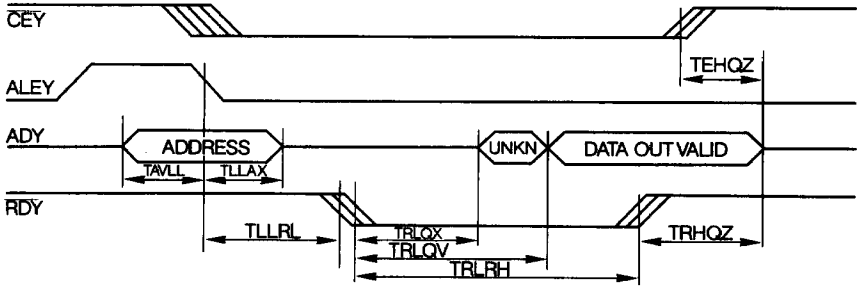
Note 1 : $\overline{RD}$ low prior to $\overline{CE}$
Note 2 : $\overline{CE}$ low prior to $\overline{RD}$
Note 3 : $\overline{CE}$ high prior to $\overline{RD}$
Note 4 : $\overline{RD}$ high prior to $\overline{CE}$

MODE 3: READ CYCLE

TIMING DIAGRAM OF READ OPERATION FROM PORT X



TIMING DIAGRAM OF A READ OPERATION FROM PORT Y



7

MODE 3: SOFTWARE CONTROLLED SWITCH

AC PARAMETERS

AC test Conditions :

- VCC = 5 V ± 10%
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

MODE 3: WRITE CYCLE

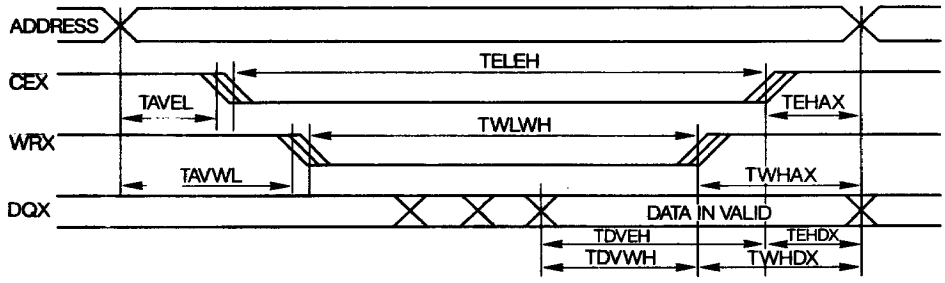
SYMBOL		PARAMETER	-5	-9	-2	Unit	Value
TEHBUL	(3)	$\overline{BUSY}$ low after $\overline{CE}$ high	85	90	95	ns	max
TWHBUL	(4)	$\overline{BUSY}$ low after $\overline{WR}$ high	85	90	95	ns	max
TEHBUH	(3)	$\overline{BUSY}$ high after $\overline{CE}$ high	85	90	95	ns	max
TWHBUH	(4)	$\overline{BUSY}$ high after $\overline{WR}$ high	85	90	95	ns	max
TAVEL	(1)	Address set up time	0	0	0	ns	min
TAVWL	(2)	Address set up time	0	0	0	ns	min
TELEH	(1) (3)	$\overline{CE}$ pulse width	80	100	120	ns	min
TWLWH	(2) (4)	$\overline{WR}$ pulse width	80	100	120	ns	min
TDVEH	(3)	Input data valid to $\overline{CE}$ high	25	30	35	ns	min
TDVWH	(4)	Input data valid to $\overline{WR}$ high	25	30	35	ns	min
TEHDX	(3)	Data hold time	25	30	35	ns	min
TWHDX	(4)	Data hold time	15	15	15	ns	min
TEHAX	(3)	Address hold time	0	0	0	ns	min
TWHAX	(4)	Address hold time	0	0	0	ns	min
TAVLL		Address set up to ALE	15	20	25	ns	min
TLLAX		Address hold time	10	15	20	ns	min
TLLWL		ALE to $\overline{WR}$ low	10	15	20	ns	min

Note 1 : $\overline{RD}$ low prior to $\overline{CE}$
Note 2 : $\overline{CE}$ low prior to $\overline{RD}$
Note 3 : $\overline{CE}$ high prior to $\overline{RD}$
Note 4 : $\overline{RD}$ high prior to $\overline{CE}$

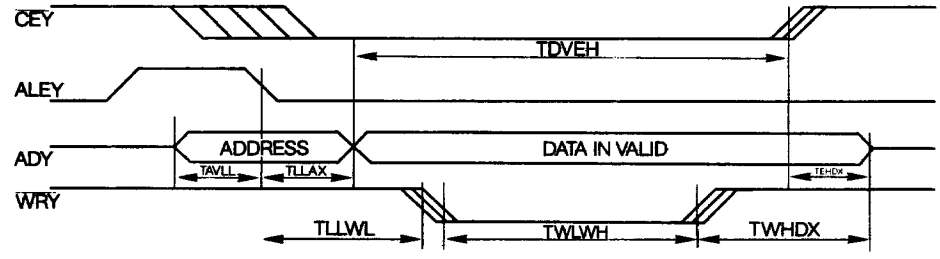
7

MODE 3: WRITE CYCLE

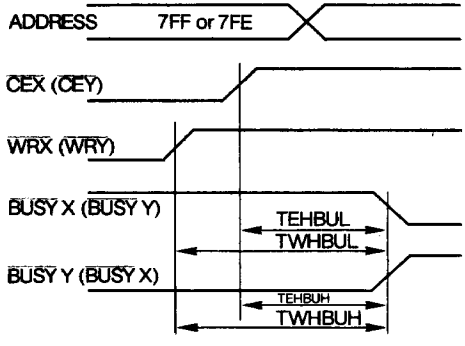
TIMING DIAGRAM OF WRITE OPERATION FROM PORT X



TIMING DIAGRAM OF A WRITE OPERATION FROM PORT Y



TIMING DIAGRAM OF A WRITE OPERATION TO THE MEMORY LOCATIONS 7FF OR 7FE



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ALL MODES

AC PARAMETERS

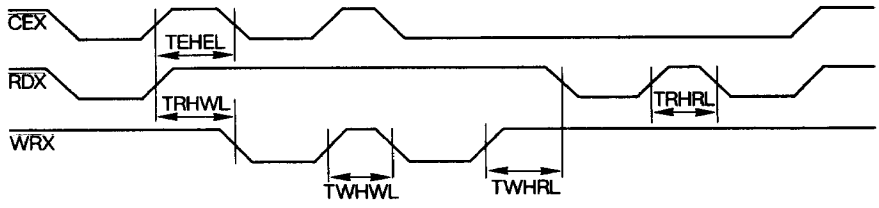
AC test Conditions :

- VCC = 5 V ± 10 %
- Input pulse levels: 0 to 3.0 V
- References levels: 1.5 V
- Output load: 1 TTL gate and CL = 100 pf (including scope and jig)
- Input rise and fall times: 10 ns

ALL MODES : READ AND WRITE CYCLES IN SEQUENCES

SYMBOL	PARAMETER	-5	-9	-2	Unit	Value
TEHEL (1) (3)	Delay between chip selections	10	15	20	ns	min
TRHWL (2) (4)	Delay between a read and a write cycle	10	15	20	ns	min
TWHWL (2) (4)	Delay between write cycles	10	15	20	ns	min
TWHRL (2) (4)	Delay between a write and a read cycle	10	15	20	ns	min
TRHRL (2) (4)	Delay between read cycles	10	15	20	ns	min

TIMING DIAGRAM OF READ AND WRITE CYCLES IN SEQUENCE FROM PORT X

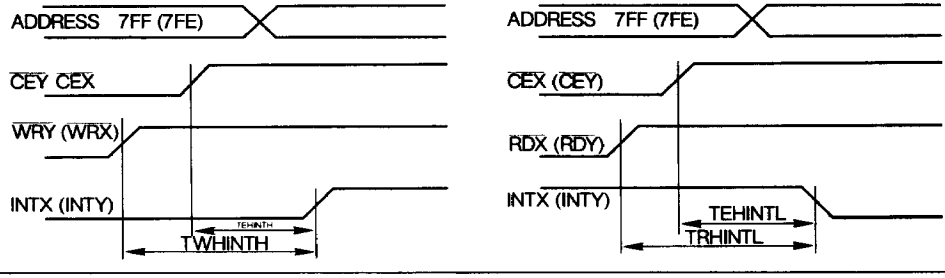


ALL MODES : INTERRUPT REQUEST

SYMBOL	PARAMETER	-5	-9	-2	Unit	Value
TEHINTH (1) (3)	INT high after $\overline{CE}$ high	40	45	50	ns	max
(2) (3)		85	90	95	ns	max
TWHINTH (1) (4)	INT high after $\overline{WR}$ high	40	45	50	ns	max
(2) (4)		85	90	95	ns	max
TEHINTL (1) (3)	INT low after $\overline{CE}$ high	40	45	50	ns	max
(2) (3)		85	90	95	ns	max
TRHINTL (1) (4)	INT low after $\overline{RD}$ high	40	45	50	ns	max
(2) (4)		85	90	95	ns	max

Note 1 : Mode 1 and 2
Note 2 : Mode 3
Note 3 : $\overline{CE}$ high prior to $\overline{RD}$ or $\overline{WR}$
Note 4 : $\overline{RD}$ or $\overline{WR}$ high prior to $\overline{CE}$

TIMING DIAGRAM FOR INTERRUPT REQUEST FOR ALL MODE



ORDERING INFORMATION

DEVICE TYPE	PACKAGE	TEMPERATURE RANGE
HM1 – 65231 – 2	CERAMIC DIL	– 55 °C to + 125 °C
HM1 – 65231 – 8	CERAMIC DIL	– 55 °C to + 125 °C
HM1 – 65231 – 9	CERAMIC DIL	– 40 °C to + 85 °C
HM3 – 65231 – 5	PLASTIC DIL	0 °C to + 70 °C
HM3 – 65231 – 9	PLASTIC DIL	– 40 °C to + 85 °C
HMS – 65231 – 5	PLASTIC LCC 68 PINS	0 °C to + 70 °C

HMS – 65231 – 5

– 5 → TEMPERATURE RANGE (– 2, – 5, – 8, – 9)

– 65231 → DEVICE TITLE

HMS → PACKAGE (1, 3, 4, S)

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	65231 – 5		65231 – 9		65213 – 2		UNIT
			min	max	min	max	min	max	
VCC for data retention	VCCDR	CS = VCC VIN = OV or VCC	2	–	2	–	2	–	V
Data retention current	ICCDR	VCC = 2. OV. CS = VCC VIN = OV or VCC	–	40	–	140	–	400	μA
Operating recovery time	TR		TAVAV		TAVAV		TAVAV		

TAVAV = read cycle time