MATRA M H S

Preliminary

September 1990

T-46-23-13

DATA SHEET

HM 65756

32 K x 8 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45//55 ns (max)
  COMMERCIAL : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 825 mW
  STANDBY : 193 mW
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **OUTPUT ENABLE**
- **SINGLE 5 VOLT SUPPLY**

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DESCRIPTION

The HM-65756 is a high speed CMOS static RAM organised as 32,768 X 8 bits. It is manufactured using MHS's high performance CMOS technology.

Access time as fast as 25 ns are available with maximum power consumption of only 825 mW.

The HM-65756 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) an active low output enable (OE), and three state drivers.

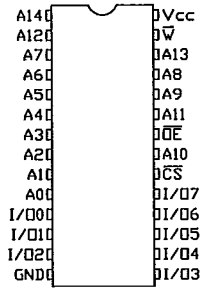
All inputs or outputs of the HM-65756 are TTL compatible and operate from single 5 V supply thus simplifying system design.

The HM-65756 is processed following the test methods of MIL STD 883C.

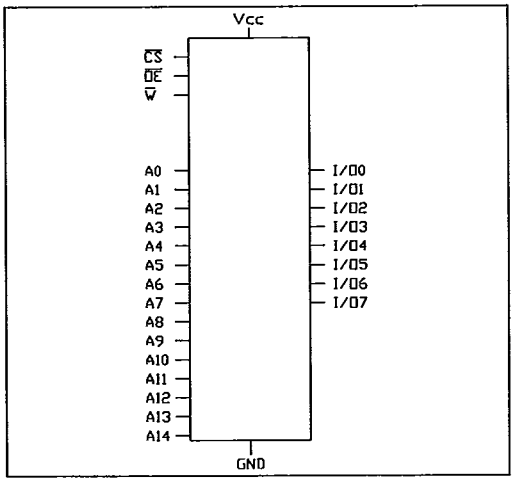
PACKAGES

Plastic 300 and 600 mils, 28 pins, DIL.
Ceramic 300 and 600 mils, 28 pins, DIL.
SOIC 300, 28 pins.
SOJ 300 mils, 28 pins.
LCC 28 pins and 32 pins.
Tape and Reel Service.

Pinout DIL 28 pins



LOGIC SYMBOL



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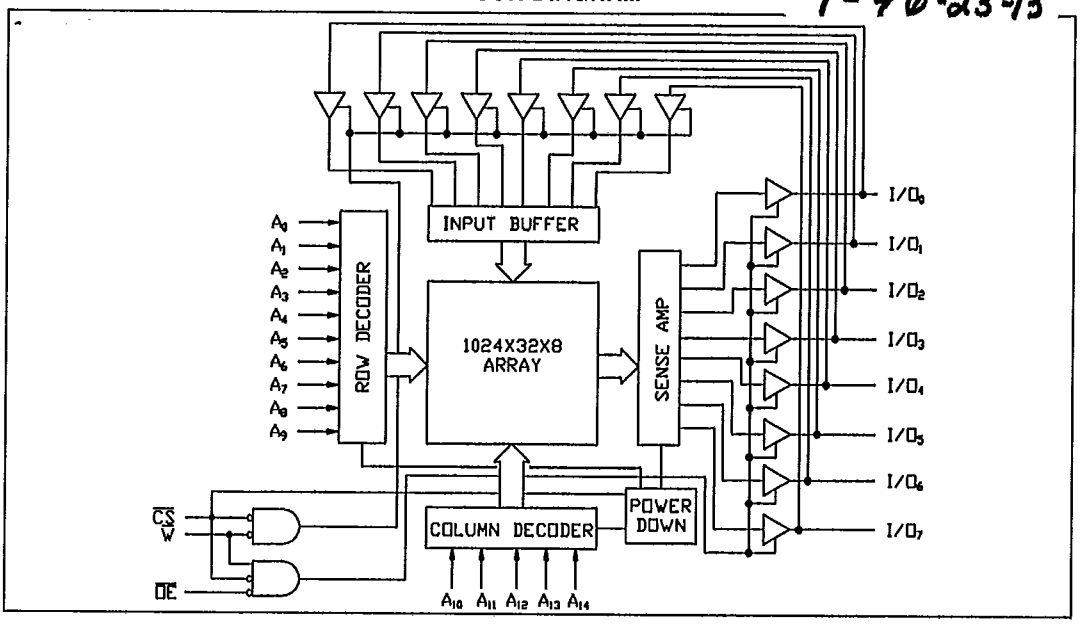
BLOCK DIAGRAM



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PIN NAMES

A0-A14	: Address inputs	$\overline{CS}$	: Chip Select
I/00-I/07	: Inputs/Outputs	$\overline{OE}$	: Output enable
VCC	: Power	$\overline{W}$	: Write enable
GND	: Ground		

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	INPUT/OUTPUT	MODE
H	X	X	Z	Deselect/Power down
L	L	H	Output	Read
L	X	L	Input	Write
L	H	H	Z	Output Disable

L = Low, H = High, X = H or L, Z = High Impedance.

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ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential..... – 0.5 V to + 7.0 V
DC input voltage..... – 3.0 V to + 7.0 V
DC output voltage in high Z state .... – 0.5 V to + 7.0 V
Storage temperature ..... – 65°C to + 150°C
Output current into outputs (low) ..... 20 mA
Electro static discharge voltage ..... 2000 V (MIL STD 883C method 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, V_{CC} = 5.0 V, these parameters are not tested.

AC TEST LOADS AND WAVEFORMS

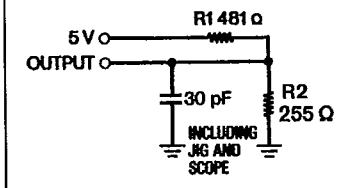


Figure 1a

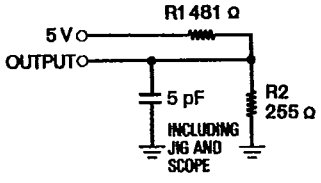


Figure 1b

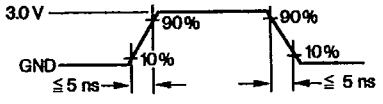
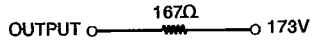


Figure 2

Equivalent to : THEVENIN EQUIVALENT



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ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	−10.0	–	10.0	µA
IOZ	(3)	Output leakage current	−10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	−300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = −4.0 mA.

CONSUMPTION FOR COMMERCIAL (– 5) SPECIFICATION :

SYMBOL		PARAMETER	65756 H-5	65756 K-5	65756 M-5	65756 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	35	35	35	35	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	170	150	150	150	mA	max

CONSUMPTION FOR INDUSTRIAL (– 9) AND MILITARY (- 2) SPECIFICATION :

SYMBOL		PARAMETER	65756 K-9/-2	65756 M-9/-2	65756 N-9/-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	35	35	35	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	160	160	160	mA	max

Notes : 6. $\overline{CS} \geq VIH$, a pull-up resistor to Vcc on the $\overline{CS}$ is required to keep the device unselected during the Vcc power-up. Othewise ICCSB will exceed the above value. Min duty cycle = 100 %.
7. $\overline{CS} \geq Vcc - 0.3$ V.
8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

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ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels	Gnd to 3.0 V	Input timing reference levels	1.5 V
Input rise	5 ns	Output loading IOL/IOH (see figure 1a and 1b)	+ 30 pF

WRITE CYCLE specification : Commercial, Industrial and Military

SYMBOL	PARAMETER	65756 H-5/-9/-2	65756 K-5/-9/-2	65756 M-5/-9/-2	65756 N-5/-9/-2	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address Valid to write end	20	30	40	50	ns	min
TDVWH	Data set-up time	15	17	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	13	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	40	ns	min
TWHAX	Address hold from write end	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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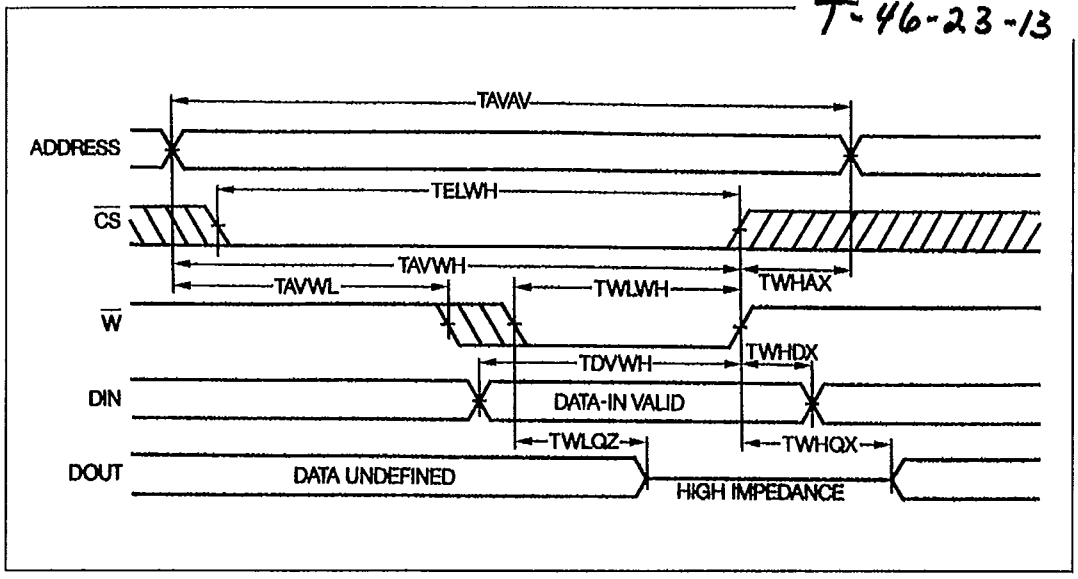
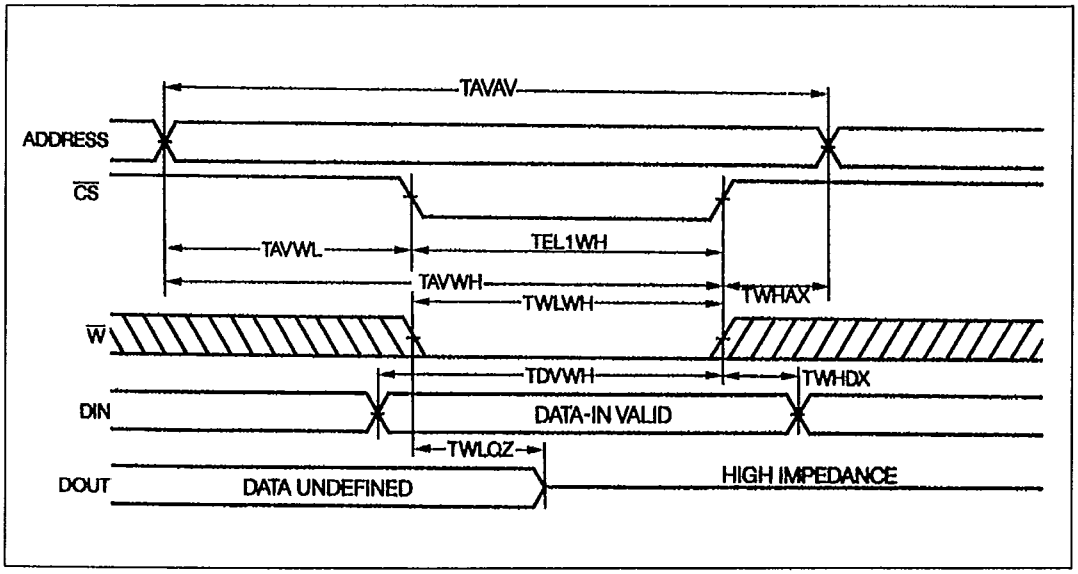
WRITE CYCLE 1 : $\overline{W}$ controlled (note 9)



WRITE CYCLE 2 : $\overline{CS}$ controlled (note 9)



Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write. Data out will be high impedance if $\overline{OE}$ = VIH.

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READ CYCLE specification : Commercial, Industrial and Military

SYMBOL	PARAMETER	65756 H-5	65756 K-5/-9/-2	65756 M-5/-9/-2	65756 N-5/-9/-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address Valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	13	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	15	20	20	20	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	13	15	20	25	ns	max

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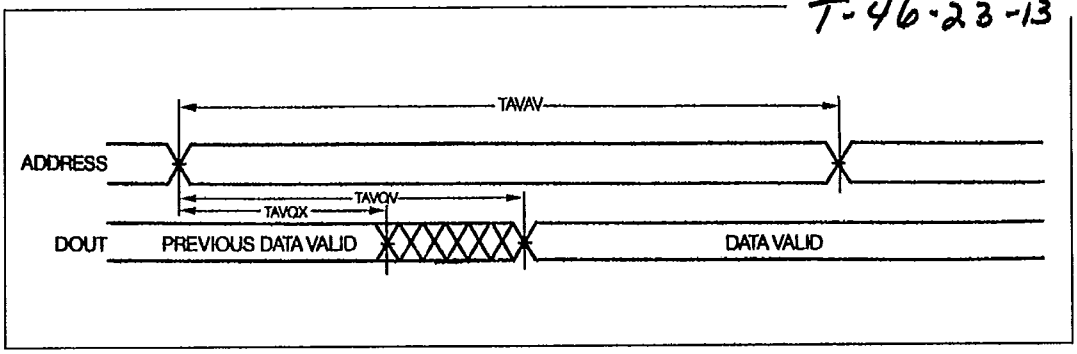
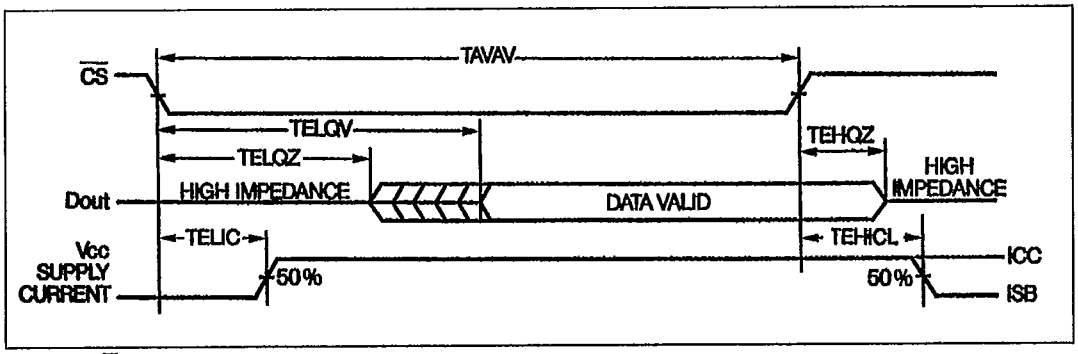
READ CYCLE 1 : (note 10, 11, 12)



READ CYCLE 2 : (note 10, 12)



Notes : 10. $\overline{W}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
12. Address valid prior or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION

Package	Device Type	Grade	Level
HM1	65756	K	–5 : R
0 - Chip form 1 - Ceramic 28 pins 300 mils 1E - Ceramic 28 pins 600 mils 3 - Plastic 28 pins 300 mils 3E - Plastic 28 pins 600 mils 4P - LCC 28 pins/4J - LCC 32 pins T - SOIC 28 pins 300 mils U - SOJ 28 pins	32 k x 8 high speed static RAM	H = 25 ns K = 35 ns M = 45 ns N = 55 ns	–5 : Commercial –9 : Industrial –2 : Military –8 : Military with B.I Tape & Reel Service (B.I : Burn-In)