
HM5116160 Series

HM5118160 Series

16 M FP DRAM (1-Mword $\times$ 16-bit)
4 k Refresh/1 k Refresh

HITACHI

ADE-203-634E (Z)
Rev. 5.0
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Description

The Hitachi HM5116160 Series, HM5118160 Series are CMOS dynamic RAMs organized as 1,048,576-word $\times$ 16-bit. They employ the most advanced CMOS technology for high performance and low power. The HM5116160 Series, HM5118160 Series offer Fast Page Mode as a high speed access mode. They have package variations of 42-pin plastic SOJ and 50-pin plastic TSOP II.

Features

- Single 5 V ($\pm 10\%$)
- Access time: 60 ns/70 ns (max)
- Power dissipation
 - Active mode : 550 mW/495 mW (max) (HM5116160 Series)
935 mW/825 mW (max) (HM5118160 Series)
 - Standby mode : 11 mW (max)
: 0.83 mW (max) (L-version)
- Fast page mode capability
- Refresh cycles
 - 4096 refresh cycles : 64 ms (HM5116160 Series)
: 128 ms (L-version)
 - 1024 refresh cycles : 16 ms (HM5118160 Series)
: 128 ms (L-version)
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)
- $2\overline{\text{CAS}}$ -byte control
- Battery backup operation (L-version)

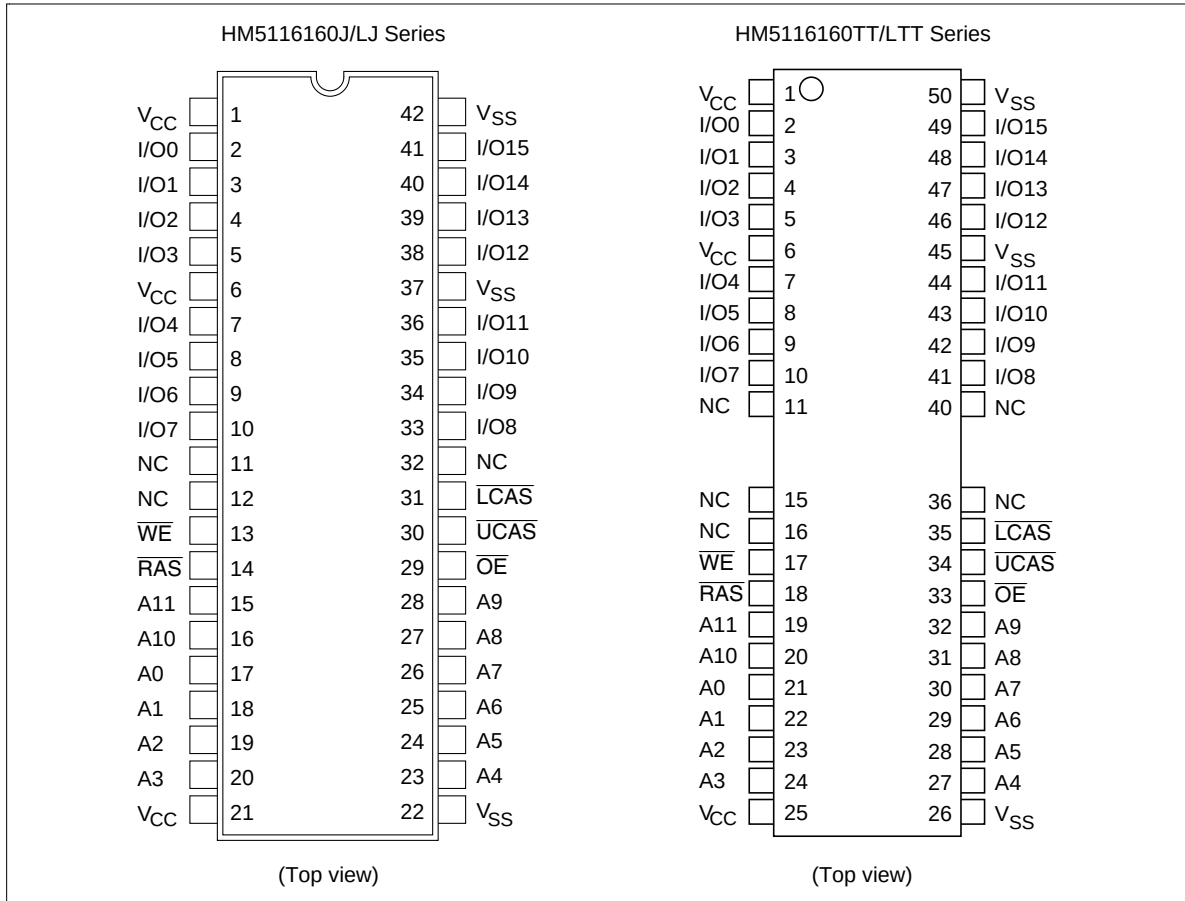
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Ordering Information

Type No.	Access time	Package
HM5116160J-6	60 ns	400-mil 42-pin plastic SOJ (CP-42D)
HM5116160J-7	70 ns	
HM5116160LJ-6	60 ns	
HM5116160LJ-7	70 ns	
HM5118160J-6	60 ns	
HM5118160J-7	70 ns	
HM5118160LJ-6	60 ns	
HM5118160LJ-7	70 ns	
HM5116160TT-6	60 ns	400-mil 50-pin plastic TSOP II (TTP-50/44DC)
HM5116160TT-7	70 ns	
HM5116160LTT-6	60 ns	
HM5116160LTT-7	70 ns	
HM5118160TT-6	60 ns	
HM5118160TT-7	70 ns	
HM5118160LTT-6	60 ns	
HM5118160LTT-7	70 ns	

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Pin Arrangement

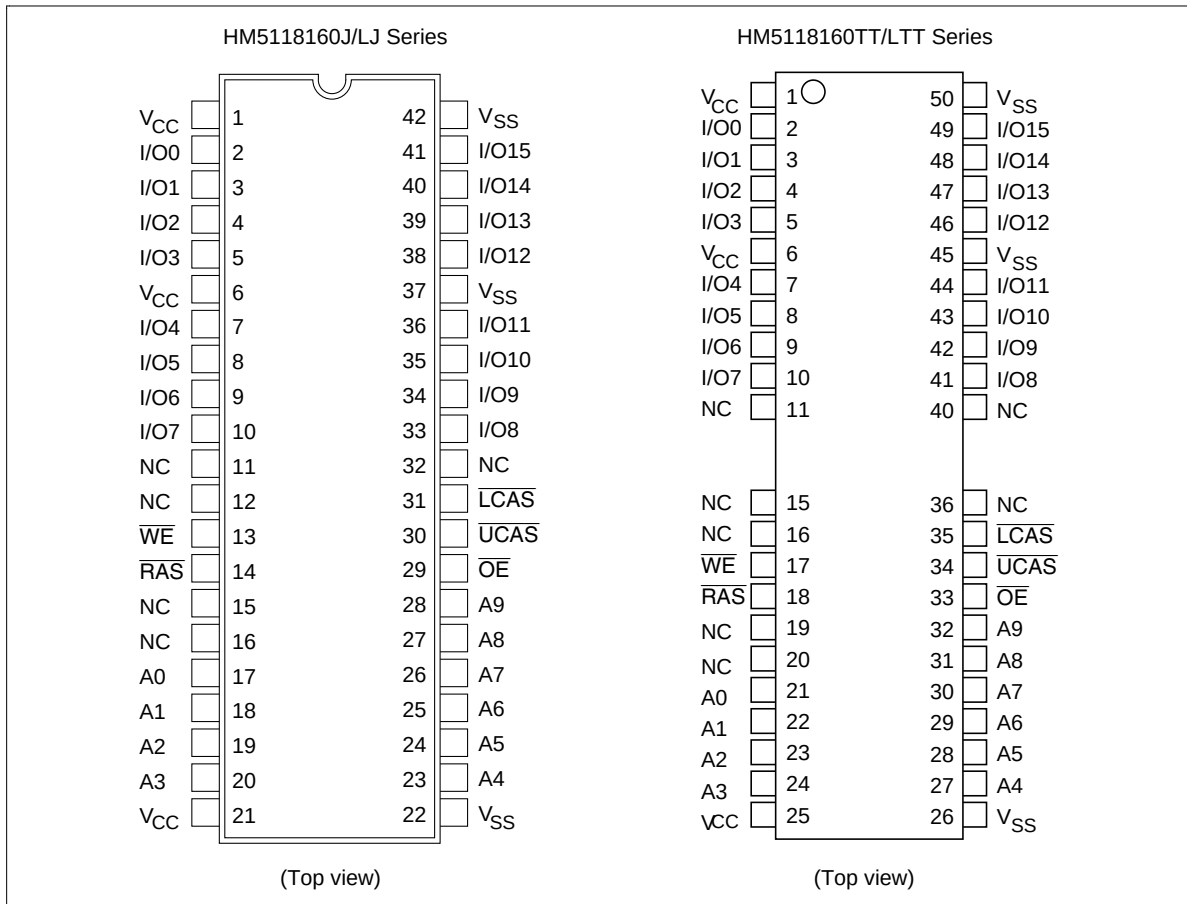


Pin Description

Pin name	Function
A0 to A11	Address input - Row/Refresh address A0 to A11 - Column address A0 to A7
I/O0 to I/O15	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

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Pin Arrangement

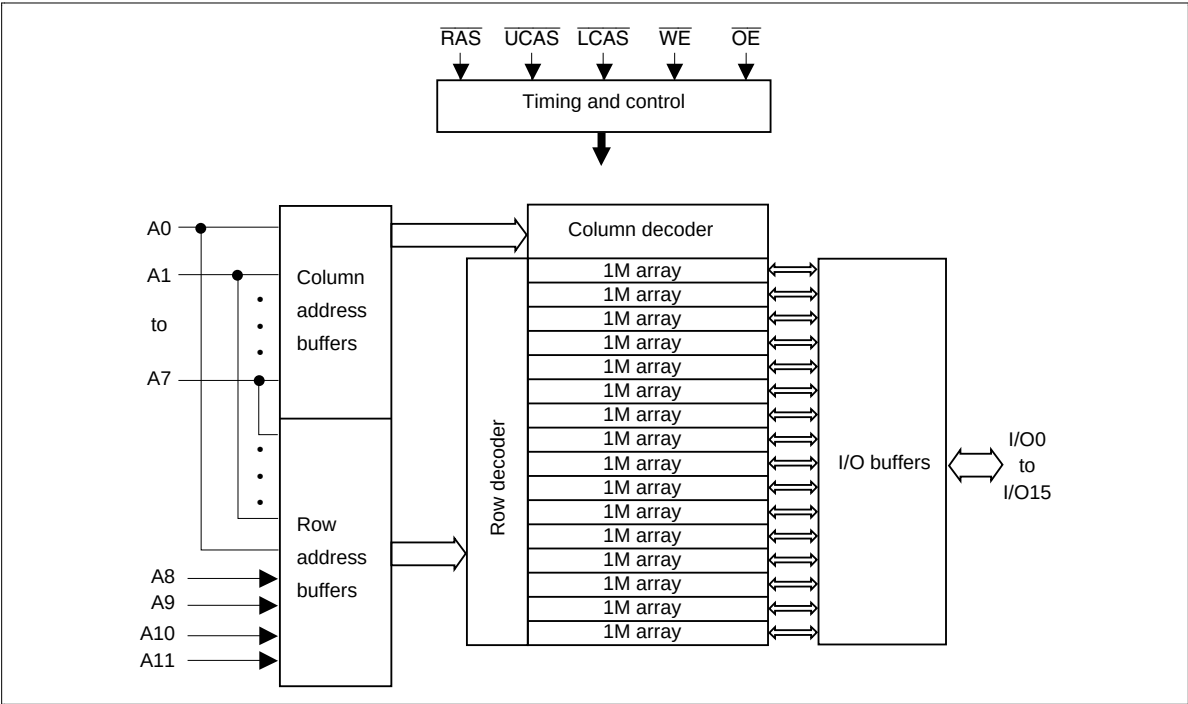


Pin Description

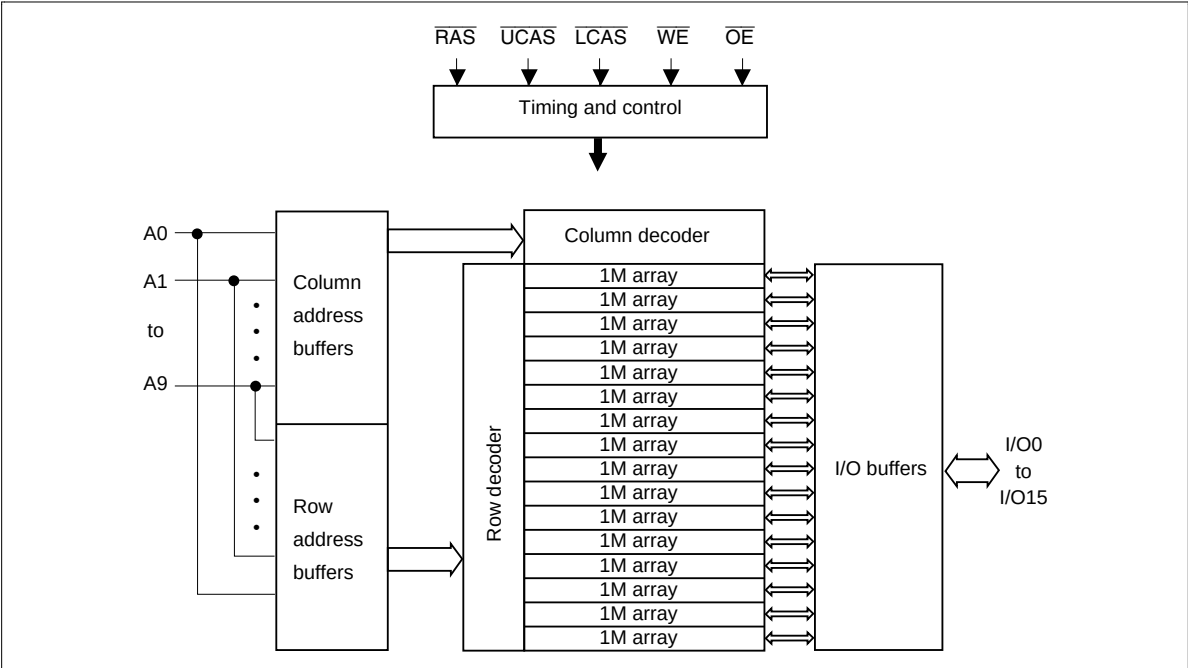
Pin name	Function
A0 to A9	Address input - Row/Refresh address A0 to A9 - Column address A0 to A9
I/O0 to I/O15	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

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Block Diagram (HM5116160 Series)



Block Diagram(HM5118160 Series)



Truth Table

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$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output		Operation
H	D	D	D	D	Open		Standby
L	L	H	H	L	Valid	Lower byte	Read cycle
L	H	L	H	L	Valid	Upper byte	
L	L	L	H	L	Valid	Word	
L	L	H	L^{*2}	D	Open	Lower byte	Early write cycle
L	H	L	L^{*2}	D	Open	Upper byte	
L	L	L	L^{*2}	D	Open	Word	
L	L	H	L^{*2}	H	Undefined	Lower byte	Delayed write cycle
L	H	L	L^{*2}	H	Undefined	Upper byte	
L	L	L	L^{*2}	H	Undefined	Word	
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write cycle
L	H	L	H to L	L to H	Valid	Upper byte	
L	L	L	H to L	L to H	Valid	Word	
L	H	H	D	D	Open	Word	$\overline{\text{RAS}}$ -only refresh cycle
H to L	H	L	D	D	Open	Word	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or
H to L	L	H	D	D	Open	Word	Self refresh cycle (L-version)
H to L	L	L	D	D	Open	Word	
L	L	L	H	H	Open		Read cycle (Output disabled)

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2. $t_{\text{WCS}} \geq 0 \text{ ns}$ Early write cycle

$t_{\text{WCS}} < 0 \text{ ns}$ Delayed write cycle

3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by the earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edge.) However write OPERATION and output High-Z control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.

ex. if $\overline{\text{RAS}} = \text{H to L}$, $\overline{\text{UCAS}} = \text{H}$, $\overline{\text{LCAS}} = \text{L}$, then $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle is selected.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}
 2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (HM5116160 Series)

		HM5116160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I _{CC1}	—	100	—	90	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	μA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current ^{*2}	I _{CC3}	—	100	—	90	mA	t _{RC} = min
Standby current ^{*1}	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	100	—	90	mA	t _{RC} = min
Fast page mode current ^{*1, *3}	I _{CC7}	—	95	—	85	mA	t _{PC} = min
Battery backup current ^{*4} (Standby with CBR refresh) (L-version)	I _{CC10}	—	500	—	500	μA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	300	—	300	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL}.

3. Address can be changed once or less while UCAS and LCAS = V_{IH}.

4. V_{IH} ≥ V_{CC} − 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

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DC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) (HM5118160 Series)

		HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current ^{*1, *2}	I _{CC1}	—	170	—	150	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	μA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current ^{*2}	I _{CC3}	—	170	—	150	mA	t _{RC} = min
Standby current ^{*1}	I _{CC5}	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	170	—	150	mA	t _{RC} = min
Fast page mode current ^{*1, *3}	I _{CC7}	—	165	—	145	mA	t _{PC} = min
Battery backup current ^{*4} (Standby with CBR refresh) (L-version)	I _{CC10}	—	500	—	500	μA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 125 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	300	—	300	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{UCAS}$ and $\overline{LCAS} = V_{IH}$.

4. $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{UCAS}$ and $\overline{LCAS} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *¹, *², *¹⁸, *¹⁹, *²⁰

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	110	—	130	—	ns	
RAS precharge time	t _{RP}	40	—	50	—	ns	
CAS precharge time	t _{CP}	10	—	10	—	ns	
RAS pulse width	t _{RAS}	60	10000	70	10000	ns	
CAS pulse width	t _{CAS}	15	10000	18	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	21
Column address hold time	t _{CAH}	10	—	15	—	ns	21
RAS to CAS delay time	t _{RCD}	20	45	20	52	ns	3
RAS to column address delay time	t _{RAD}	15	30	15	35	ns	4
RAS hold time	t _{RSH}	15	—	18	—	ns	
CAS hold time	t _{CSH}	60	—	70	—	ns	
CAS to RAS precharge time	t _{CRP}	5	—	5	—	ns	22
OE to Din delay time	t _{OED}	15	—	18	—	ns	5
OE delay time from Din	t _{DZO}	0	—	0	—	ns	6
CAS delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	ns	7

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Read Cycle

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 17,
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17,
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9, 25
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12, 22
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5

Write Cycle

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	14, 21
Write command hold time	t _{WCH}	10	—	15	—	ns	21
Write command pulse width	t _{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15	—	18	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	15	—	18	—	ns	23
Data-in setup time	t _{DS}	0	—	0	—	ns	15, 23
Data-in hold time	t _{DH}	10	—	15	—	ns	15, 23

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Read-Modify-Write Cycle

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	155	—	181	—	ns	
RAS to $\overline{WE}$ delay time	t _{RWD}	85	—	98	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t _{CWD}	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time	t _{AWD}	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t _{OEh}	15	—	18	—	ns	

Refresh Cycle

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	ns	21
CAS hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	ns	22
RAS precharge to CAS hold time	t _{RPC}	5	—	5	—	ns	21

Fast Page Mode Cycle

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t _{PC}	40	—	45	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	35	—	40	ns	9, 17, 22
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	35	—	40	—	ns	

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Fast Page Mode Read-Modify-Write Cycle

		HM5116160/HM5118160					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t _{PRWC}	85	—	96	—	ns	
WE delay time from $\overline{\text{CAS}}$ precharge	t _{CPW}	60	—	68	—	ns	14, 22

Refresh (HM5116160 Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Refresh (HM5118160 Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	16	ms	1024 cycles
Refresh period (L-version)	t_{REF}	128	ms	1024 cycles

Self Refresh Mode (L-version)

		HM5116160L/HM5118160L					
		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	μs	26, 27, 28, 29
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	110	—	130	—	ns	
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	−50	—	−50	—	ns	

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- Notes:
1. AC measurements assume $t_r = 5 \text{ ns}$.
 2. An initial pause of $200 \mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 2 TTL loads and 100 pF . ($V_{\text{OH}} = 2.4 \text{ V}$, $V_{\text{OL}} = 0.4 \text{ V}$)
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASp} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 19. When both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ go low at the same time, all 16-bit data are written into the device. $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ cannot be staggered within the same write/read cycles.
 20. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 21. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 22. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 23. t_{CWL} , t_{DH} and t_{DS} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 24. t_{CP} is determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}}/V_{\text{SS}}$ line noise, which causes to degrade $V_{\text{IH min}}/V_{\text{IL max}}$ level.
 26. Please do not use t_{RASS} timing, $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} \geq 100 \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .

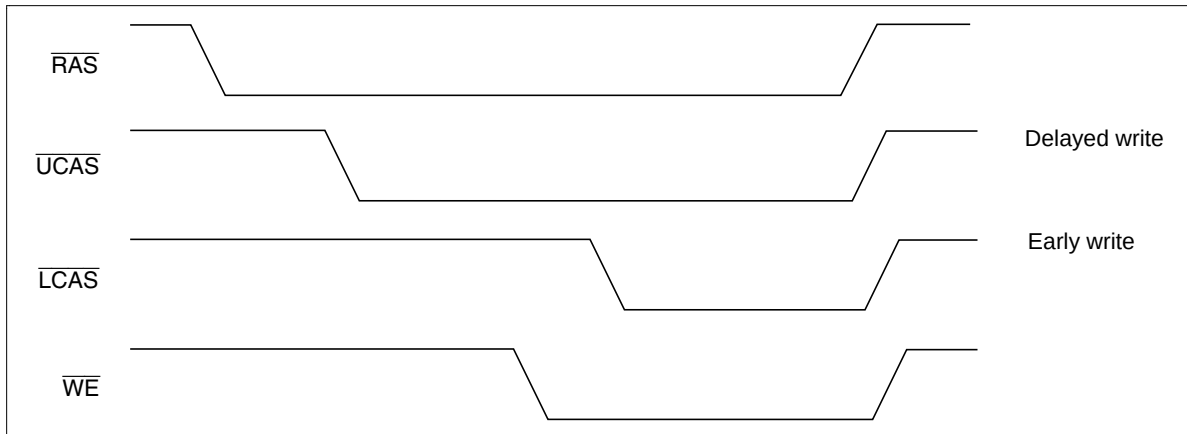
HM5116160 Series, HM5118160 Series

27. If you use distributed CBR refresh mode with 15.6 μ s interval in normal read/write cycle, CBR refresh should be executed within 15.6 μ s immediately after exiting from and before entering into self refresh mode.
28. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles (4096 cycles: HM5116160 Series, 1024 cycles: HM5118160 Series) of distributed CBR refresh with 15.6 μ s interval should be executed within 64 or 16 ms (64 ms: HM5116160, 16 ms: HM5118160) immediately after exiting from and before entering into the self refresh mode.
29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
30. XXX: H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)
/////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

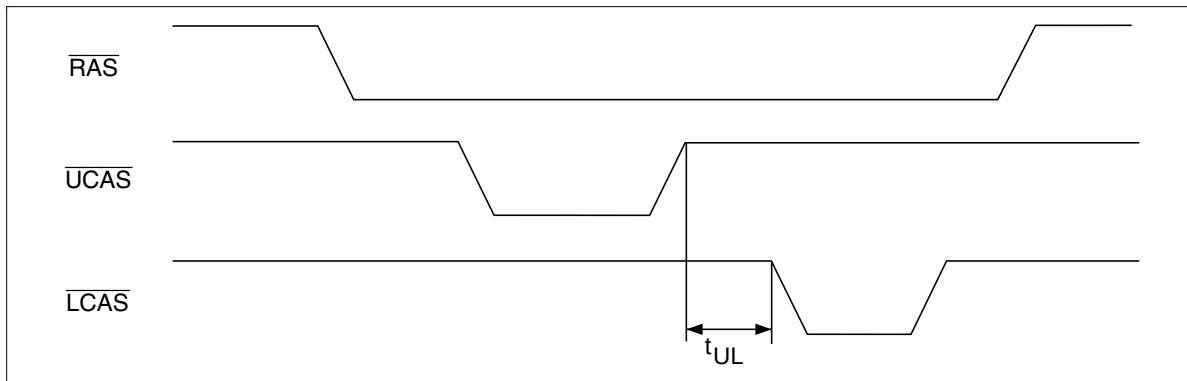
Notes concerning $\overline{2CAS}$ control

Please do not separate the $\overline{UCAS}/\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}/\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}/\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.

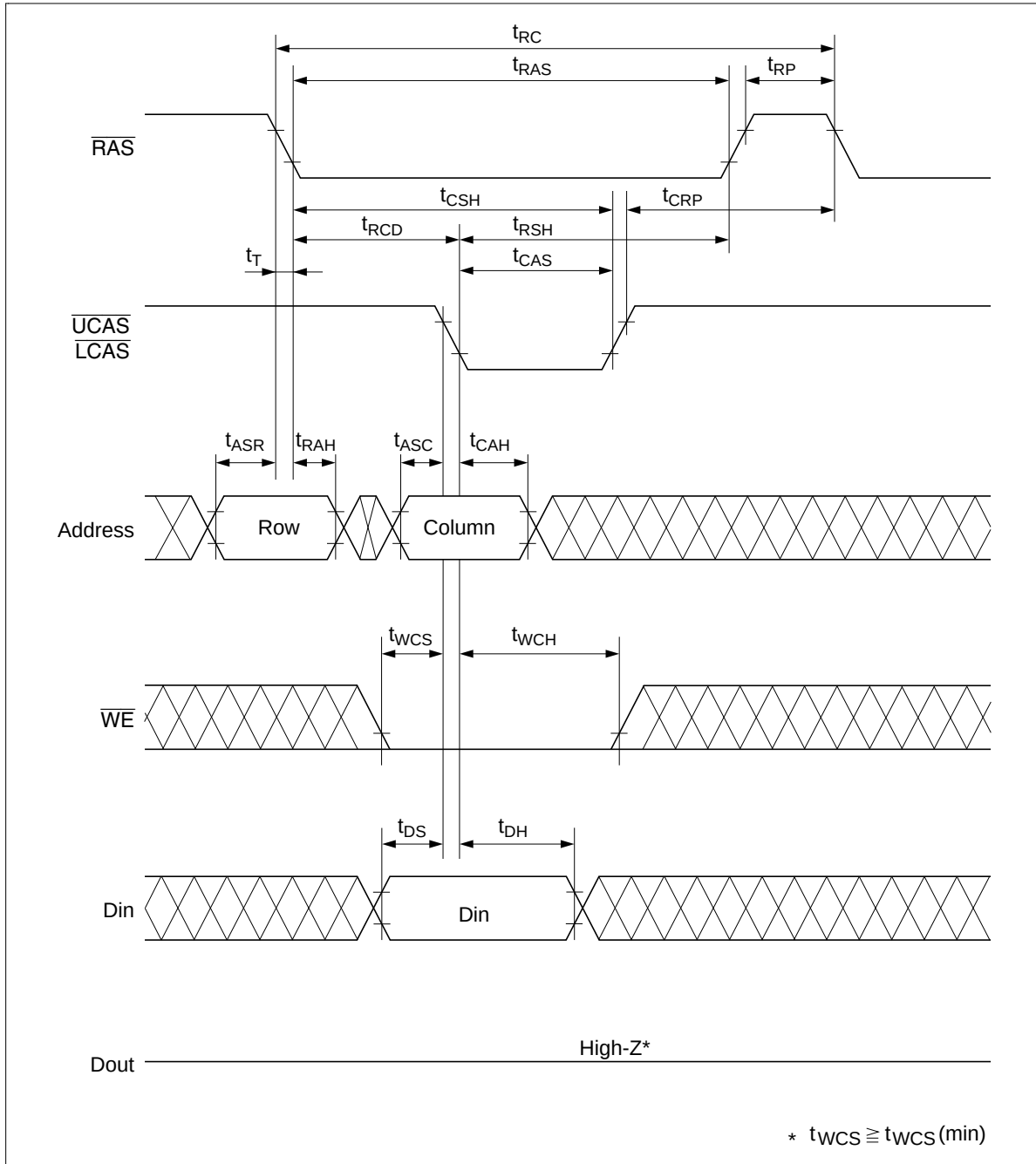


3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



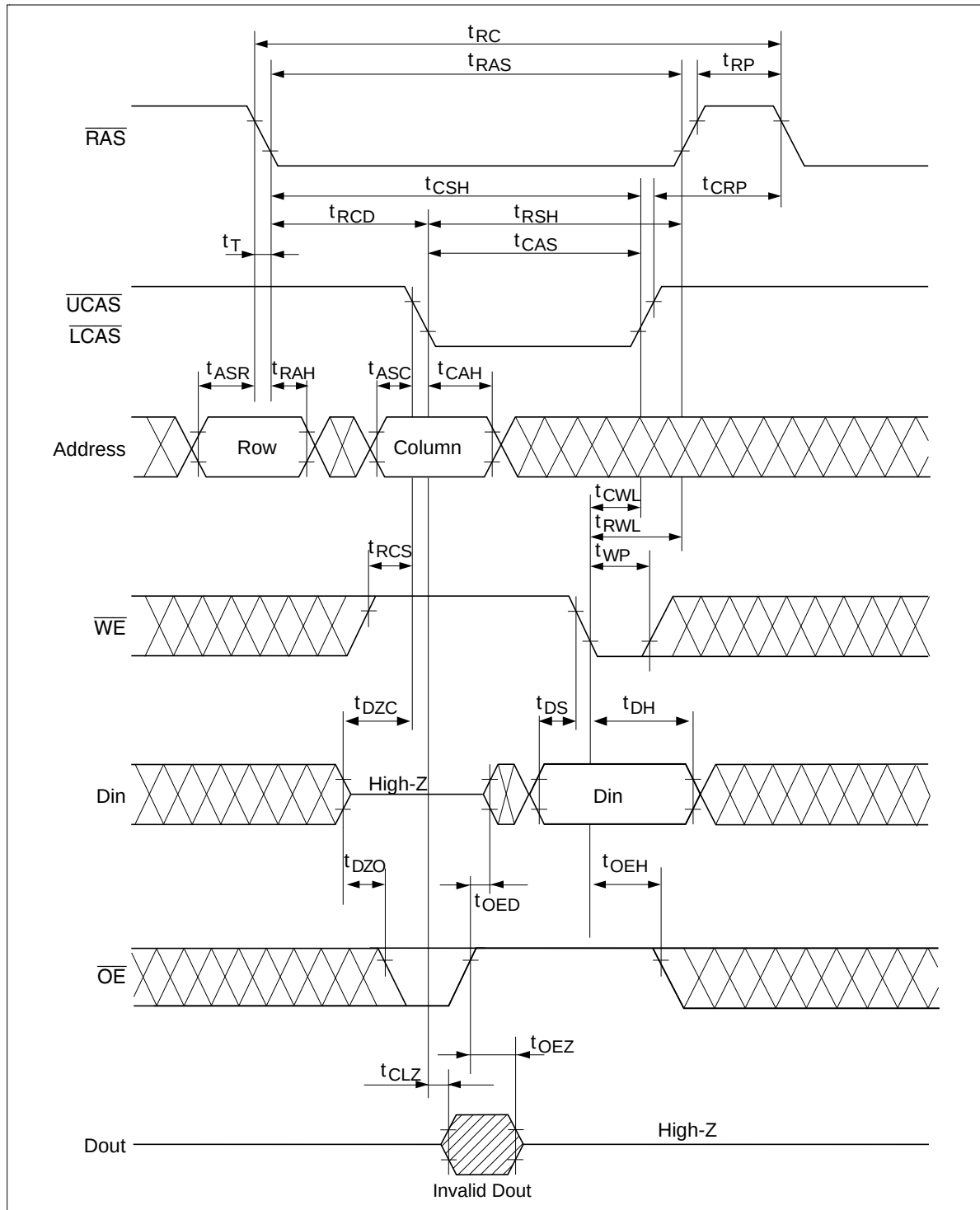
4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

Early Write Cycle

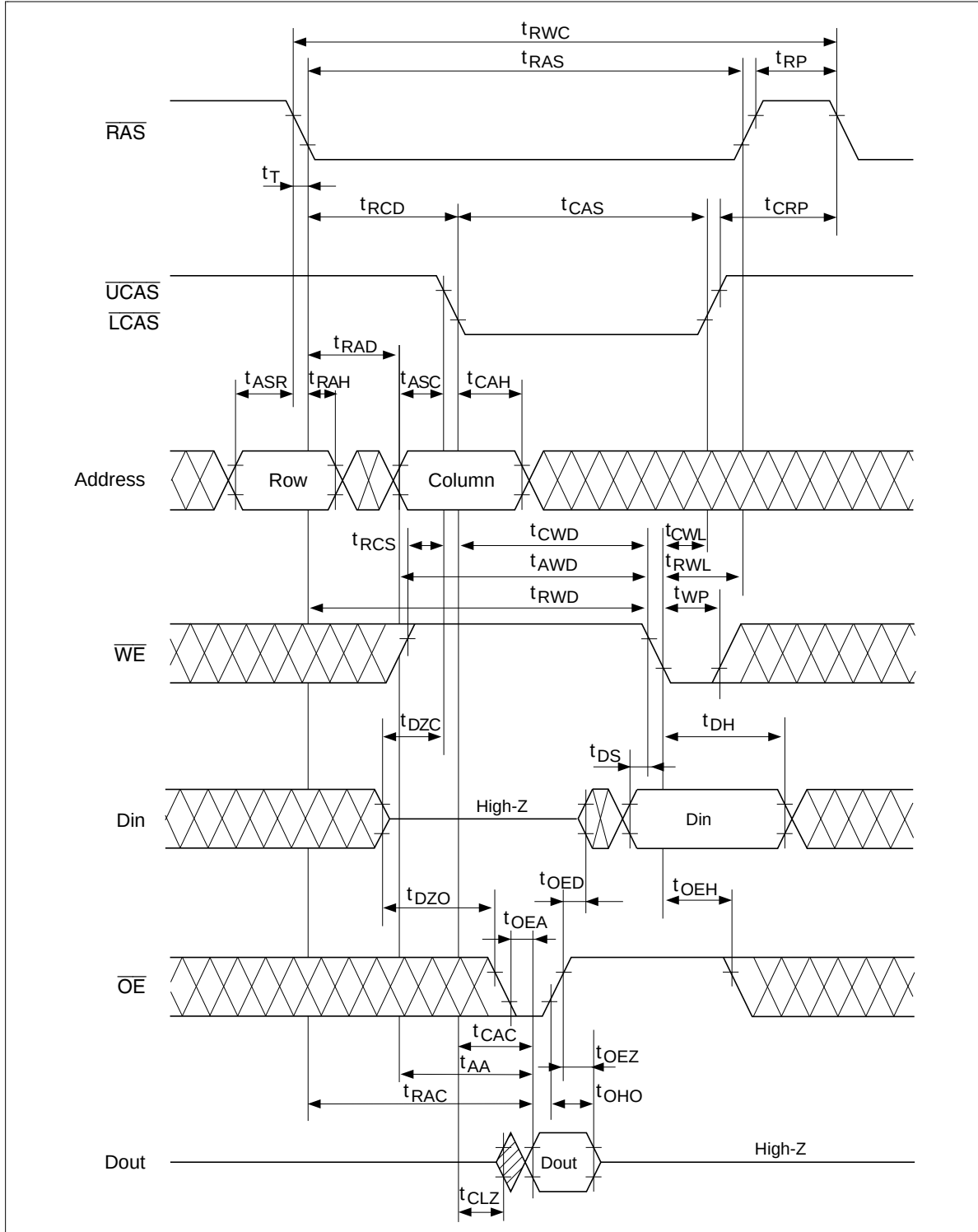


HM5116160 Series, HM5118160 Series

Delayed Write Cycle*¹⁸

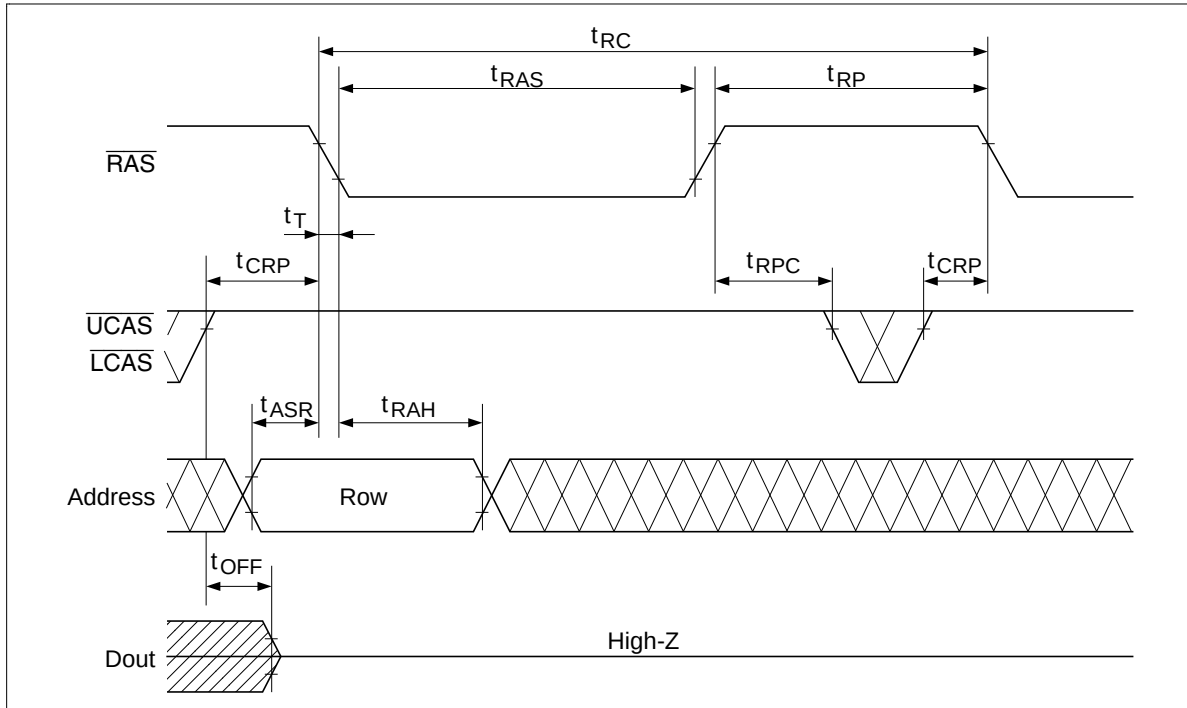


Read-Modify-Write Cycle*18



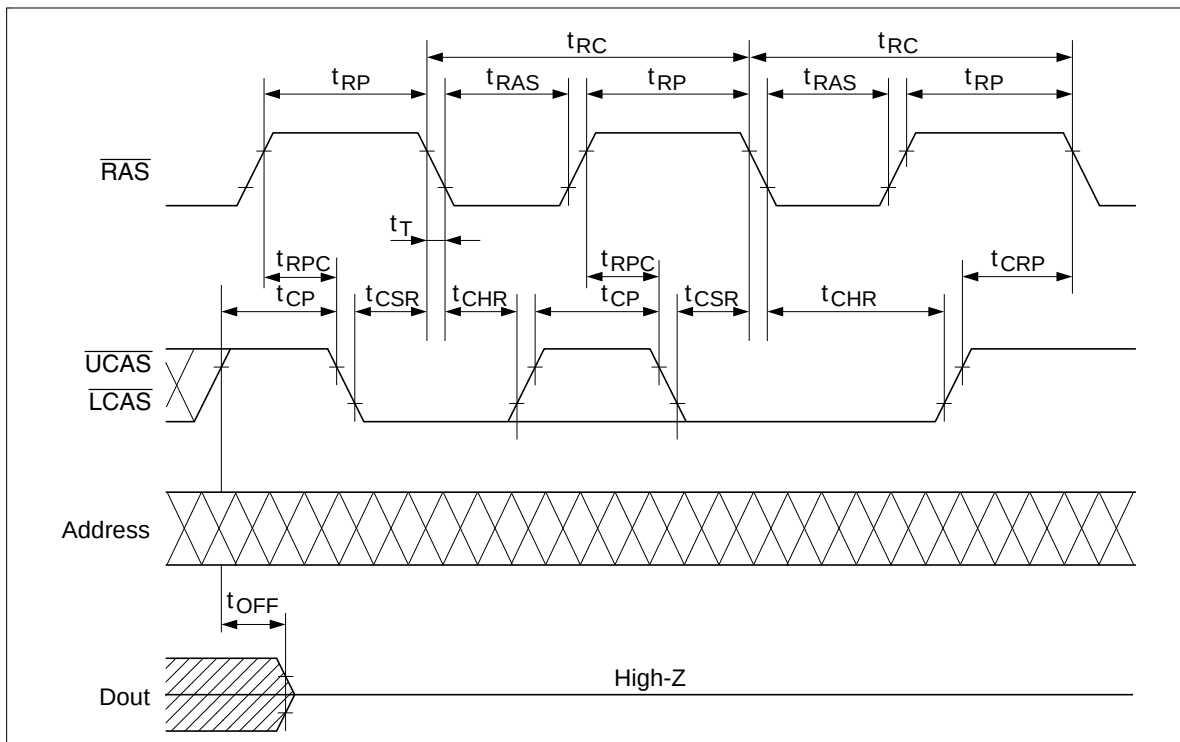
HM5116160 Series, HM5118160 Series

$\overline{\text{RAS}}$ -Only Refresh Cycle



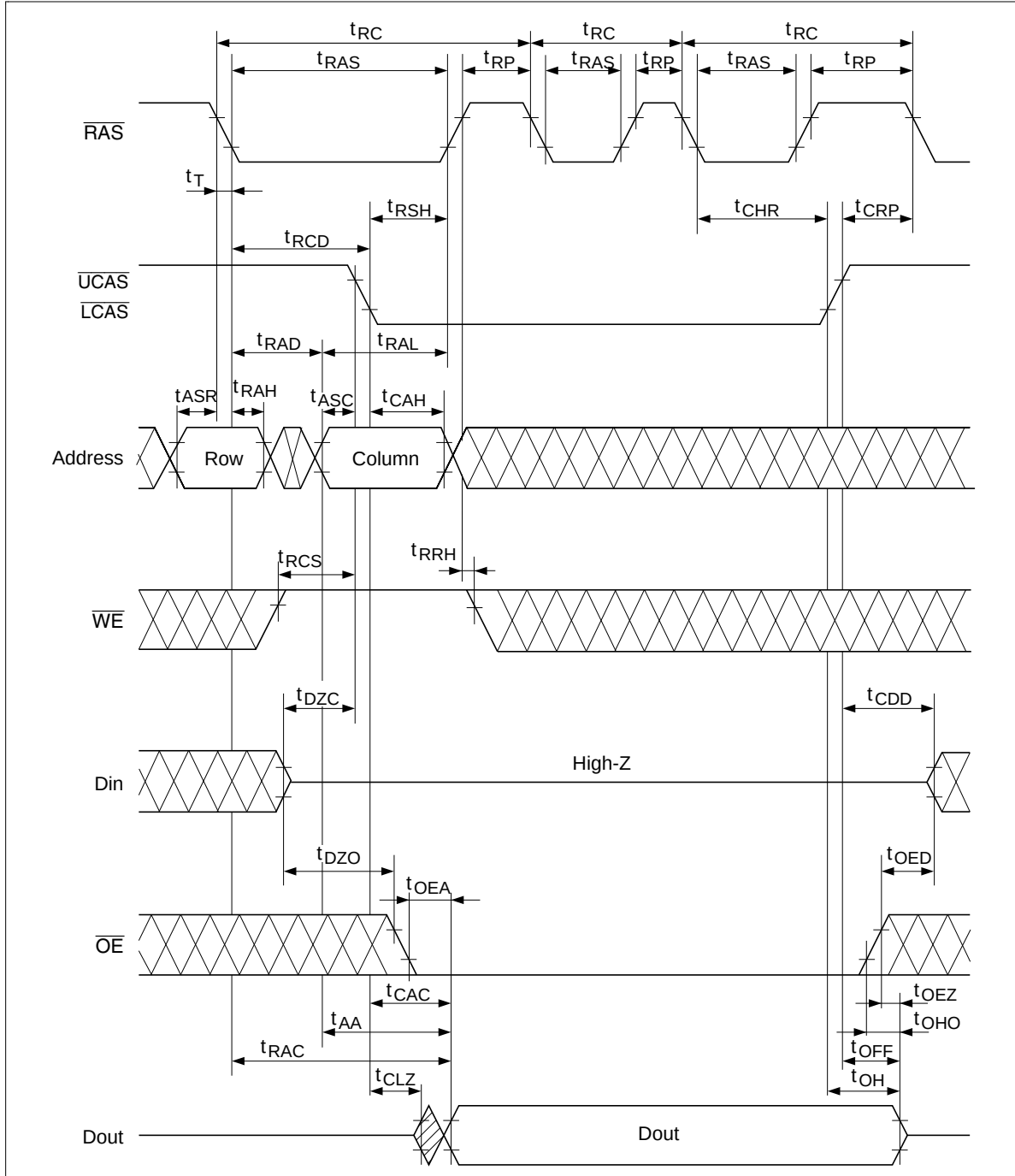
HM5116160 Series, HM5118160 Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

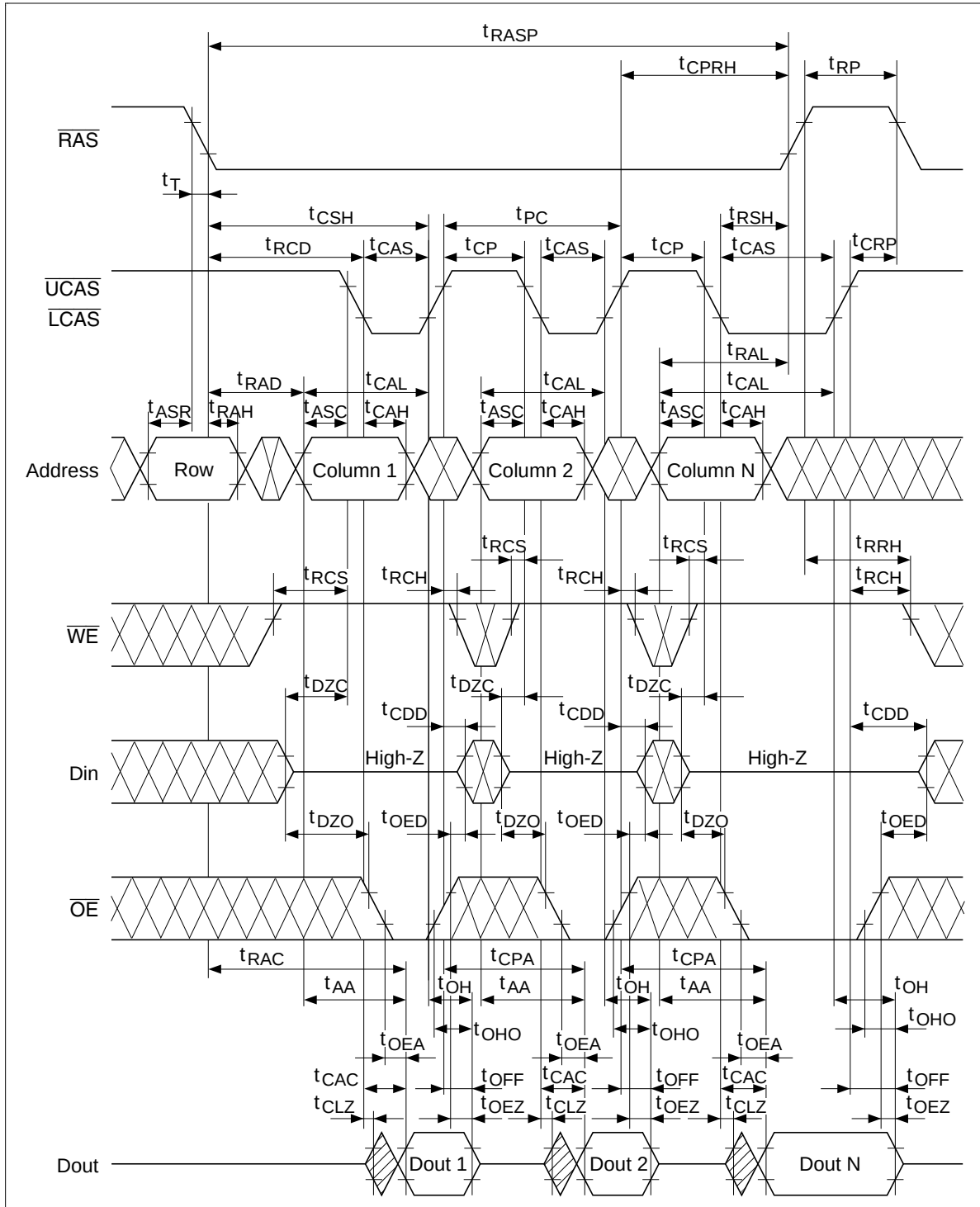


HM5116160 Series, HM5118160 Series

Hidden Refresh Cycle

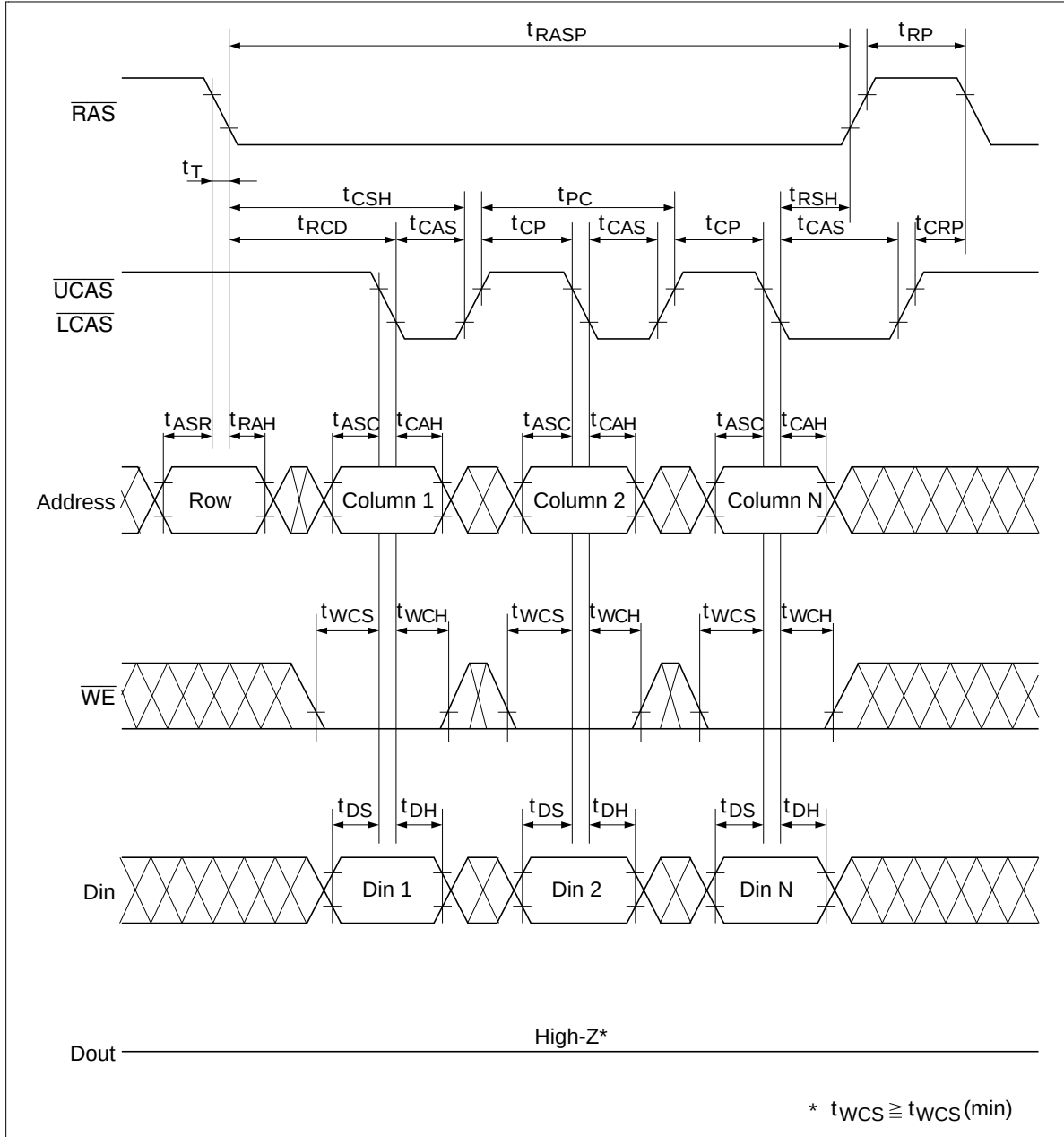


Fast Page Mode Read Cycle



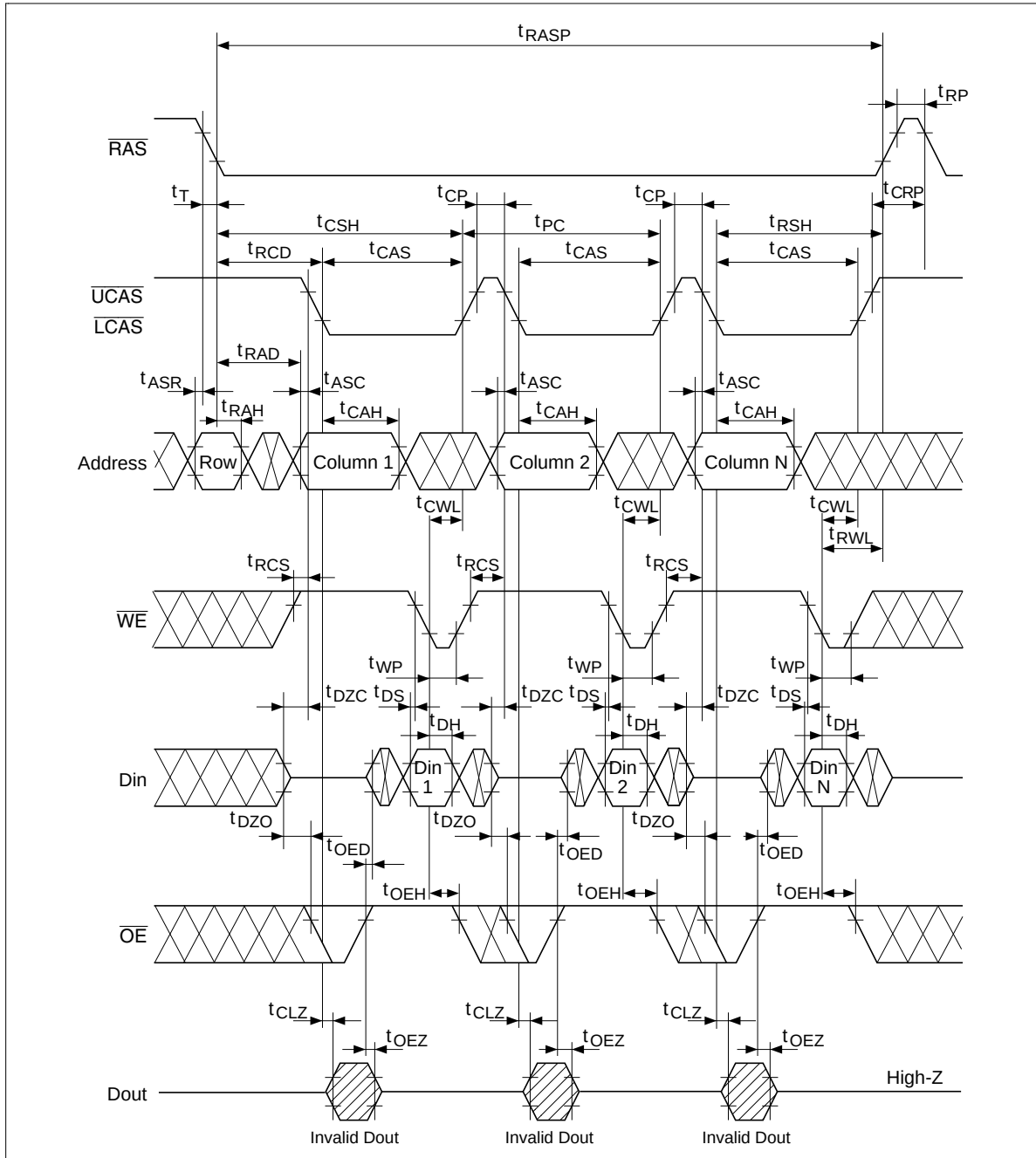
HM5116160 Series, HM5118160 Series

Fast Page Mode Early Write Cycle



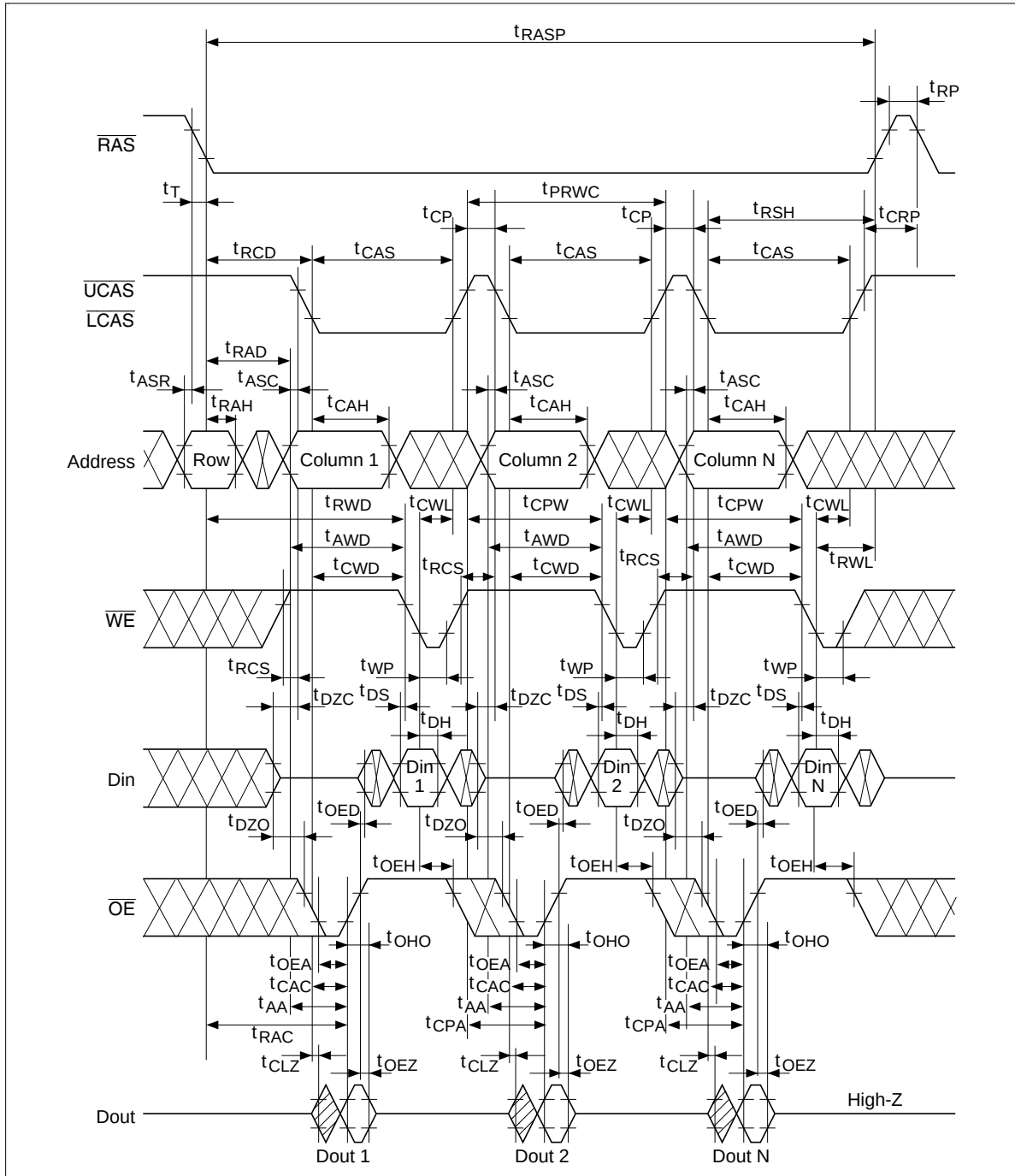
HM5116160 Series, HM5118160 Series

Fast Page Mode Delayed Write Cycle*¹⁸



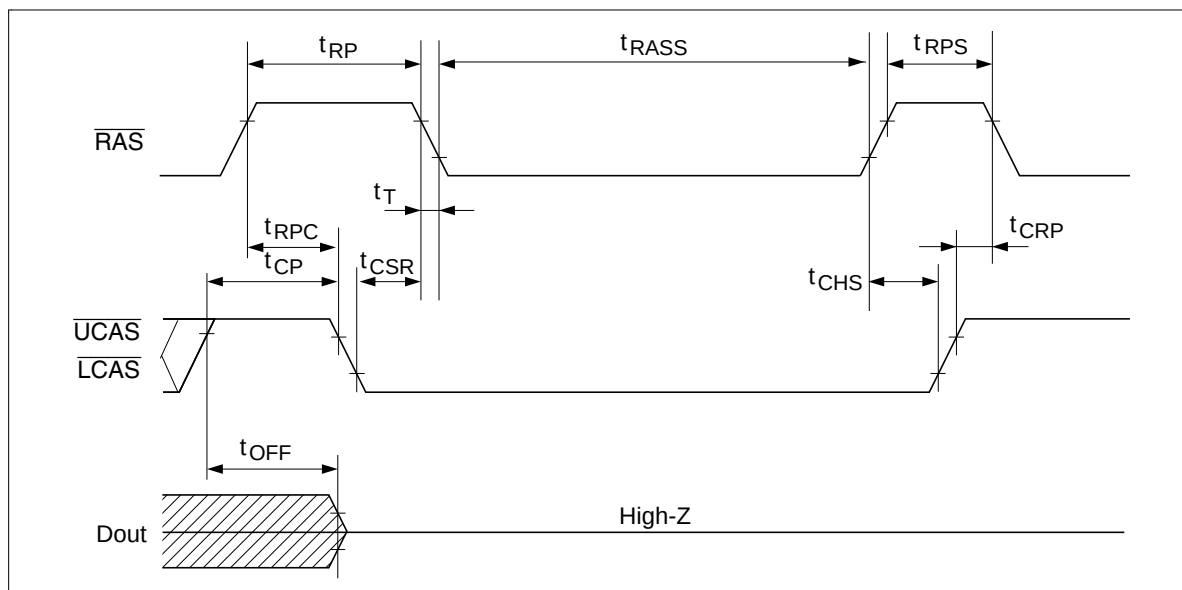
HM5116160 Series, HM5118160 Series

Fast Page Mode Read-Modify-Write Cycle*18



HM5116160 Series, HM5118160 Series

Self Refresh Cycle (L-version)*26, 27, 28, 29



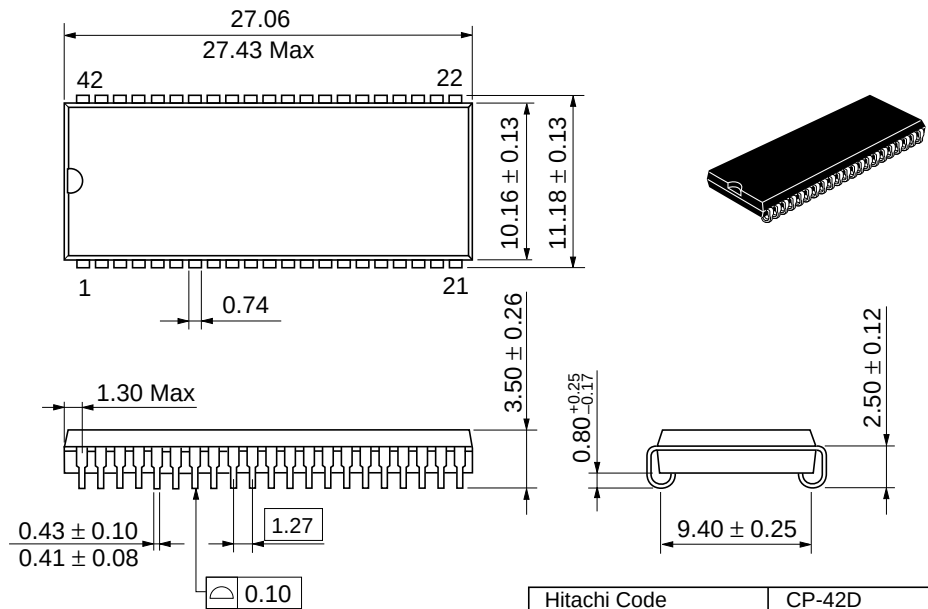
HM5116160 Series, HM5118160 Series

Package Dimensions

HM5116160J/LJ Series

HM5118160J/LJ Series (CP-42D)

Unit: mm



Dimension including the plating thickness
Base material dimension

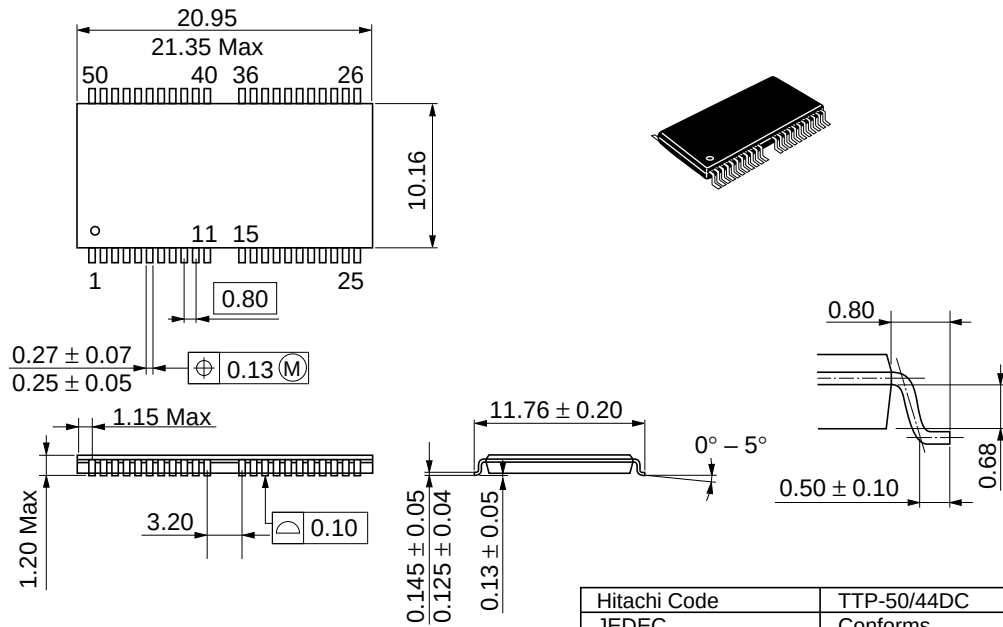
Hitachi Code	CP-42D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.75 g

HM5116160 Series, HM5118160 Series

HM5116160TT/LTT Series

HM5118160TT/LTT Series (TTP-50/44DC)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-50/44DC
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.50 g

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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A
Tel: 800-285-1601
Fax: 303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

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HM5116160 Series, HM5118160 Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Sep. 30, 1996	Initial issue	Y. Kasama	M. Mishima
2.0	Dec. 5, 1996	Addition of HM5116160/HM5118160-5 Series DC Characteristics (HM5116160 Series) I_{CC7} max: 105/95 mA to 105/95/85 mA DC Characteristics (HM5118160 Series) I_{CC7} max: 170/150 mA to 185/165/145 mA AC Characteristics t_{RRH} min: 0/0 ns to 5/5/5 ns t_{RPC} min: 0/0 ns to 5/5/5 ns	Y. Kasama	M. Mishima
3.0	Feb. 21, 1997	AC Characteristics t_{RRH} min: 5/5/5 ns to 0/0/0 ns	Y. Kasama	Y. Matsuno
4.0	Jun. 25, 1997	Deletion of HM5116160/HM5118160-5 Series Timing Waveforms Deletion of note: $t_{OE H} \geq t_{CWL}$	Y. Kasama	Y. Matsuno
5.0	Nov. 1997	Change of Subtitle		