

# HM514170, HM514170L Series

262,144-word × 16-bit Dynamic Random Access Memory

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM514170 are CMOS dynamic RAM organized as 262,144-word × 16-bit. HM514170 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514170 offer fast page mode as a high speed access mode.

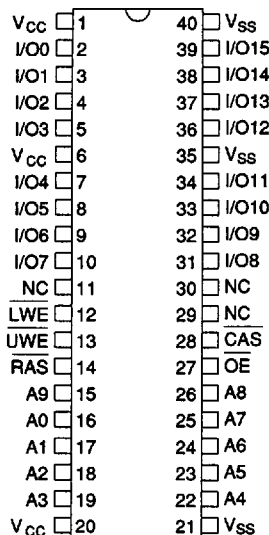
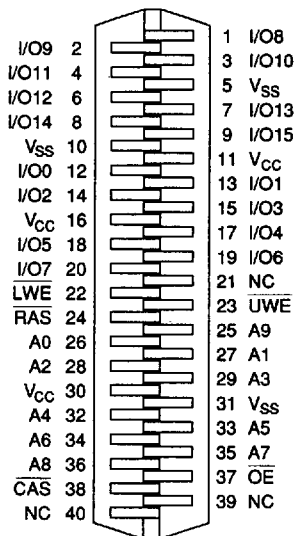
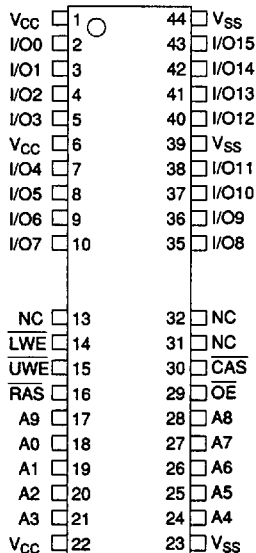
Multiplexed address input permits the HM514170 to be packaged in standard 400-mil 40-pin plastic SOJ, standard 475-mil 40-pin plastic ZIP, and 400-mil 40-pin plastic TSOP.

## Features

- Single 5 V (± 10%)
- High speed
  - Access time: 70 ns/80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 770 mW/660 mW/550 mW (max)
  - Standby mode: 11 mW (max)
  - 1.1 mW (max) (L-version)
- Fast page mode capability
- 1024 refresh cycles: 16 ms
- 128 ms (L-version)
- 2  $\overline{WE}$  byte control
- 3 variations of refresh
  - $\overline{RAS}$ -only refresh
  - CAS-before-RAS refresh
  - Hidden refresh
- Battery back up operation (L-version)

## Ordering Information

| Type No.       | Access time | Package                                |
|----------------|-------------|----------------------------------------|
| HM514170JP-7   | 70 ns       | 400-mil 40-pin plastic SOJ (CP-40D)    |
| HM514170JP-8   | 80 ns       |                                        |
| HM514170JP-10  | 100 ns      |                                        |
| HM514170ZP-7   | 70 ns       | 475-mil 40-pin plastic ZIP (ZP-40)     |
| HM514170ZP-8   | 80 ns       |                                        |
| HM514170ZP-10  | 100 ns      |                                        |
| HM514170TT-7   | 70 ns       | 400-mil 40-pin plastic TSOP (TTP-40DB) |
| HM514170TT-8   | 80 ns       |                                        |
| HM514170TT-10  | 100 ns      |                                        |
| HM514170LJP-7  | 70 ns       | 400 mil 40-pin plastic SOJ (CP-40D)    |
| HM514170LJP-8  | 80 ns       |                                        |
| HM514170LJP-10 | 100 ns      |                                        |
| HM514170LZP-7  | 70 ns       | 475-mil 40-pin plastic ZIP (ZP-40)     |
| HM514170LZP-8  | 80 ns       |                                        |
| HM514170LZP-10 | 100 ns      |                                        |
| HM514170LTT-7  | 70 ns       | 400-mil 40-pin plastic TSOP (TTP-40DB) |
| HM514170LTT-8  | 80 ns       |                                        |
| HM514170LTT-10 | 100 ns      |                                        |

**HM514170, HM514170L Series****Pin Arrangement****HITACHI/ LOGIC/ARRAYS/MEM****HM514170JP/LJP Series****(Top View)****HM514170ZP/LZP Series****(Bottom View)****HM514170TT/LTT Series****(Top View)****Pin Description**

| Pin name | Function |
|----------|----------|
|----------|----------|

|         |                                                                                                 |
|---------|-------------------------------------------------------------------------------------------------|
| A0 – A9 | Address input<br>– Row address A0 – A9<br>– Column address A0 – A7<br>– Refresh address A0 – A9 |
|---------|-------------------------------------------------------------------------------------------------|

|              |                  |
|--------------|------------------|
| I/O0 – I/O15 | Data-in/data-out |
|--------------|------------------|

|     |                    |
|-----|--------------------|
| RAS | Row address strobe |
|-----|--------------------|

|     |                       |
|-----|-----------------------|
| CAS | Column address strobe |
|-----|-----------------------|

|          |                   |
|----------|-------------------|
| UWE, LWE | Read/write enable |
|----------|-------------------|

|    |               |
|----|---------------|
| OE | Output enable |
|----|---------------|

|     |              |
|-----|--------------|
| Vcc | Power (+5 V) |
|-----|--------------|

|     |        |
|-----|--------|
| Vss | Ground |
|-----|--------|

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## Truth Table

## HITACHI/ LOGIC/ARRAYS/MEM

| Inputs |     |     |     |    | I/O         |              | Operation        |
|--------|-----|-----|-----|----|-------------|--------------|------------------|
| RAS    | LWE | UWE | CAS | OE | I/O0 - I/O7 | I/O8 - I/O15 |                  |
| H      | H   | H   | H   | H  | High-Z      | High-Z       | Standby          |
| L      | H   | H   | H   | H  | High-Z      | High-Z       | Refresh          |
| L      | H   | H   | L   | L  | Dout        | Dout         | Word read        |
| L      | L   | H   | L   | H  | Din         | Don't care   | Lower byte write |
| L      | H   | L   | L   | H  | Don't care  | Din          | Upper byte write |
| L      | L   | L   | L   | H  | Din         | Din          | Word write       |
| L      | H   | H   | L   | H  | High-Z      | High-Z       |                  |

## Absolute Maximum Ratings

| Parameter                               | Symbol    | Value        | Unit |
|-----------------------------------------|-----------|--------------|------|
| Voltage on any pin relative to $V_{SS}$ | $V_T$     | -1.0 to +7.0 | V    |
| Supply voltage relative to $V_{SS}$     | $V_{CC}$  | -1.0 to +7.0 | V    |
| Short circuit output current            | $I_{out}$ | 50           | mA   |
| Power dissipation                       | $P_T$     | 1.0          | W    |
| Operating temperature                   | $T_{opr}$ | 0 to +70     | °C   |
| Storage temperature                     | $T_{stg}$ | -55 to +125  | °C   |

## Recommended DC Operating Conditions ( $T_a = 0$ to +70°C) \*2

| Parameter          | Symbol             | Min  | Typ | Max | Unit | Note |
|--------------------|--------------------|------|-----|-----|------|------|
| Supply voltage     | $V_{SS}$           | 0    | 0   | 0   | V    |      |
|                    | $V_{CC}$           | 4.5  | 5.0 | 5.5 | V    | 1    |
| Input high voltage | $V_{IH}$           | 2.4  | —   | 6.5 | V    | 1    |
| Input low voltage  | (I/O pin) $V_{IL}$ | -1.0 | —   | 0.8 | V    | 1    |
|                    | (Others) $V_{IL}$  | -2.0 | —   | 0.8 | V    | 1    |

- Notes: 1. All voltage referenced to  $V_{SS}$   
2. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
The supply voltage with all  $V_{SS}$  pins must be on the same level.

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DC Characteristics ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                                      | Symbol     | HM514170-7 |          | HM514170-8 |          | HM514170-10 |          | Unit          | Test conditions                                                                                                                                                     | Notes |
|----------------------------------------------------------------|------------|------------|----------|------------|----------|-------------|----------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
|                                                                |            | Min        | Max      | Min        | Max      | Min         | Max      |               |                                                                                                                                                                     |       |
| Operating current                                              | $I_{CC1}$  | —          | 140      | —          | 120      | —           | 100      | mA            | RAS cycling, CAS cycling<br>$t_{RC} = \text{min}$                                                                                                                   | 1, 2  |
| Standby current                                                | $I_{CC2}$  | —          | 2        | —          | 2        | —           | 2        | mA            | TTL interface<br>RAS, CAS = $V_{IH}$<br>Dout = High-Z                                                                                                               |       |
|                                                                |            | —          | 1        | —          | 1        | —           | 1        | mA            | CMOS interface<br>RAS, CAS $\geq V_{CC} - 0.2\text{ V}$<br>Dout = High-Z                                                                                            |       |
| Standby current (L-version)                                    |            | —          | 200      | —          | 200      | —           | 200      | $\mu\text{A}$ | CMOS interface<br>RAS, CAS $\geq V_{CC} - 0.2\text{ V}$<br>Dout = High-Z                                                                                            |       |
| RAS-only refresh current                                       | $I_{CC3}$  | —          | 120      | —          | 100      | —           | 80       | mA            | $t_{RC} = \text{min}$                                                                                                                                               | 2     |
| Standby current                                                | $I_{CC5}$  | —          | 5        | —          | 5        | —           | 5        | mA            | RAS = $V_{IH}$ , CAS = $V_{IL}$<br>Dout = enable                                                                                                                    | 1     |
| CAS-before-RAS refresh current                                 | $I_{CC6}$  | —          | 120      | —          | 100      | —           | 80       | mA            | $t_{RC} = \text{min}$                                                                                                                                               |       |
| Fast page mode current                                         | $I_{CC7}$  | —          | 130      | —          | 120      | —           | 110      | mA            | $t_{PC} = \text{min}$                                                                                                                                               | 1, 3  |
| Battery back up current (Standby with CBR refresh) (L-version) | $I_{CC10}$ | —          | 300      | —          | 300      | —           | 300      | $\mu\text{A}$ | Standby: CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC} = 125\text{ }\mu\text{s}$<br>$t_{RAS} \leq 1\text{ }\mu\text{s}$ , CAS = $V_{IL}$<br>WE = $V_{IH}$ | 4     |
| Input leakage current                                          | $I_{LI}$   | -10        | 10       | -10        | 10       | -10         | 10       | $\mu\text{A}$ | $0\text{ V} \leq V_{in} \leq 7\text{ V}$                                                                                                                            |       |
| Output leakage current                                         | $I_{LO}$   | -10        | 10       | -10        | 10       | -10         | 10       | $\mu\text{A}$ | $0\text{ V} \leq V_{out} \leq 7\text{ V}$<br>Dout = disable                                                                                                         |       |
| Output high voltage                                            | $V_{OH}$   | 2.4        | $V_{CC}$ | 2.4        | $V_{CC}$ | 2.4         | $V_{CC}$ | V             | High Iout = -5 mA                                                                                                                                                   |       |
| Output low voltage                                             | $V_{OL}$   | 0          | 0.4      | 0          | 0.4      | 0           | 0.4      | V             | Low Iout = 4.2 mA                                                                                                                                                   |       |

- Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected,  $I_{CC}$  max is specified at the output open condition.  
2. Address can be changed once or less while RAS =  $V_{IL}$ .  
3. Address can be changed once or less while CAS =  $V_{IH}$ .  
4.  $V_{IH} \geq V_{CC} - 0.2\text{ V}$ ,  $V_{IL} \leq 0.2\text{ V}$

# HM514170, HM514170L Series

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Capacitance ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ )

| Parameter                              | Symbol    | Typ | Max | Unit | Notes |
|----------------------------------------|-----------|-----|-----|------|-------|
| Input capacitance (Address)            | $C_{I1}$  | —   | 5   | pF   | 1     |
| Input capacitance (Clocks)             | $C_{I2}$  | —   | 7   | pF   | 1     |
| Output capacitance (Data-in, Data-out) | $C_{I/O}$ | —   | 10  | pF   | 1, 2  |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $CAS = V_{IH}$  to disable Dout

AC Characteristics ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ) \*1, \*14, \*15

## Test Conditions

- Input rise and fall times: 5 ns
- Output load: 2 TTL gate +  $C_L$  (100 pF)
- Input timing reference levels: 0.8 V, 2.4 V
- (Including scope and jig)

## Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

HM514170-7 HM514170-8 HM514170-10

| Parameter                        | Symbol    | Min | Max   | Min | Max   | Min | Max   | Unit | Notes |
|----------------------------------|-----------|-----|-------|-----|-------|-----|-------|------|-------|
| Random read or write cycle time  | $t_{RC}$  | 130 | —     | 150 | —     | 180 | —     | ns   |       |
| RAS precharge time               | $t_{RP}$  | 50  | —     | 60  | —     | 70  | —     | ns   |       |
| RAS pulse width                  | $t_{RAS}$ | 70  | 10000 | 80  | 10000 | 100 | 10000 | ns   |       |
| CAS pulse width                  | $t_{CAS}$ | 20  | 10000 | 20  | 10000 | 25  | 10000 | ns   |       |
| Row address setup time           | $t_{ASR}$ | 0   | —     | 0   | —     | 0   | —     | ns   |       |
| Row address hold time            | $t_{RAH}$ | 10  | —     | 10  | —     | 15  | —     | ns   |       |
| Column address setup time        | $t_{ASC}$ | 0   | —     | 0   | —     | 0   | —     | ns   |       |
| Column address hold time         | $t_{CAH}$ | 15  | —     | 15  | —     | 20  | —     | ns   |       |
| RAS to CAS delay time            | $t_{RCD}$ | 20  | 50    | 20  | 60    | 25  | 75    | ns   | 8     |
| RAS to column address delay time | $t_{RAD}$ | 15  | 35    | 15  | 40    | 20  | 55    | ns   | 9     |
| RAS hold time                    | $t_{RSH}$ | 20  | —     | 20  | —     | 25  | —     | ns   |       |
| CAS hold time                    | $t_{CSH}$ | 70  | —     | 80  | —     | 100 | —     | ns   |       |
| CAS to RAS precharge time        | $t_{CRP}$ | 15  | —     | 15  | —     | 15  | —     | ns   |       |
| OE to Din delay time             | $t_{ODD}$ | 20  | —     | 20  | —     | 25  | —     | ns   |       |

# HM514170, HM514170L Series

## Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (cont)

| Parameter                       | Symbol           | HM514170-7 |     | HM514170-8 |     | HM514170-10 |     | Unit | Notes |
|---------------------------------|------------------|------------|-----|------------|-----|-------------|-----|------|-------|
|                                 |                  | Min        | Max | Min        | Max | Min         | Max |      |       |
| OE delay time from Din          | t <sub>DZO</sub> | 0          | —   | 0          | —   | 0           | —   | ns   |       |
| CAS setup time from Din         | t <sub>DZC</sub> | 0          | —   | 0          | —   | 0           | —   | ns   |       |
| Transition time (rise and fall) | t <sub>T</sub>   | 3          | 50  | 3          | 50  | 3           | 50  | ns   | 7     |
| Refresh period                  | t <sub>REF</sub> | —          | 16  | —          | 16  | —           | 16  | ms   |       |
| Refresh period (L-version)      | t <sub>REF</sub> | —          | 128 | —          | 128 | —           | 128 | ms   |       |

## Read Cycle

## HITACHI/ LOGIC/ARRAYS/MEM

| Parameter                       | Symbol            | HM514170-7 |     | HM514170-8 |     | HM514170-10 |     | Unit | Notes    |
|---------------------------------|-------------------|------------|-----|------------|-----|-------------|-----|------|----------|
|                                 |                   | Min        | Max | Min        | Max | Min         | Max |      |          |
| Access time from RAS            | t <sub>RAC</sub>  | —          | 70  | —          | 80  | —           | 100 | ns   | 2, 3     |
| Access time from CAS            | t <sub>CAC</sub>  | —          | 20  | —          | 20  | —           | 25  | ns   | 3, 4, 13 |
| Access time from address        | t <sub>AA</sub>   | —          | 35  | —          | 40  | —           | 45  | ns   | 3, 5, 13 |
| Access time from OE             | t <sub>OAC</sub>  | —          | 20  | —          | 20  | —           | 25  | ns   |          |
| Read command setup time         | t <sub>RCS</sub>  | 0          | —   | 0          | —   | 0           | —   | ns   |          |
| Read command hold time to CAS   | t <sub>RCH</sub>  | 0          | —   | 0          | —   | 0           | —   | ns   |          |
| Read command hold time to RAS   | t <sub>RRH</sub>  | 0          | —   | 0          | —   | 0           | —   | ns   |          |
| Column address to RAS lead time | t <sub>RAL</sub>  | 35         | —   | 40         | —   | 45          | —   | ns   |          |
| Output buffer turn-off time     | t <sub>OFF1</sub> | 0          | 15  | 0          | 15  | 0           | 20  | ns   | 6        |
| Output buffer turn-off to OE    | t <sub>OFF2</sub> | 0          | 15  | 0          | 15  | 0           | 20  | ns   | 6        |
| CAS to Din delay time           | t <sub>CDD</sub>  | 15         | —   | 15         | —   | 20          | —   | ns   |          |

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## Write Cycle

| Parameter                                      | Symbol    | HM514170-7 |     | HM514170-8 |     | HM514170-10 |     | Unit | Notes |
|------------------------------------------------|-----------|------------|-----|------------|-----|-------------|-----|------|-------|
|                                                |           | Min        | Max | Min        | Max | Min         | Max |      |       |
| Write command setup time                       | $t_{WCS}$ | 0          | —   | 0          | —   | 0           | —   | ns   | 10    |
| Write command hold time                        | $t_{WCH}$ | 15         | —   | 15         | —   | 20          | —   | ns   |       |
| Write command pulse width                      | $t_{WP}$  | 10         | —   | 10         | —   | 20          | —   | ns   |       |
| Write command to $\overline{RAS}$ lead time    | $t_{RWL}$ | 20         | —   | 20         | —   | 25          | —   | ns   |       |
| Write command to $\overline{CAS}$ lead time    | $t_{CWL}$ | 20         | —   | 20         | —   | 25          | —   | ns   |       |
| Data-in setup time                             | $t_{DS}$  | 0          | —   | 0          | —   | 0           | —   | ns   | 11    |
| Data-in hold time                              | $t_{DH}$  | 15         | —   | 15         | —   | 20          | —   | ns   | 11    |
| $\overline{CAS}$ to $\overline{OE}$ delay time | $t_{COD}$ | —          | 0   | —          | 0   | —           | 0   | ns   | 18    |

## Read-Modify-Write Cycle

| Parameter                                      | Symbol    | HM514170-7 |     | HM514170-8 |     | HM514170-10 |     | Unit | Notes  |
|------------------------------------------------|-----------|------------|-----|------------|-----|-------------|-----|------|--------|
|                                                |           | Min        | Max | Min        | Max | Min         | Max |      |        |
| Read-modify-write cycle time                   | $t_{RWC}$ | 180        | —   | 200        | —   | 245         | —   | ns   |        |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 95         | —   | 105        | —   | 135         | —   | ns   | 10     |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 45         | —   | 45         | —   | 60          | —   | ns   | 10     |
| Column address to $\overline{WE}$ delay time   | $t_{AWD}$ | 60         | —   | 65         | —   | 80          | —   | ns   | 10, 13 |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEh}$ | 20         | —   | 20         | —   | 25          | —   | ns   |        |

## Refresh Cycle

| Parameter                                                                                  | Symbol    | HM514170-7 |     | HM514170-8 |     | HM514170-10 |     | Unit | Note |
|--------------------------------------------------------------------------------------------|-----------|------------|-----|------------|-----|-------------|-----|------|------|
|                                                                                            |           | Min        | Max | Min        | Max | Min         | Max |      |      |
| $\overline{CAS}$ setup time<br>( $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle) | $t_{CSR}$ | 10         | —   | 10         | —   | 10          | —   | ns   |      |
| $\overline{CAS}$ hold time<br>( $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycle)  | $t_{CHR}$ | 10         | —   | 10         | —   | 10          | —   | ns   |      |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time                                   | $t_{RPC}$ | 10         | —   | 10         | —   | 10          | —   | ns   |      |
| $\overline{CAS}$ precharge time in normal mode                                             | $t_{CPN}$ | 10         | —   | 10         | —   | 10          | —   | ns   |      |



**HM514170, HM514170L Series**
**Fast Page Mode Cycle**
**HITACHI/ LOGIC/ARRAYS/MEM**
**HM514170-7 HM514170-8 HM514170-10**

| Parameter                                                                                                     | Symbol            | Min | Max    | Min | Max    | Min | Max    | Unit | Notes |
|---------------------------------------------------------------------------------------------------------------|-------------------|-----|--------|-----|--------|-----|--------|------|-------|
| Fast page mode cycle time                                                                                     | t <sub>PC</sub>   | 50  | —      | 55  | —      | 60  | —      | ns   |       |
| Fast page mode $\overline{\text{CAS}}$ precharge time                                                         | t <sub>CP</sub>   | 15  | —      | 15  | —      | 15  | —      | ns   |       |
| Fast page mode $\overline{\text{RAS}}$ pulse width                                                            | t <sub>RASC</sub> | —   | 100000 | —   | 100000 | —   | 100000 | ns   | 12    |
| Access time from $\overline{\text{CAS}}$ precharge                                                            | t <sub>ACP</sub>  | —   | 40     | —   | 45     | —   | 50     | ns   | 3, 13 |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge                                      | t <sub>RHCP</sub> | 40  | —      | 45  | —      | 50  | —      | ns   |       |
| Fast page mode read-modify-write cycle $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time | t <sub>CPW</sub>  | 65  | —      | 70  | —      | 85  | —      | ns   |       |
| Fast page mode read-modify-write cycle time                                                                   | t <sub>PCM</sub>  | 95  | —      | 100 | —      | 110 | —      | ns   |       |

**Counter Test Cycle**
**HM514170-7 HM514170-8 HM514170-10**

| Parameter                                                    | Symbol           | Min | Max | Min | Max | Min | Max | Unit | Note |
|--------------------------------------------------------------|------------------|-----|-----|-----|-----|-----|-----|------|------|
| $\overline{\text{CAS}}$ precharge time in counter test cycle | t <sub>CPT</sub> | 50  | —   | 50  | —   | 50  | —   | ns   |      |

# HM514170, HM514170L Series

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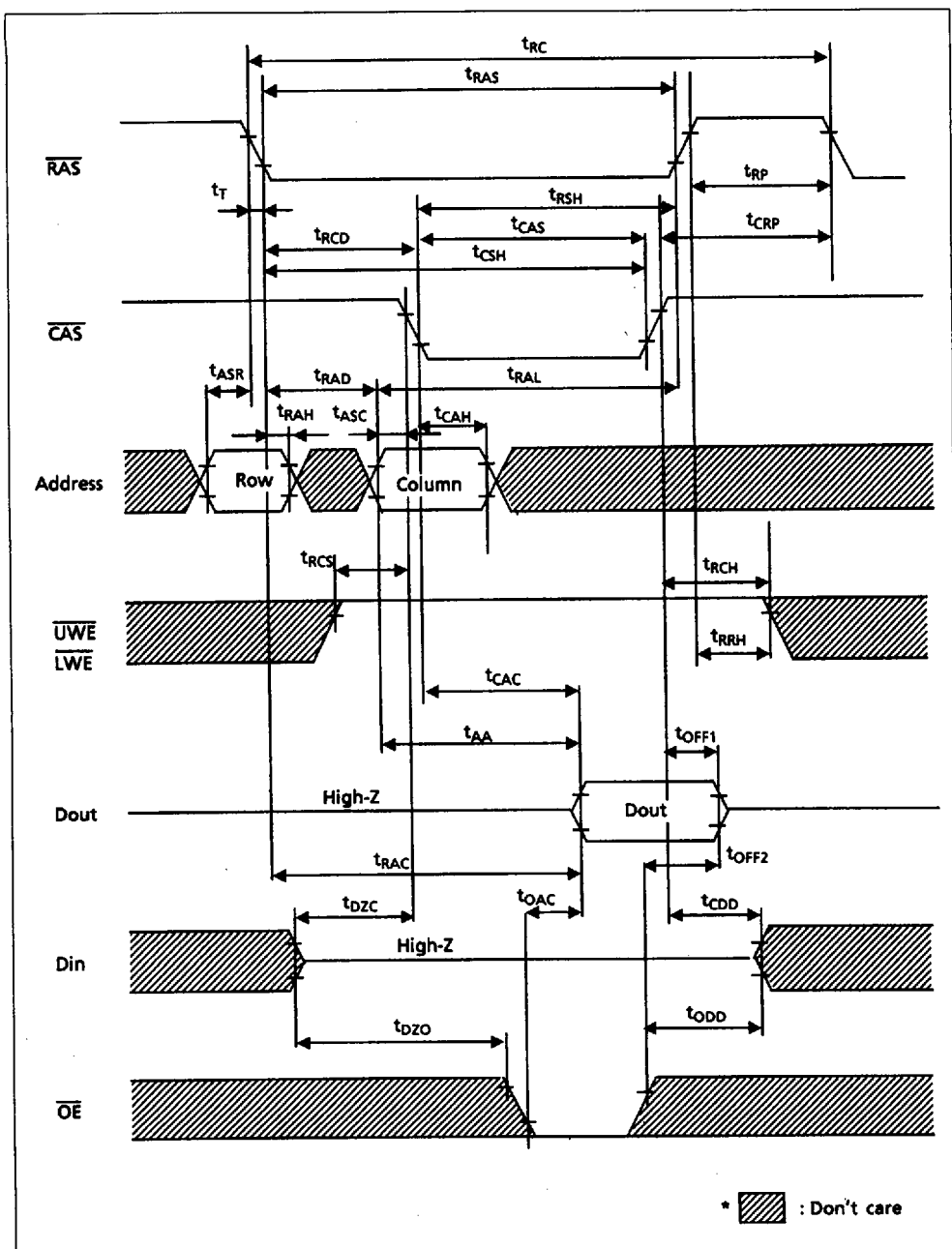
- Notes:
1. AC measurements assume  $t_T = 5 \text{ ns}$ .
  2. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  4. Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ .
  5. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \geq t_{RAD}(\text{max})$ .
  6.  $t_{OFF}(\text{max})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  7.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. Operation with the  $t_{RCD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RCD}(\text{max})$  is specified as a reference point only, if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
  9. Operation with the  $t_{RAD}(\text{max})$  limit insures that  $t_{RAC}(\text{max})$  can be met,  $t_{RAD}(\text{max})$  is specified as a reference point only, if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
  10.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}(\text{min})$ ,  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{AWD} \geq t_{AWD}(\text{min})$  and  $t_{CPW} \geq t_{CPW}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle and to  $\overline{\text{WE}}$  leading edge in a delayed write or a read-modify-write cycle.
  12.  $t_{RASC}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
  13. Access time is determined by the longer of  $t_{AA}$  or  $t_{CAC}$  or  $t_{ACP}$ .
  14. An initial pause of 100  $\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh cycle or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles is required.
  15. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device.
  16. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  17. When both  $\text{LWE}$  and  $\text{UWE}$  go low at the same time, all 16-bits data are written into the device.  $\text{LWE}$  and  $\text{UWE}$  cannot be straggled within the same write cycles.
  18. Do not enable  $\text{Dout}$  buffer when using delayed write timing.

## HM514170, HM514170L Series

## Timing Waveforms

HITACHI/ LOGIC/ARRAYS/MEM

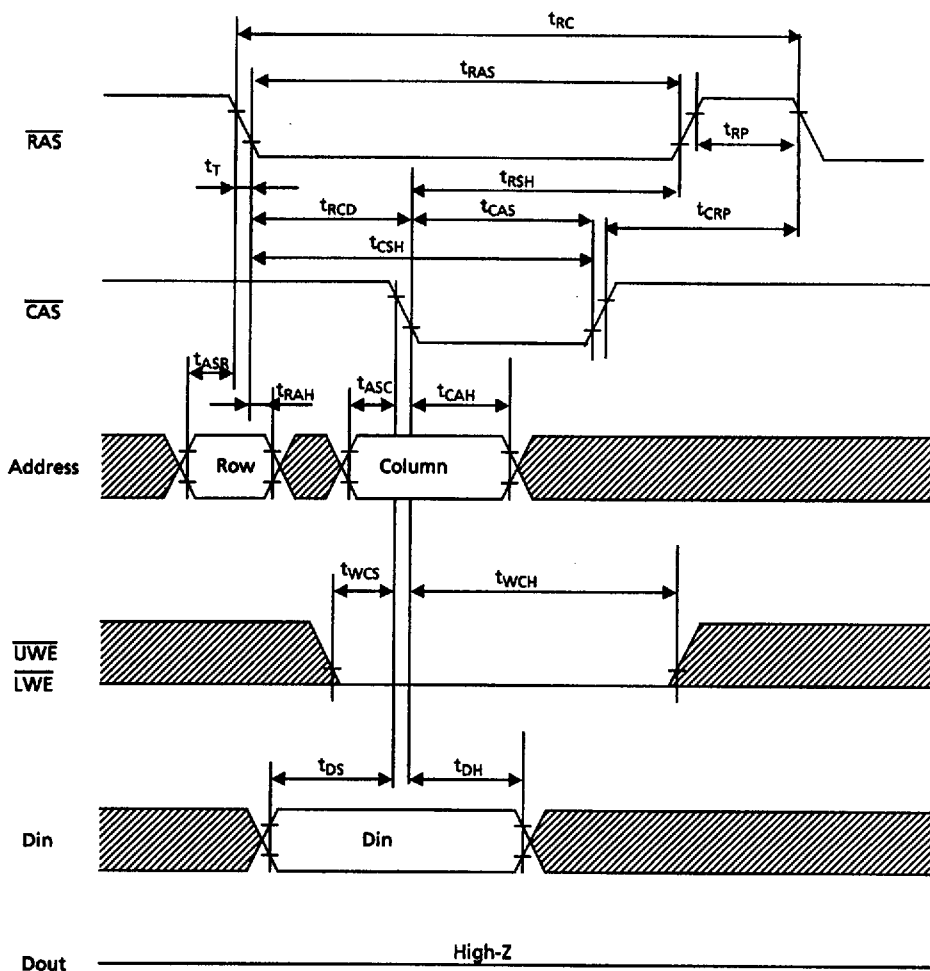
## Read Cycle



# HM514170, HM514170L Series

HITACHI/ LOGIC/ARRAYS/MEM

## Early Write Cycle



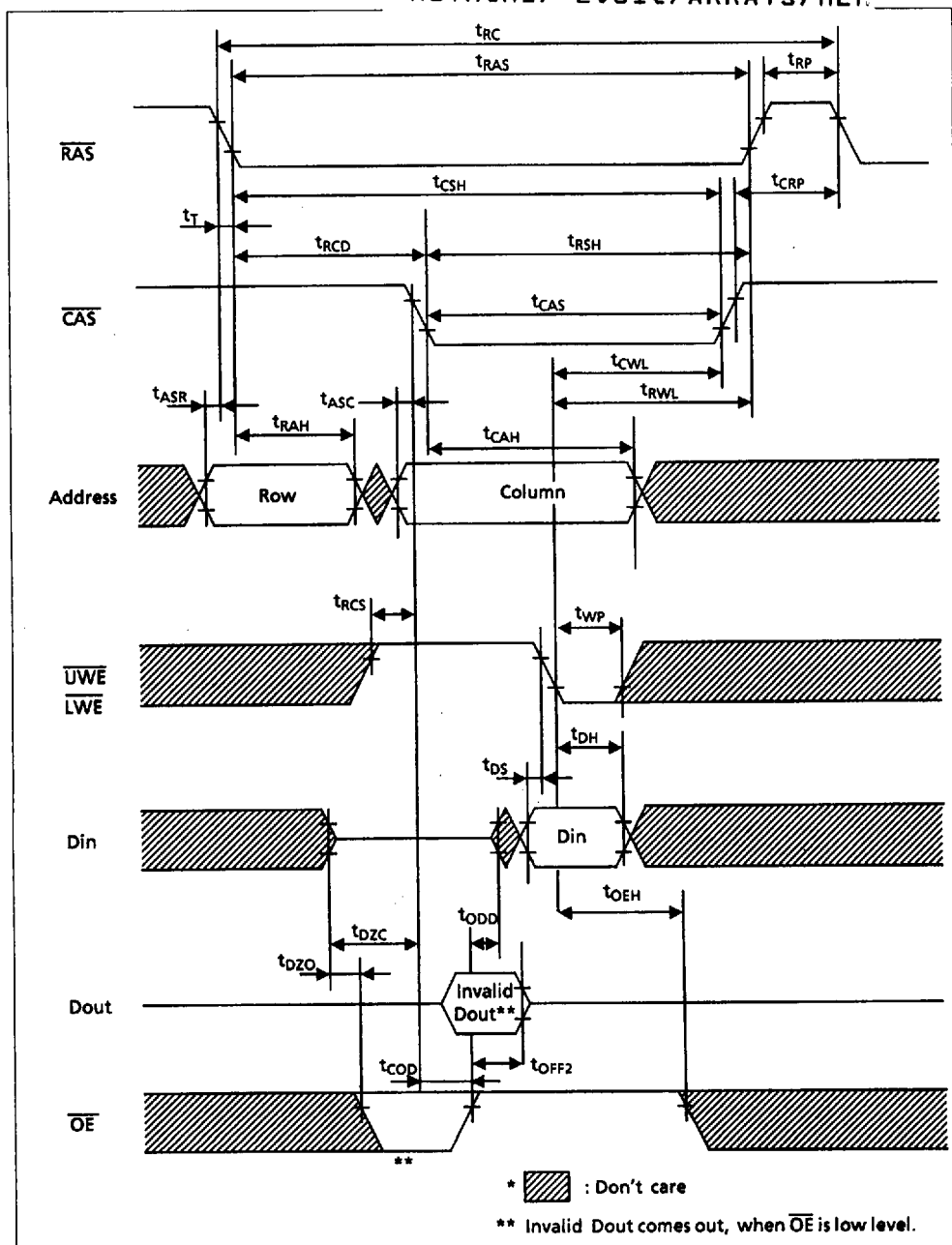
\* : Don't care

\*\*  $\overline{\text{OE}}$  : Don't care

# HM514170, HM514170L Series

## Delayed Write Cycle

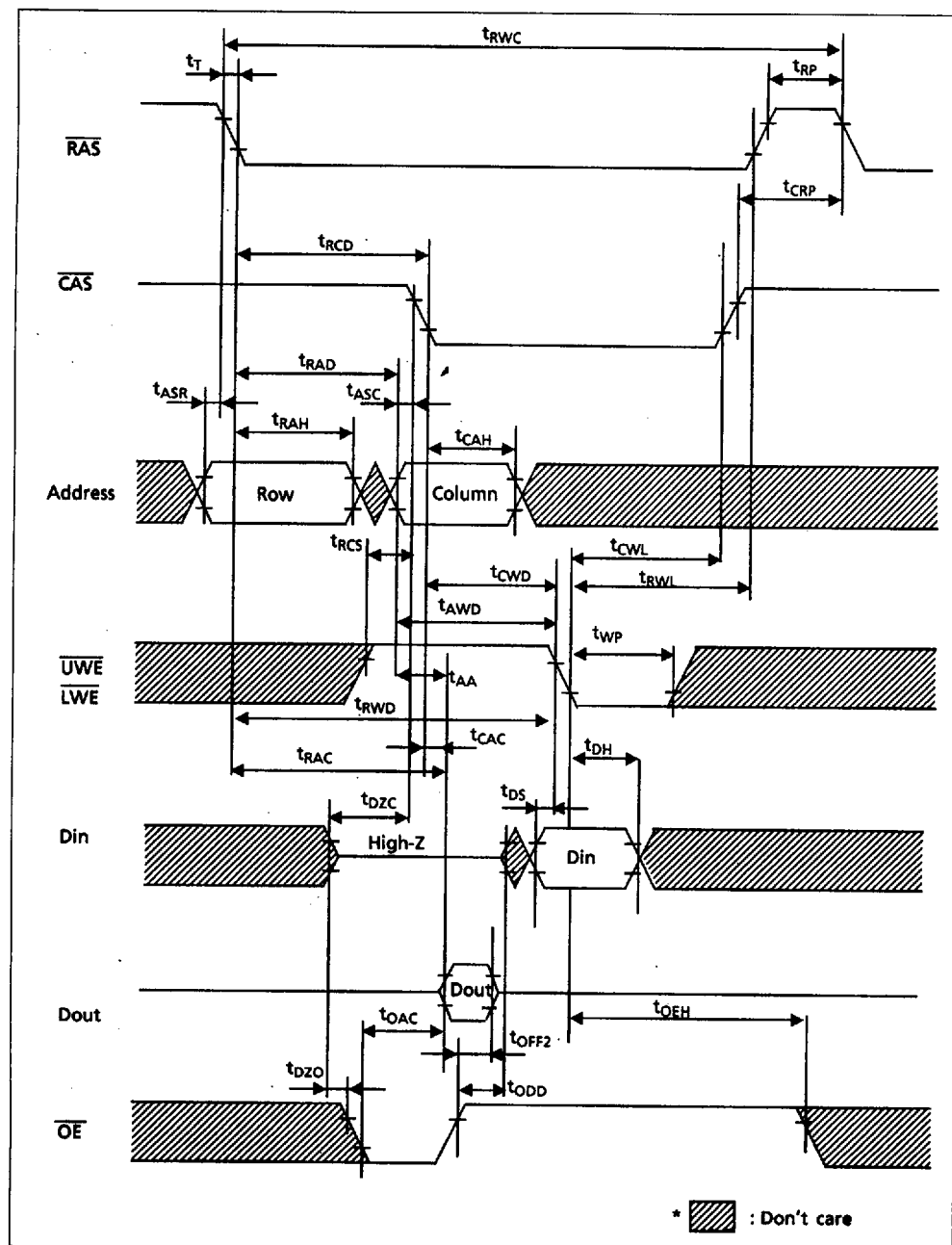
## HITACHI/ LOGIC/ARRAYS/MEM



# HITACHI/ LOGIC/ARRAYS/MEM

## HM514170, HM514170L Series

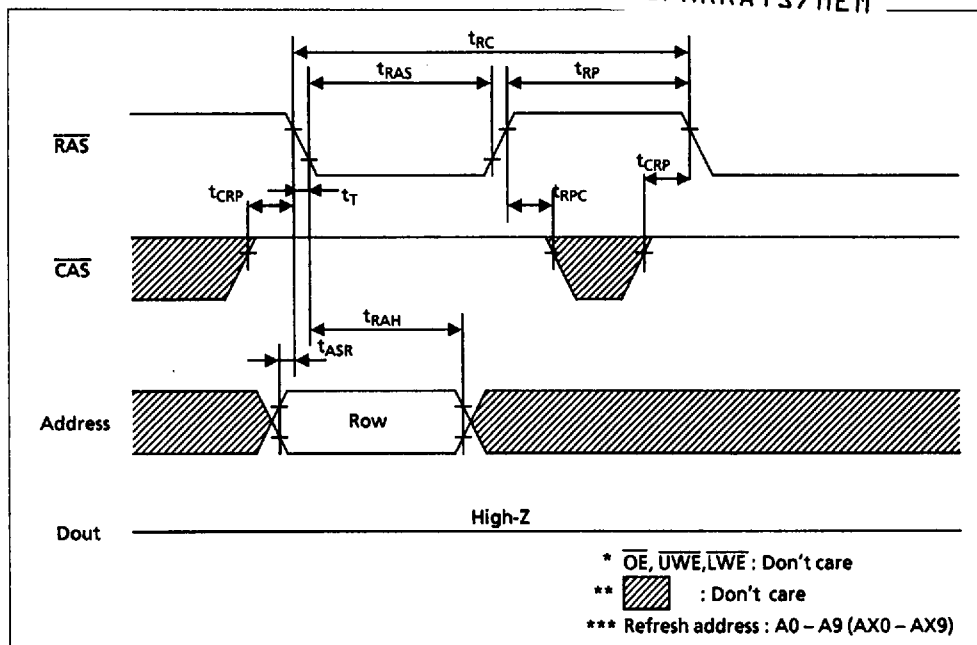
### Read-Modify-Write Cycle



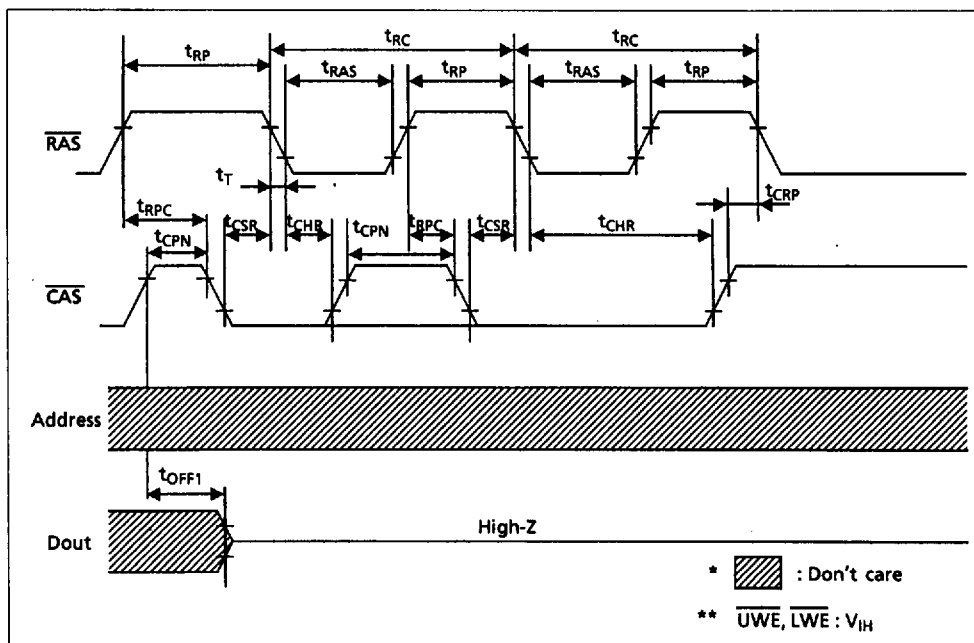
# HM514170, HM514170L Series

## RAS-Only Refresh Cycle

HITACHI/ LOGIC/ARRAYS/MEM

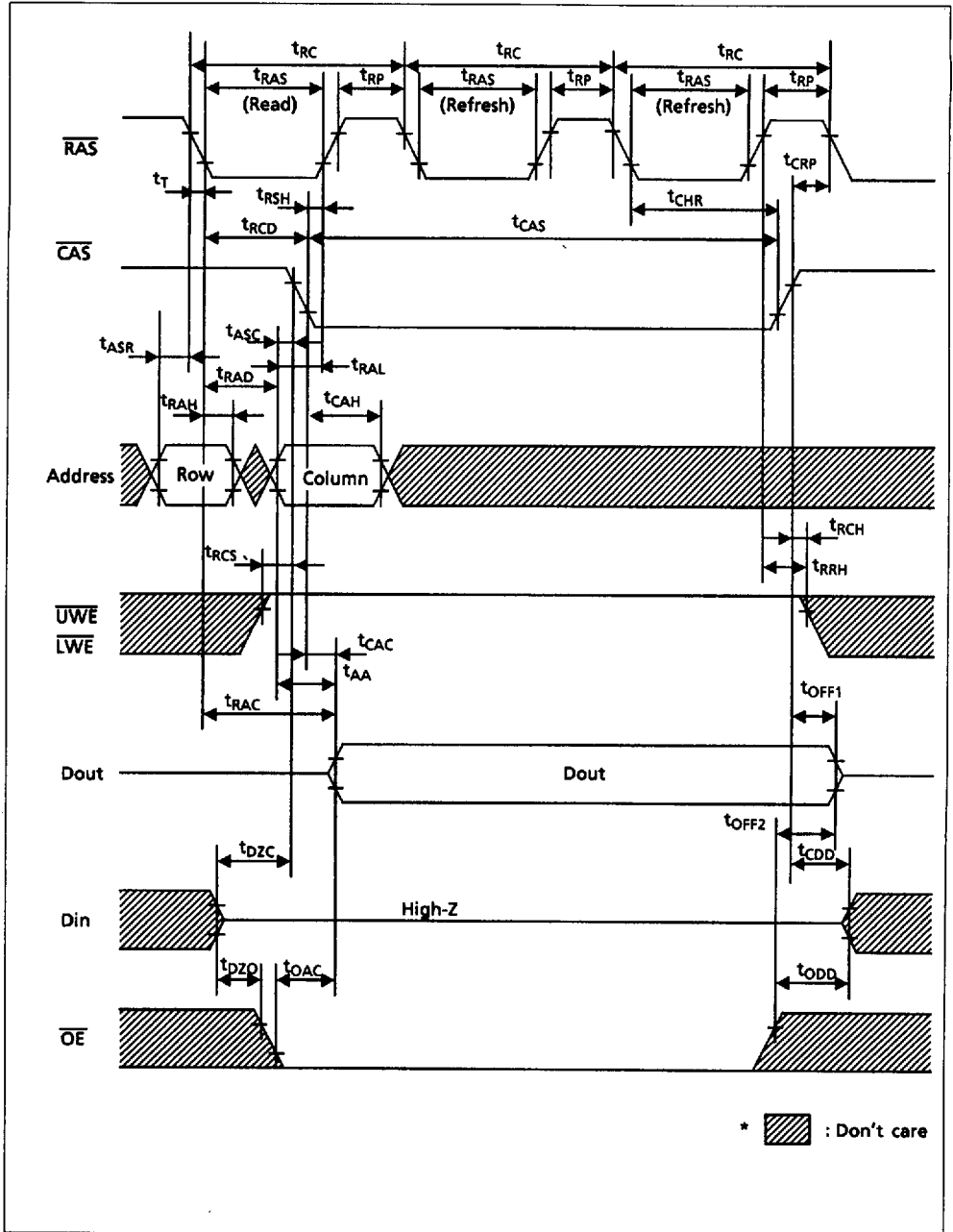


## CAS-Before-RAS Refresh Cycle



**HM514170, HM514170L Series**

**Hidden Refresh Cycle**

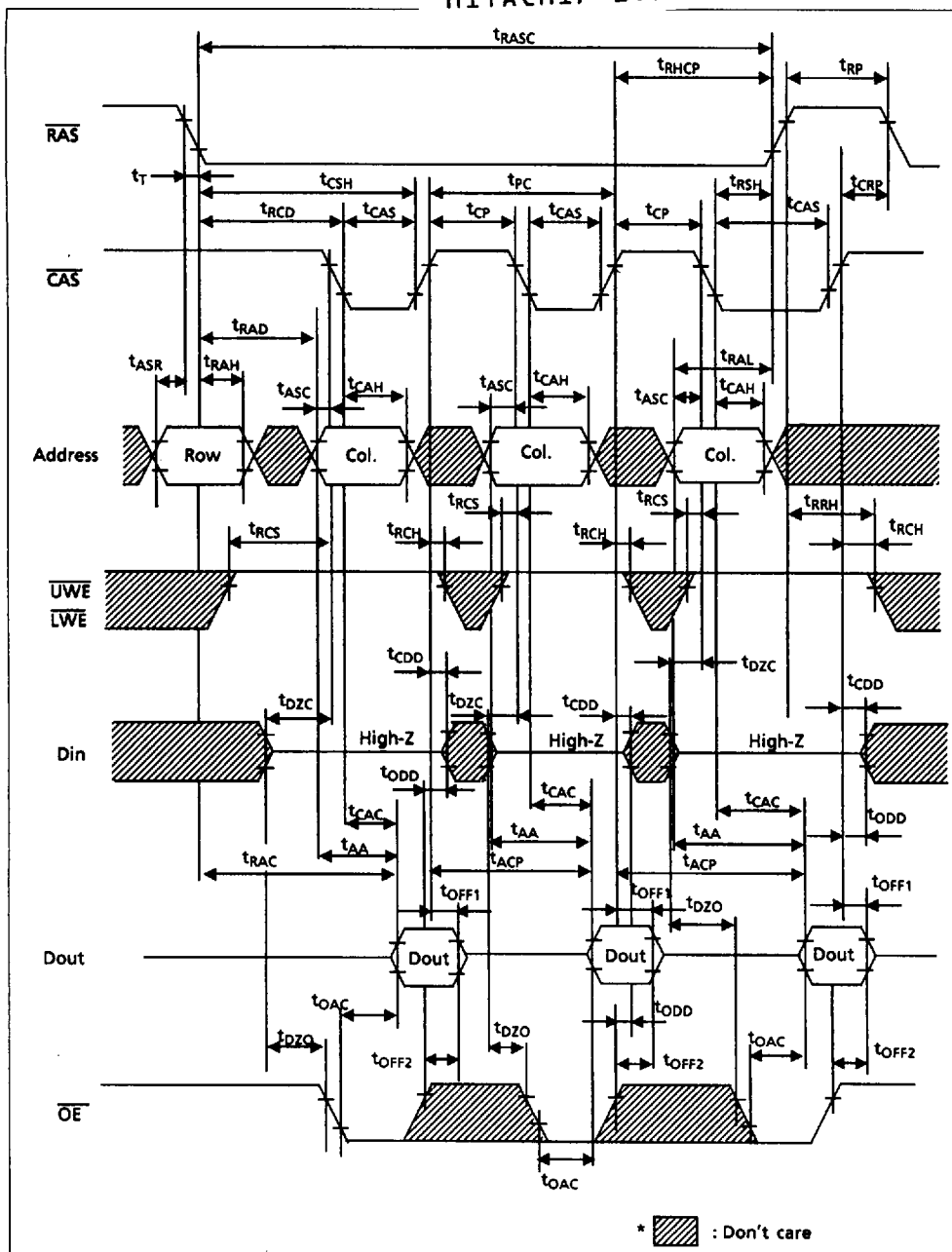


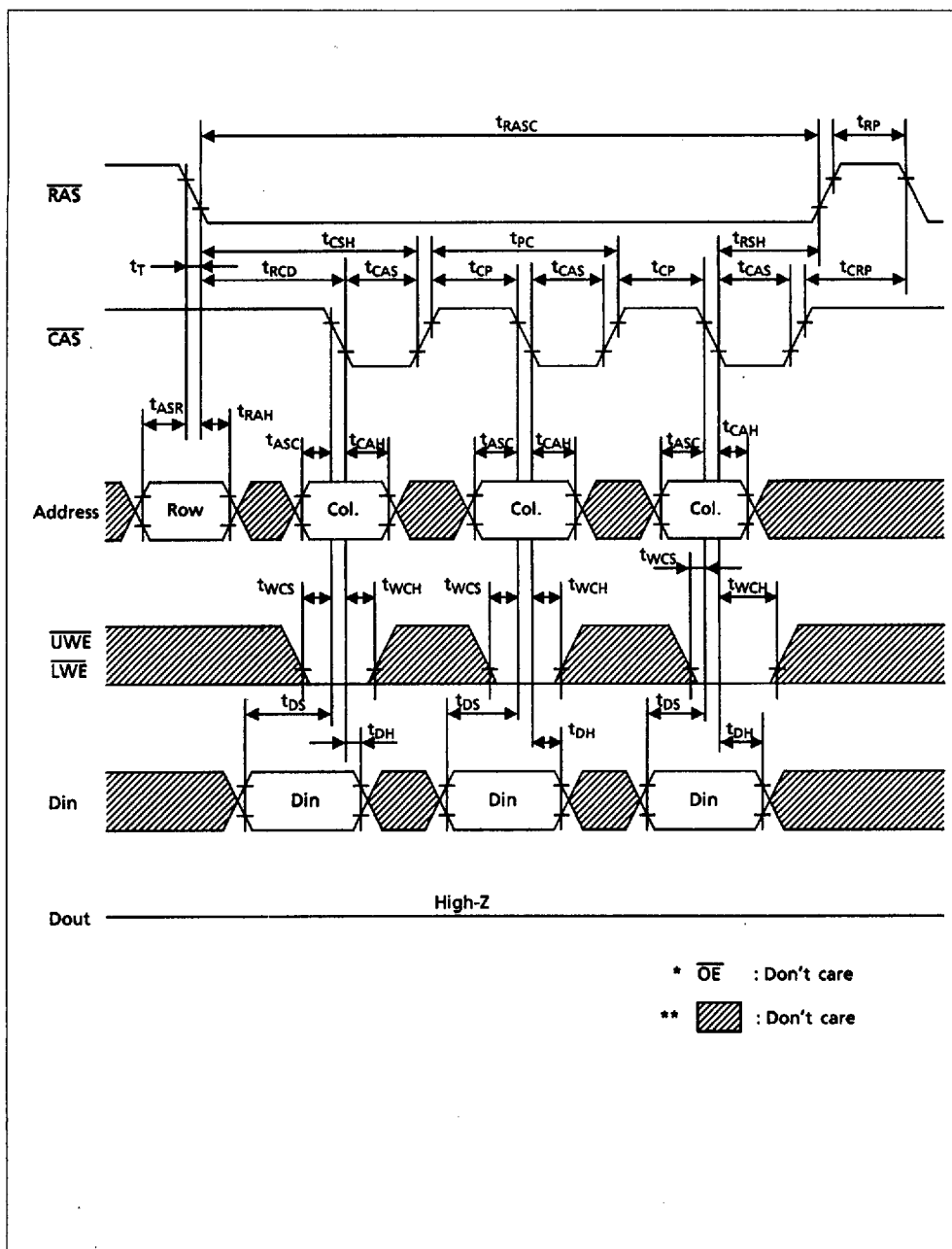


# HM514170, HM514170L Series

## Fast Page Mode Read Cycle

HITACHI/ LOGIC/ARRAYS/MEM

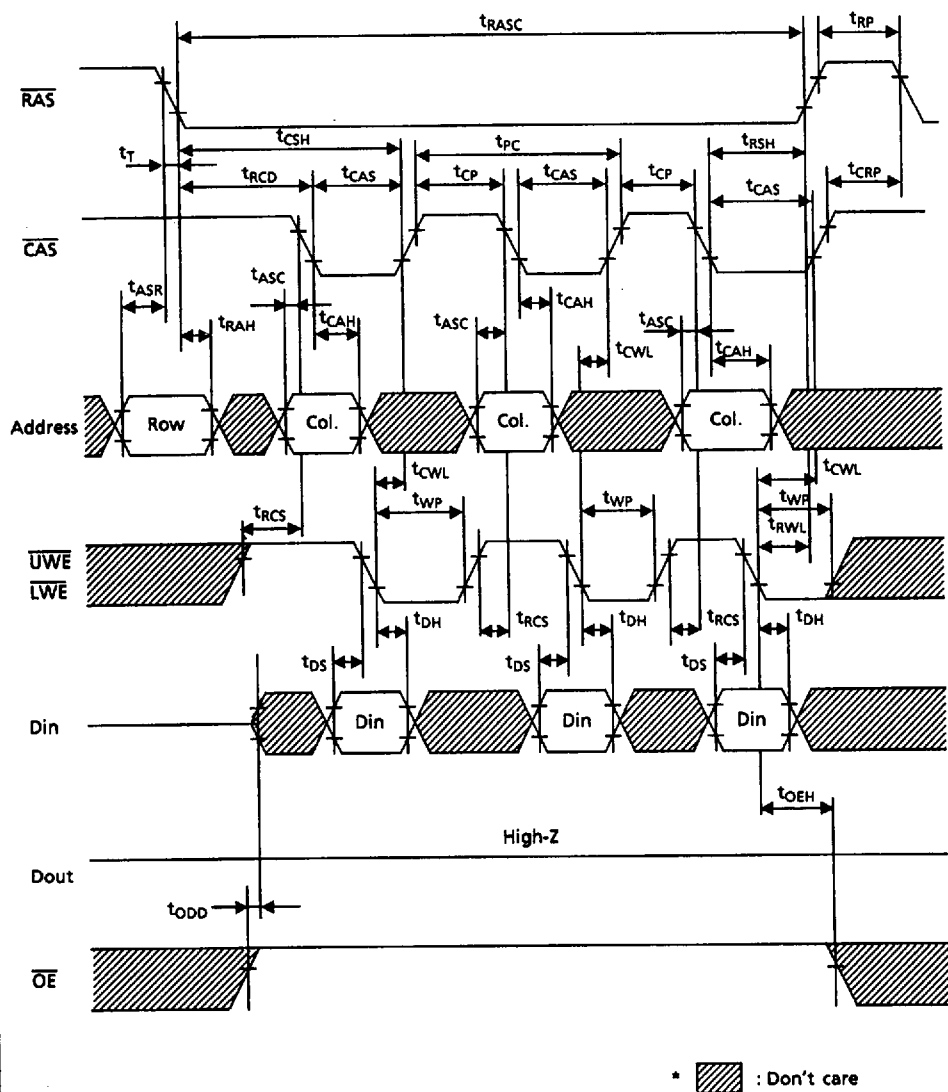


**HM514170, HM514170L Series****HITACHI/ LOGIC/ARRAYS/MEM****Fast Page Mode Early Write Cycle**

## HM514170, HM514170L Series

### Fast Page Mode Delayed Write Cycle

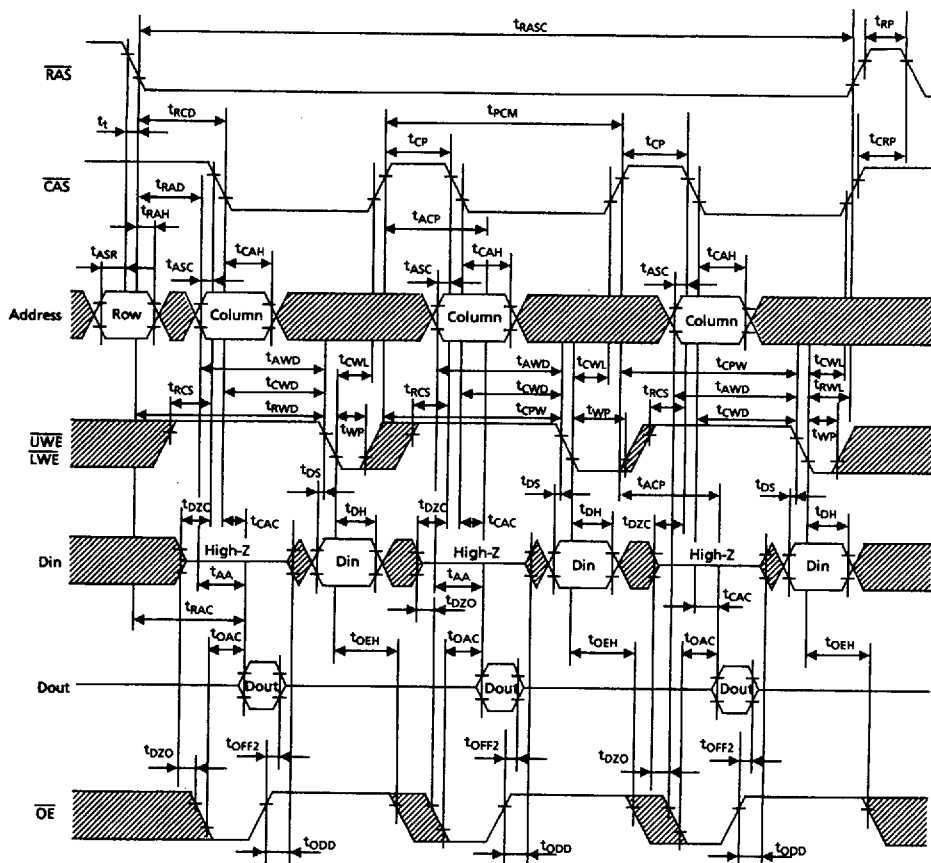
HITACHI/ LOGIC/ARRAYS/MEM



## HM514170, HM514170L Series

### Fast Page Mode Read-Modify-Write Cycle

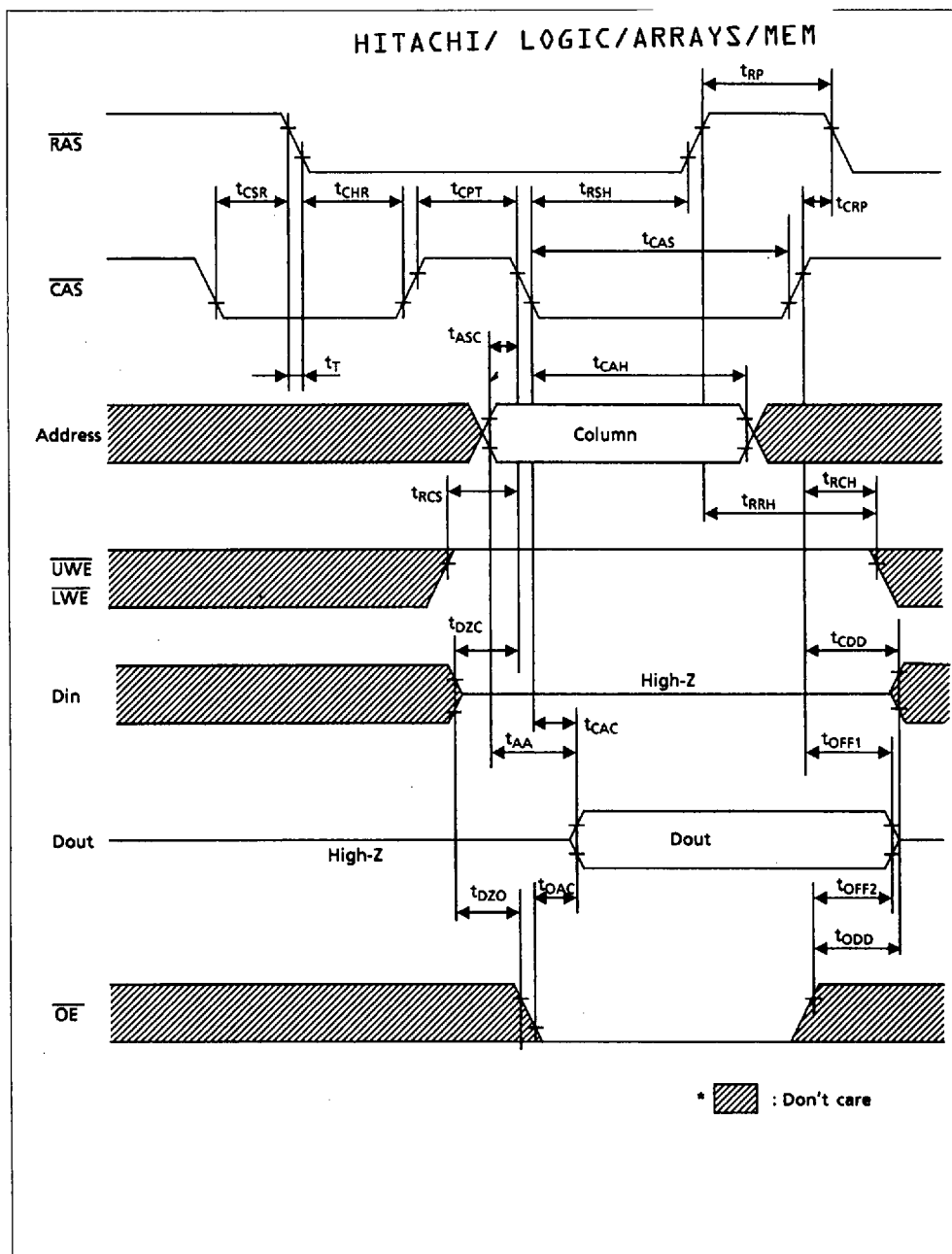
## HITACHI/ LOGIC/ARRAYS/MEM



★  : Don't care

## HM514170, HM514170L Series

CAS-Before-RAS Refresh Counter Check Cycle (Read)



# HM514170, HM514170L Series

CAS-Before-RAS Refresh Counter Check Cycle (Write)

HITACHI/ LOGIC/ARRAYS/MEM

