

HM514256A/AL Series

262,144-Word x 4-Bit CMOS Dynamic RAM

DESCRIPTION

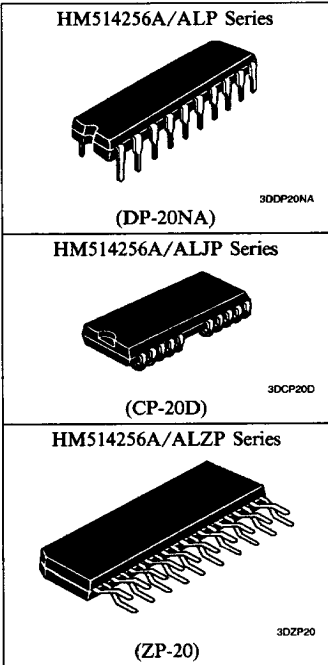
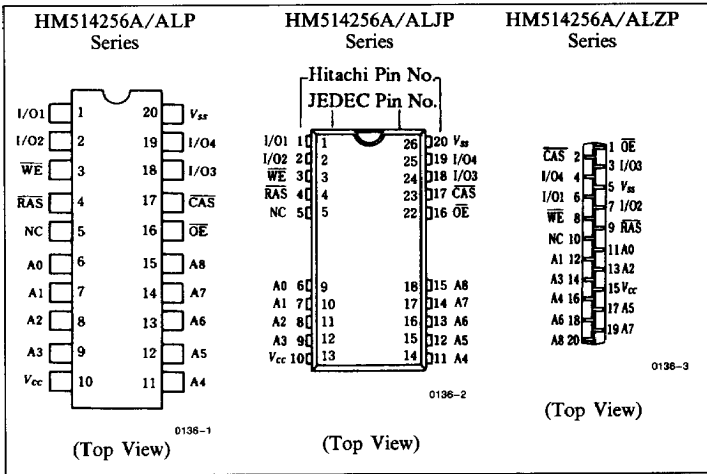
The Hitachi HM514256A/AL is a CMOS dynamic RAM organized 262,144-word x 4-bit. HM514256A/AL has realized higher density, higher performance and various functions by employing 1.3 μ m CMOS technology and some new CMOS circuit design technologies. The HM514256A/AL offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514256A/AL to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

FEATURES

- Single 5V ($\pm 10\%$)
- High Speed
 - Access Time 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
 - Standby 11 mW (max), 1.7 mW (max) (L Version)
 - Active 495 mW/440 mW/363 mW/302.5 mW/258.5 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycles (8 ms), (64 ms) (L Version)
- 2 Variations of Refresh
 - RAS Only Refresh
 - CAS Before RAS Refresh

PIN OUT



PIN DESCRIPTION

Pin Name	Function
A0-A8	Address Input
A0-A8	Refresh Address Input
I/O1-I/O4	Data Input/Data Output
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
VCC	Power Supply (+ 5V)
VSS	Ground

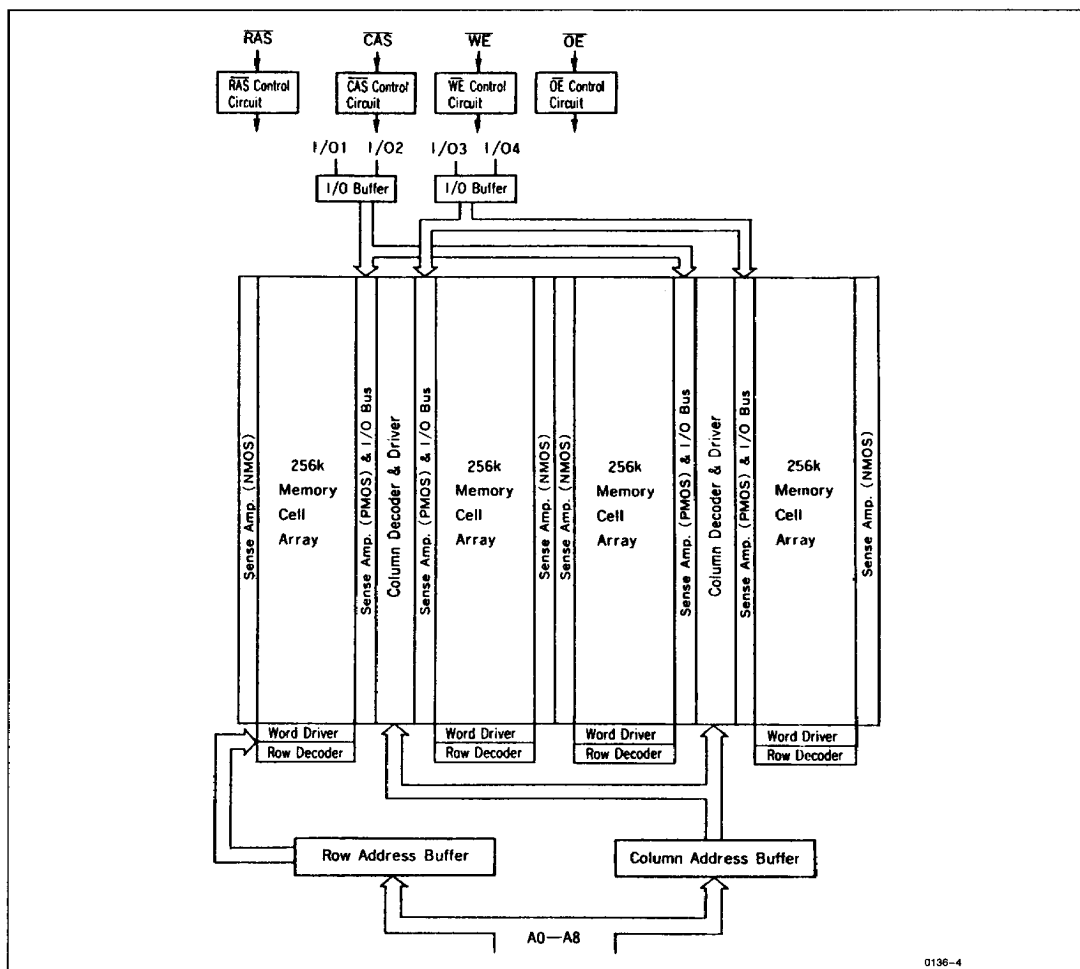


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■ ORDERING INFORMATION

Part No.	Access Time	Package	Part No.	Access Time	Package
HM514256AP-6	60 ns	300-mil 20-pin Plastic DIP (DP-20NA)	HM514256ALP-6	60 ns	300-mil 20-pin Plastic DIP (DP-20NA)
HM514256AP-7	70 ns		HM514256ALP-7	70 ns	
HM514256AP-8	80 ns		HM514256ALP-8	80 ns	
HM514256AP-10	100 ns		HM514256ALP-10	100 ns	
HM514256AP-12	120 ns		HM514256ALP-12	120 ns	
HM514256AJP-6	60 ns	300-mil 20-pin Plastic SOJ (CP-20D)	HM514256ALJP-6	60 ns	300-mil 20-pin Plastic SOJ (CP-20D)
HM514256AJP-7	70 ns		HM514256ALJP-7	70 ns	
HM514256AJP-8	80 ns		HM514256ALJP-8	80 ns	
HM514256AJP-10	100 ns		HM514256ALJP-10	100 ns	
HM514256AJP-12	120 ns		HM514256ALJP-12	120 ns	
HM514256AZP-6	60 ns	400-mil 20-pin Plastic ZIP (ZP-20)	HM514256ALZP-6	60 ns	400-mil 20-pin Plastic ZIP (ZP-20)
HM514256AZP-7	70 ns		HM514256ALZP-7	70 ns	
HM514256AZP-8	80 ns		HM514256ALZP-8	80 ns	
HM514256AZP-10	100 ns		HM514256ALZP-10	100 ns	
HM514256AZP-12	120 ns		HM514256ALZP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55° to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	I/O Pin V_{IL}	-1.0	—	0.8	V	1
	Others V_{IL}	-2.0	—	0.8	V	1

Note: 1. All voltage reference to V_{SS} .• DC Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Item	Symbol	HM514256										Unit	Test Conditions	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	90	—	80	—	66	—	55	—	47	mA	RAS, CAS Cycling, t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	2	—	2	—	2	—	2	—	2	mA	RAS, CAS = V _{IH} D _{out} = High-Z TTL Interface	
		—	1	—	1	—	1	—	1	—	1	mA	RAS, CAS ≥ V _{CC} − 0.2V CMOS Interface	
		—	300	—	300	—	300	—	300	—	300	μA	D _{out} = High-Z CMOS Interface L-Version	
RAS Only Refresh Current	I _{CC3}	—	90	—	80	—	66	—	55	—	47	mA	t _{RC} = Min	2
Battery Backup Current (Only for L-Version)	I _{CC4}	—	300	—	300	—	300	—	300	—	300	μA	t _{RC} = 125 μs CAS Before RAS Cycling	4
Standby Current	I _{CC5}	—	5	—	5	—	5	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} D _{out} = Enable	1
CAS Before RAS Refresh Current	I _{CC6}	—	80	—	70	—	66	—	55	—	47	mA	t _{RC} = Min	
Fast Page Mode Current	I _{CC7}	—	80	—	70	—	55	—	55	—	47	mA	t _{PC} = Min	1, 3
Input Leakage Current	I _{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V _{in} ≤ 7V	
Output Leakage Current	I _{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V _{out} ≤ 7V D _{out} = Disable	



• DC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) (continued)

Item	Symbol	HM514256										Unit	Test Conditions	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High I _{out} = − 5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I _{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
 2. Address can be changed less than three times while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
 4. $t_{RAS} = t_{RAS}(\text{min})$ to $1\text{ }\mu\text{s}$.
 Input Voltage: I/O Pins: $V_{IH} \geq V_{CC} - 0.2V$, $V_{IL} \leq 0.2V$ or High-Z
 The Other Pins: $V_{IH} \geq V_{CC} - 0.2V$, or $V_{IL} \leq 0.2V$

• Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} \pm 10\%$)

Item	Symbol	Typ	Max	Unit	Note
Input Capacitance	Address	C_{I1}	—	5	pF
	Clock	C_{I2}	—	7	pF
Input/Output Capacitance	Data Input/Data Output	$C_{I/O}$	—	10	pF

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable D_{out} .

• AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)¹⁴

Test Conditions

Input Rise and Fall Times 5 ns
 Input Timing Reference Levels 0.8V, 2.4V
 Output Load 2 TTL Gate + C_L (100 pF)
 (Including Scope and Jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	120	—	130	—	160	—	190	—	220	—	ns	
RAS Precharge Time	t _{RP}	50	—	50	—	70	—	80	—	90	—	ns	
RAS Pulse Width	t _{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
CAS Pulse Width	t _{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
RAS to Column Delay Time	t _{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
RAS Hold Time	t _{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
CAS to RAS Precharge Time	t _{CRP}	10	—	10	—	10	—	10	—	10	—	ns	



Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (continued)

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
OE to D _{in} Delay Time	t _{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
OE Delay Time from D _{in}	t _{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
CAS Delay Time from D _{in}	t _{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	3	50	ns	1, 7
Refresh Period	t _{REF}	—	8	—	8	—	8	—	8	—	8	ms	
Refresh Period (Only for L-Version)	t _{REF}	—	64	—	64	—	64	—	64	—	64	ms	

Read Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t _{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access Time from $\overline{\text{OE}}$	t _{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{CAS}}$	t _{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{RAS}}$	t _{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t _{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-off to $\overline{\text{OE}}$	t _{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{\text{CAS}}$ to D _{in} Delay Time	t _{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t _{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to RAS Lead Time	t _{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to CAS Lead Time	t _{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold time	t _{DH}	15	—	15	—	15	—	20	—	25	—	ns	11



Read-Modify-Write Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t _{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
RAS to WE Delay Time	t _{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
CAS to WE Delay Time	t _{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column Address to WE Delay Time	t _{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
OE Hold Time from WE	t _{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

Refresh Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh Cycle)	t _{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh Cycle)	t _{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t _{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode CAS Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode RAS Pulse Width	t _{RASC}	—	100000	—	100000	—	100000	—	1000000	—	100000	ns	12
Access Time from CAS Precharge	t _{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
RAS Hold Time from CAS Precharge	t _{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t _{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

- Notes: 1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. Transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .



- **Read Cycle**

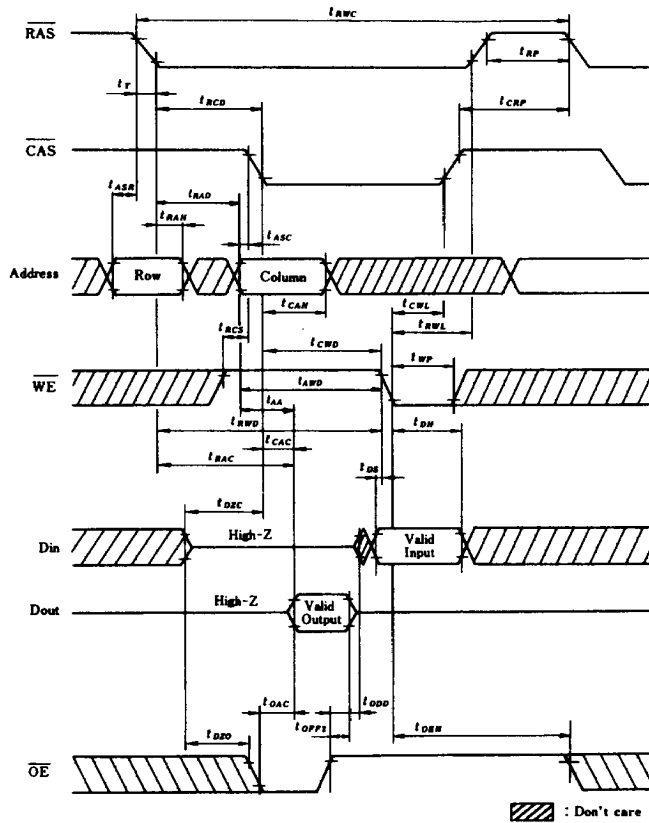




- **Delayed Write Cycle**

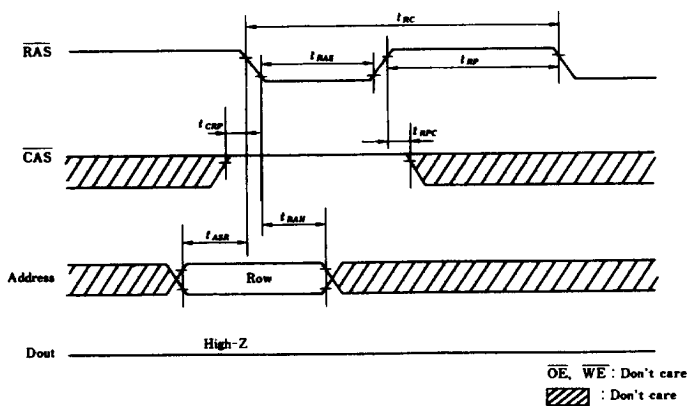


• Read-Modify-Write Cycle



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• RAS Only Refresh Cycle



OE, WE : Don't care
 : Don't care

0136-9



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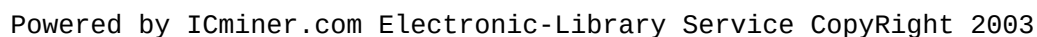
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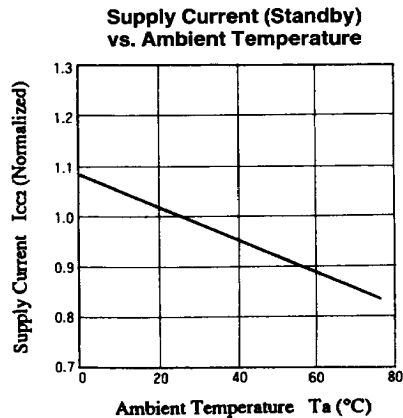
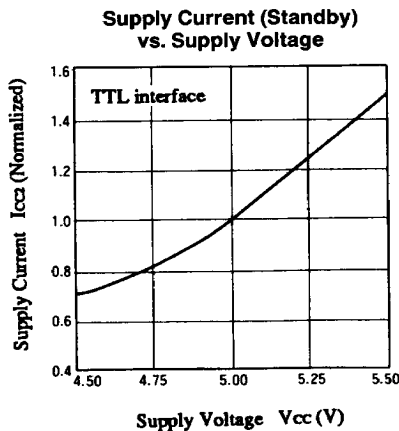
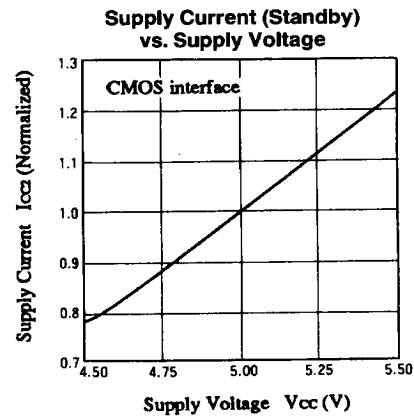
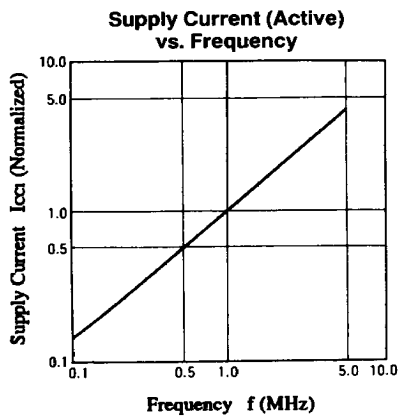
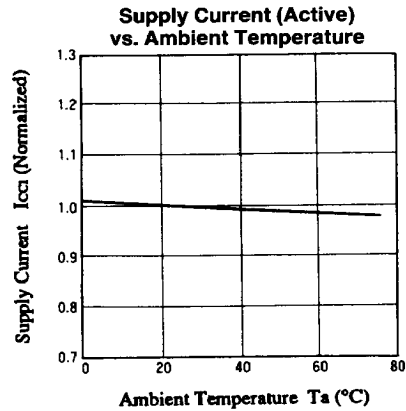
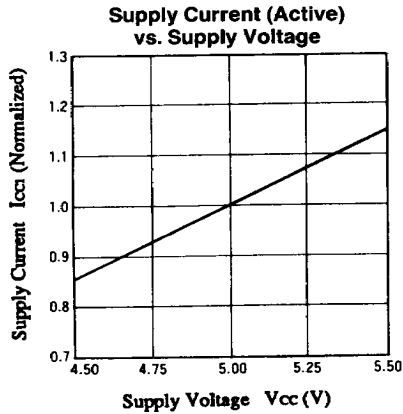
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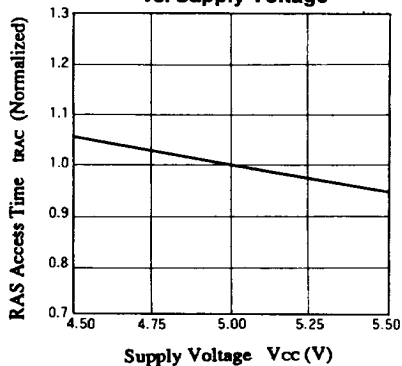
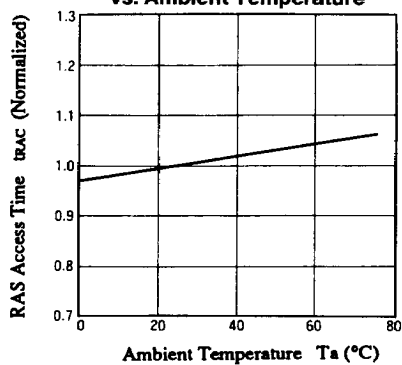
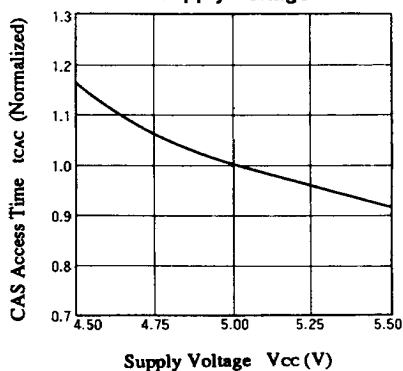
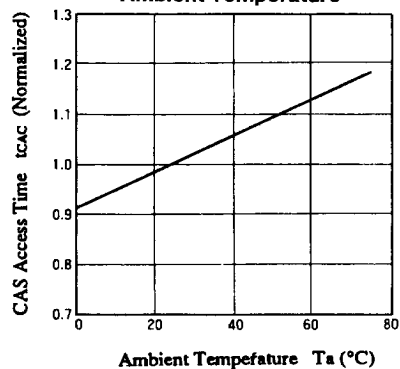
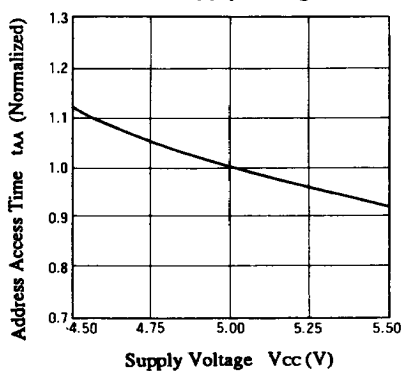
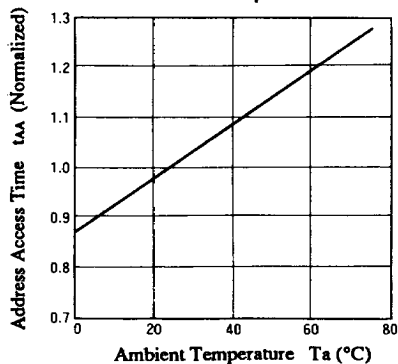


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**RAS Access Time
vs. Supply Voltage****RAS Access Time
vs. Ambient Temperature****CAS Access Time vs.
Supply Voltage****CAS Access Time vs.
Ambient Temperature****Address Access Time
vs. Supply Voltage****Address Access Time vs.
Ambient Temperature**

0136-16

