ADE-203-186A (Z)

HM5241605 Series

131,072-word × 16-bit × 2-bank Synchronous Dynamic RAM

HITACHI

Rev. 1.0
Nov. 18, 1994

All inputs and outputs are referred to the rising edge of the clock input. The HM5241605 is offered in 2 banks for improved performance.

Features

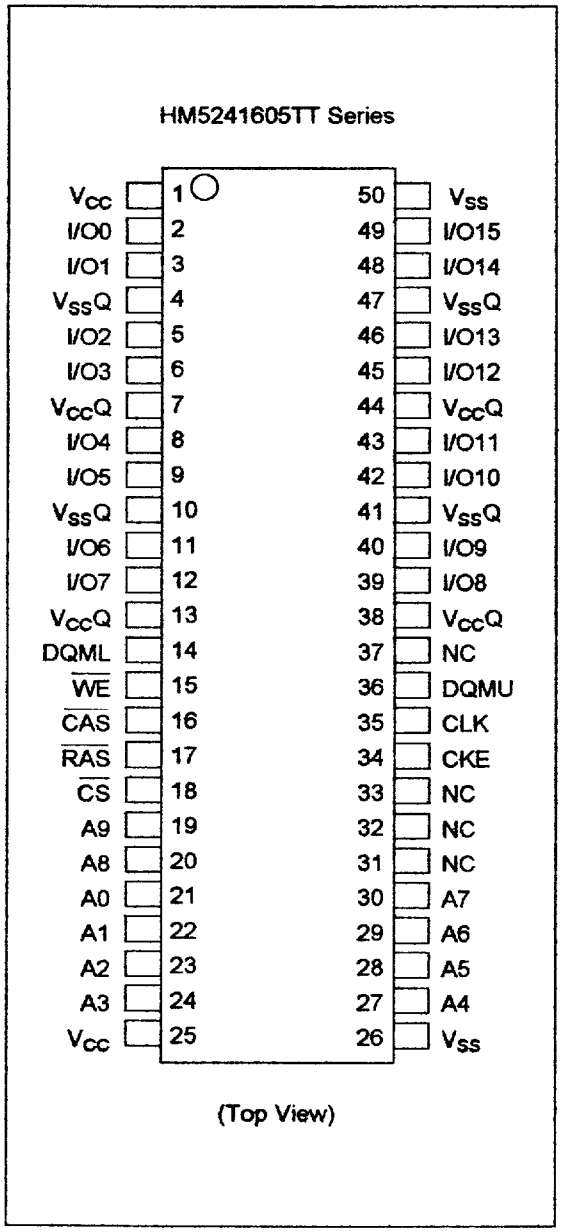
- 3.3V Power supply
- Clock frequency
  66 MHz/57 MHz/50 MHz
- LVTTL interface
- Single pulsed $\overline{RAS}$
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length
  1/2/4/8/full page
- Programmable burst sequence
  Sequential/interleave
- Full page burst length capability
  Sequential burst
  burst stop capability
- Programmable $\overline{CAS}$ latency
  1/2/3
- Byte control by DQMU and DQML
- 1024 refresh cycles: 16 ms
- 2 variations of refresh
  — Auto refresh
  — Self refresh

Ordering Information

Type No.	Frequency	Package
HM5241605TT-20	50 MHz	400-mil 50-pin
HM5241605TT-17	57 MHz	plasticTSOP II
HM5241605TT-15	66 MHz	(TTP-50D)

Hitachi semiconductor

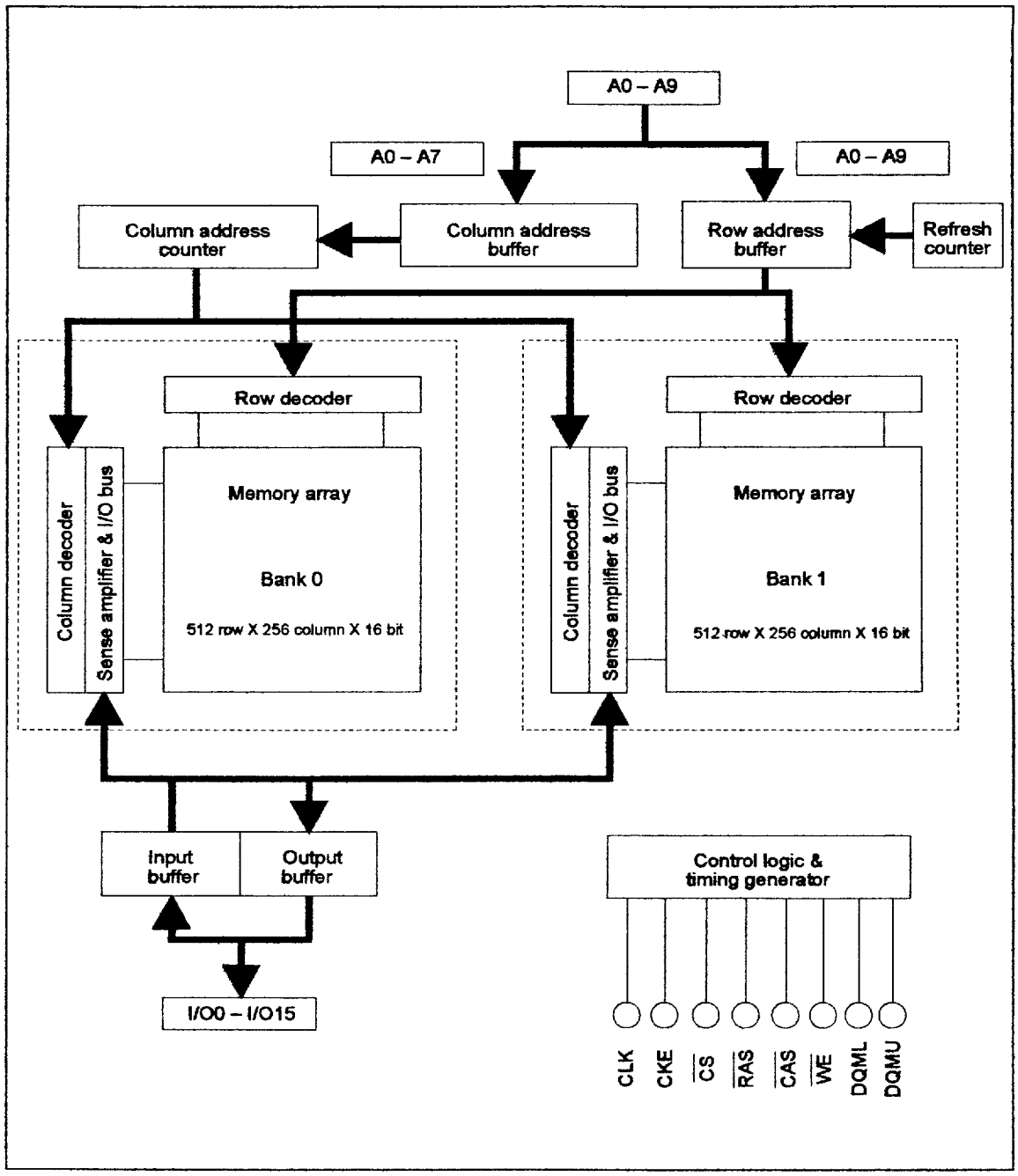
Pin Arrangement



Pin Description

Pin name	Function
A0 – A9	Address input — Row address A0 – A8 — Column address A0 – A7 — Bank select address A9
I/O0 – I/O15	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable command
DQMU DQML	Upper byte input/output mask Lower byte input/output mask
CLK	Clock input
CKE	Clock enable
V_{CC}	Power for internal circuit (3.3 V)
V_{SS}	Ground for internal circuit
$V_{CC}Q$	Power for I/O pin (3.3 V)
$V_{SS}Q$	Ground for I/O pin
NC	No connection

Block Diagram



Pin Functions

- CLK (input pin):

  CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

- $\overline{CS}$ (input pin):

  When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

- $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins):

  Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

- A0 to A8 (input pins):

  Row address (AX0 to AX8) is determined by A0 to A8 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY7) is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A8 defines the precharge mode. When A8 = High at the precharge command cycle, both banks are precharged. But when A8 = Low at the precharge command cycle, only the bank that is selected by A9 (BS) is precharged.

- A9 (input pin):

  A9 is a bank select signal (BS). The memory array of the HM5241605 is divided into bank 0 and bank 1, both which contain 512 row × 256 column × 16 bits. If A9 is Low, bank 0 is selected, and if A9 is High, bank 1 is selected.

- CKE (input pin):

  This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

- DQMU/DQML (input pins):

  DQMU controls upper byte and DQML controls lower byte input/output buffers.

  Read operation: If DQMU/DQML is High, the output buffer becomes High-Z. If the DQMU/DQML is Low, the output buffer becomes Low-Z.

  Write operation: If DQMU/DQML is High, the previous data is held (the new data is not written). If DQMU/DQML is Low, the data is written.

- I/O0 to I/O15 (I/O pins):

  Data is input to and output from these pins. These pins are the same as those of a conventional DRAM.

- V_{CC} and $V_{CC}Q$ (power supply pins):

  3.3 V is applied. (V_{CC} is for the internal circuit and $V_{CC}Q$ is for the output buffer.)

- V_{SS} and $V_{SS}Q$ (power supply pins):

  Ground is connected. (V_{SS} is for the internal circuit and $V_{SS}Q$ is for the output buffer.)

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE n - 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A7 - 0
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all bank	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

Note: H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}. V: Valid address input

- Ignore command [DESL]:

  When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignore command input at the clock. However, the internal status is held.

- No operation [NOP]:

  This command is not an execution command. However, the internal operations continue.

- Burst stop in full-page [BST]:

  This command stops a full-page burst operation (burst length = full-page(256)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for a full-page of data (256), it automatically returns to the start address, and input/output is performed repeatedly.

- Column address strobe and read command [READ]:

  This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0-AY7) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

- Read with auto-precharge [READ A]:

  This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4, or 8. When the burst length is full-page(256), this command is illegal.

- Column address strobe and write command [WRIT]:

  This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7) and the bank select address (A9) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7) and the bank select address (A9).

- Write with auto-precharge [WRIT A]:

  This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation. When the burst length is full-page(256), this command is illegal.

- Row address strobe and bank activate [ACTV]:

  This command activates the bank that is selected by A9(BS) and determines the row address (AX0-AX8). When A9 is Low, bank 0 is activated. When A9 is High, bank 1 is activated.

- Precharge selected bank [PRE]:

  This command starts precharge operation for the bank selected by A9. If A9 is Low, bank 0 is selected. If A9 is High, bank 1 is selected.

- Precharge all banks [PALL]:

  This command starts a precharge operation for all banks.

- Refresh [REF/SELF]:

  This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

- Mode register set [MRS]:

  Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0-A9) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE n - 1	CKE n	DQM U	DQM L
Upper byte write enable/output enable	ENBU	H	X	L	X
Lower byte write enable/output enable	ENBL	H	X	X	L
Upper byte write inhibit/output disable	MASKU	H	X	H	X
Lower byte write inhibit/output disable	MASKL	H	X	X	H

Note: H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}.

The HM5241605 series can mask input/output data by means of DQMU and DQML. DQMU masks the upper byte and DQML masks the lower byte.

During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, enabling data output. On the other hand, when DQMU/DQML is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMU/DQML to Low. When DQMU/DQML is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMU/DQML. For details, refer to the DQM control section of the HM5241605 operating instructions.

CKE Truth Table

Current state	Function		CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	Auto-refresh command	REF	H	H	L	L	L	H	X
Idle	Self-refresh entry	SELF	H	L	L	L	L	H	X
Idle	Power down entry		H	L	L	H	H	H	X
			H	L	H	X	X	X	X
Self refresh	Self refresh exit	SELFX	L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Power down	Power down exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X

Note: H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}.

- Clock suspend mode entry:

  The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

- ACTIVE clock suspend:

  This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

- READ suspend and READ A suspend:

  The data being output is held (and continues to be output).

- WRITE suspend and WRIT A suspend:

  In this mode, external signals are not accepted. However, the internal state is held.

- Clock suspend:

  During clock suspend mode, keep the CKL to Low.

- Clock suspend mode exit:

  The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

- IDLE:

  In this state, all banks are not selected, and completed precharge operation.

- Auto-refresh command [REF]:

  When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 1,024 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

- Self-refresh entry [SELF]:

  When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

- Power down mode entry:

  When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

- Self-refresh exit:

  When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

- Power down exit:

  When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after tRP
	L	H	H	H	X	NOP	Enter IDLE after tRP
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A8	PRE, PALL	NOP

Function Truth Table (cont)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Idle	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	Begin read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A8	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (cont.)

Current state	CS	RAS	CAS	WE	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A8	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	Term burst write an Precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active*3 ILLEGAL on same bank
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after tRC
	L	H	H	H	X	NOP	Enter IDLE after tRC
	L	H	H	L	X	BST	Enter IDLE after tRC
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes 1. H: V_{IH}. L: V_{IL}. X: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of tRWL is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

- To [DESL], [NOP] or [BST]:

  When these commands are executed, the synchronous DRAM enters the IDLE state after tRP has elapsed from the completion of precharge.

From [IDLE]

- To [DESL], [NOP], [BST], [PRE] or [PALL]:

  These commands result in no operation.

- To [ACTV]:

  The bank specified by the address pins and the ROW address is activated.

- To [REF], [SELF]:

  The synchronous DRAM enters refresh mode (auto-refresh or self- refresh).

- To [MRS]:

  The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

- To [DESL], [NOP] or [BST]:

  These commands result in no operation.

- To [READ], [READ A]:

  A read operation starts. (However, an interval of tRCD is required.)

- To [WRIT], [WRIT A]:

  A write operation starts. (However, an interval of t_{RCD} is required.)

- To [ACTV]:

  This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

- To [PRE], [PALL]:

  These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

- To [DESL], [NOP]:

  These commands continue read operations until the burst operation is completed.

- To [BST]:

  This command stops a full-page burst.

- To [READ], [READ A]:

  Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

- To [WRIT], [WRIT A]:

  These commands stop a burst read, and start a write cycle.

- To [ACTV]:

  This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

- To [PRE], [PALL]:

  These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

- To [DESL], [NOP]:

  These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

- To [ACTV]:

  This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

- To [DESL], [NOP]:

  These commands continue write operations until the burst operation is completed.

- To [BST]:

  This command stops a full-page burst.

- To [READ], [READ A]:

  These commands stop a burst and start a read cycle.

- To [WRIT], [WRIT A]:

  These commands stop a burst and start the next write cycle.

- To [ACTV]:

  This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

- To [PRE], [PALL]:

  These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

- To [DESL], [NOP]:

  These commands continue write operations until the burst is completed, and the synchronous DRAM enters precharge mode.

- To [ACTV]:

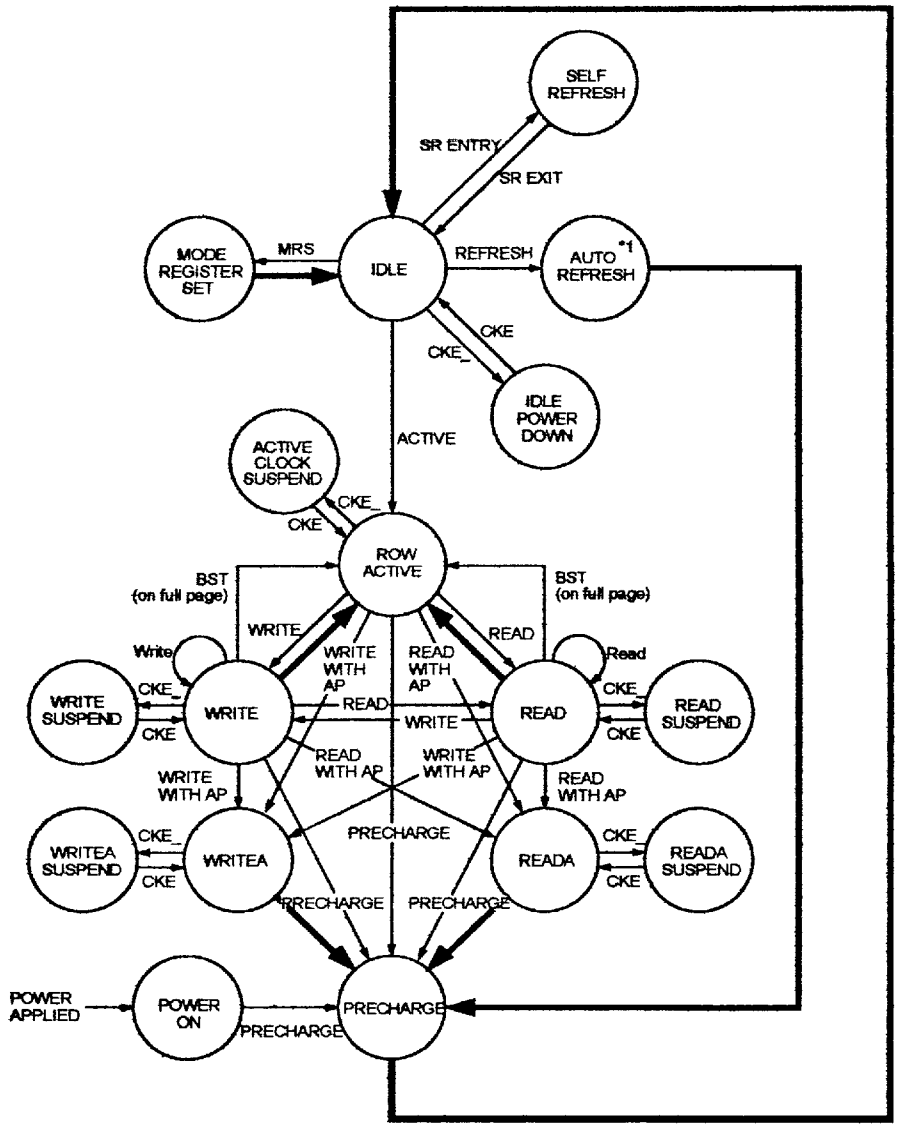
  This command makes the other bank activ. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]:

After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the IDLE state.

Simplified State Diagram



Automatic transition after completion of command.

Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A9) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

- A9 and A8: (OPCODE)

  The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

- Burst read and BURST WRITE

  Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

- Burst read and SINGLE WRITE

  Data is only written to the column address specified during the write cycle, regardless of the burst length.

- A7

  Keep this bit Low at the mode register set cycle.

- A6, A5, A4: (LMODE)

  These pins specify the $\overline{CAS}$ latency.

- A3: (BT)

  A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

- A2, A1, A0: (BL)

  These pins specify the burst length.

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE		0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

F.P. =Full Page (256)
R is Reserved(inhibit)

A9	A8	Write mode
0	0	Burst read and burst write
0	1	R
1	0	Burst read and SINGLE WRITE
1	1	R

Burst Sequence

Burst length = 2

Stating Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Stating Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Stating Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Operation of HM5241605 Series

Read/Write Operations

- Bank active

  Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A9 pin, and the row address (AX0 to AX8) is activated by the A0 to A8 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

- Read operation

  A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency - 1) cycle after read command set. HM5241605 series can perform a burst read operation.

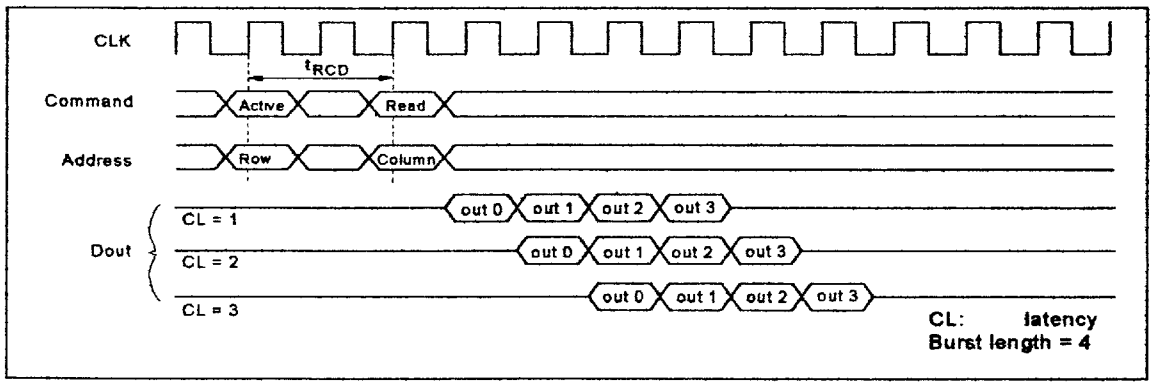
The burst length can be set to 1,2,4,8 or full-page(256). The start address for a burst read is specified by the column address (AY0 to AY7) and the bank select address (A9) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 1,2,3.

When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output.

When the burst length is full-page(256), data is repeatedly output until the burst stop command is input.

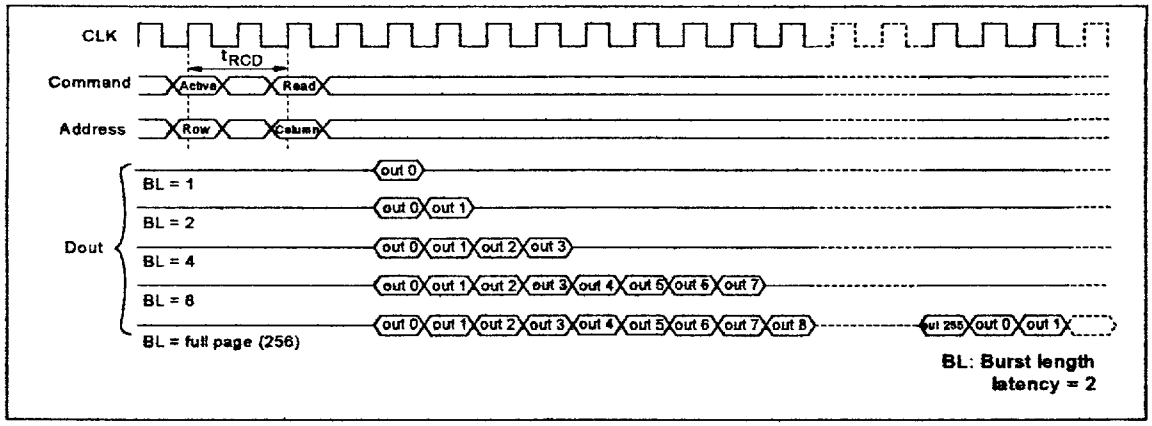
The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency



Read/Write Operations (cont)

Burst Length



- Write operation

Burst write or single write mode is selected by the OPCODE (A9, A8) of the mode register.

1. Burst write:

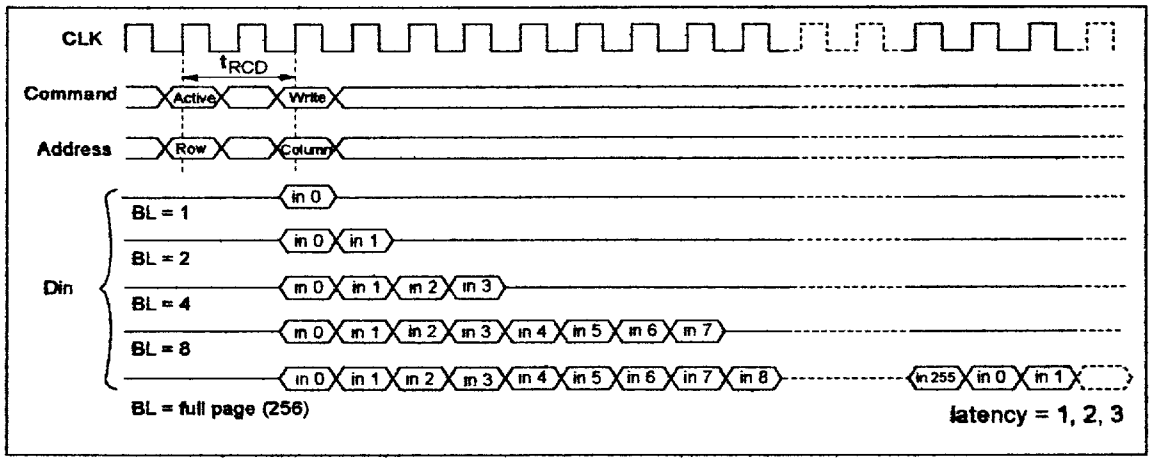
A burst write operation is enabled by setting OPCODE(A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address (AY0 to AY7) and the bank select address (A9) at the write command set cycle.

2. Single write:

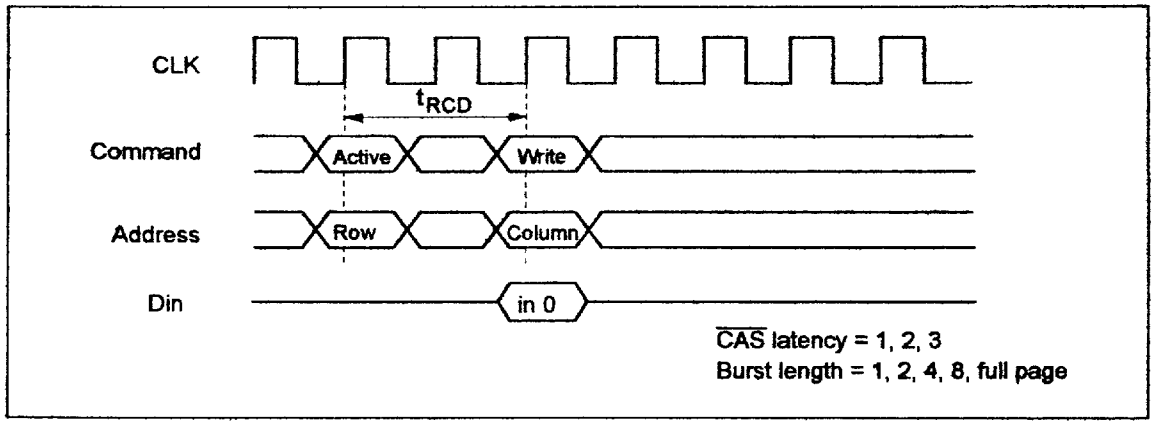
A single write operation is enabled by setting OPCODE(A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY7) and the bank select address (A9) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).

Read/Write Operations (cont)

Burst Write



Single Write



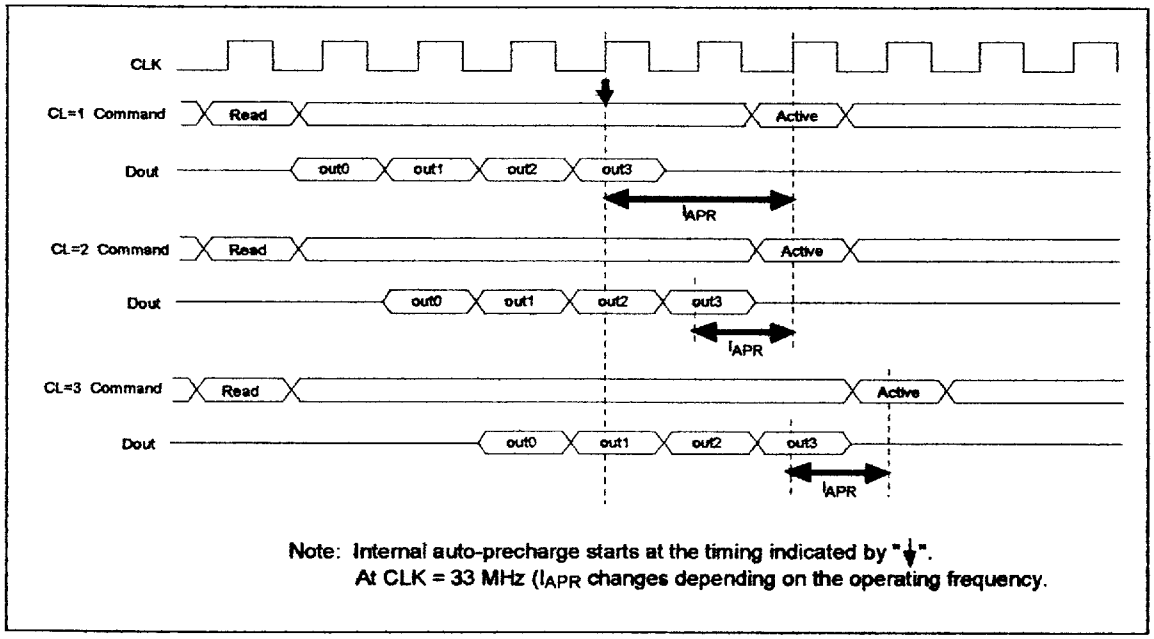
Read/Write Operations (cont)

- Read with auto-precharge:

  In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation.

  The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by t_{APR} is required before execution of the next command.

CAS latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output
1	same cycle as the final data is output



Note: Internal auto-precharge starts at the timing indicated by "↓".
At CLK = 33 MHz (t_{APR} changes depending on the operating frequency.

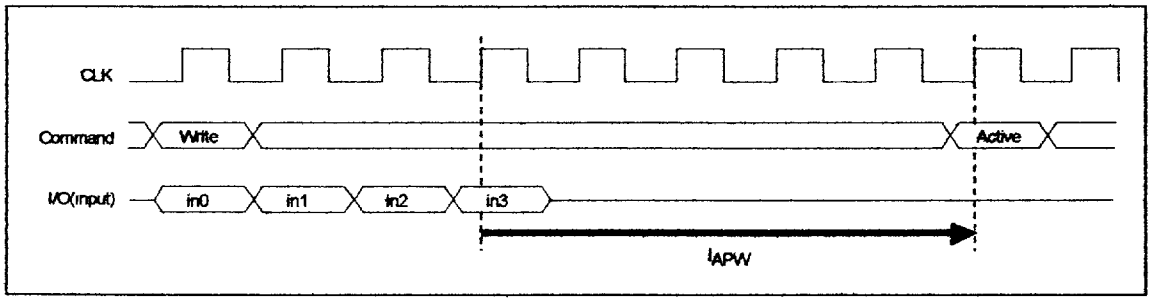
Read/Write Operations (cont)

- Write with auto-precharge:

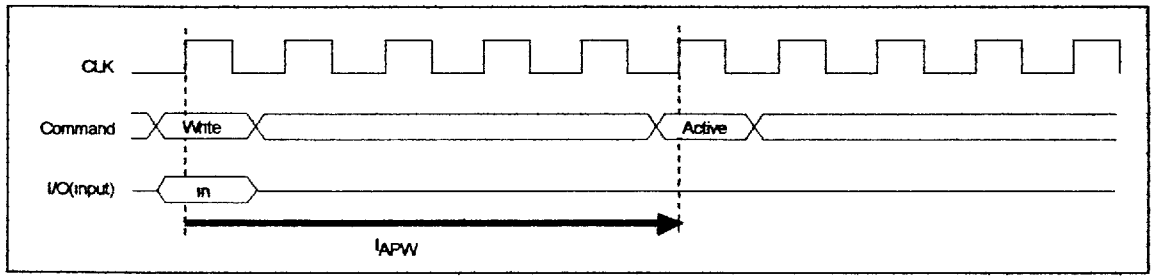
  In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation.

  The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of t_{APW} is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write



Full-page Burst Stop

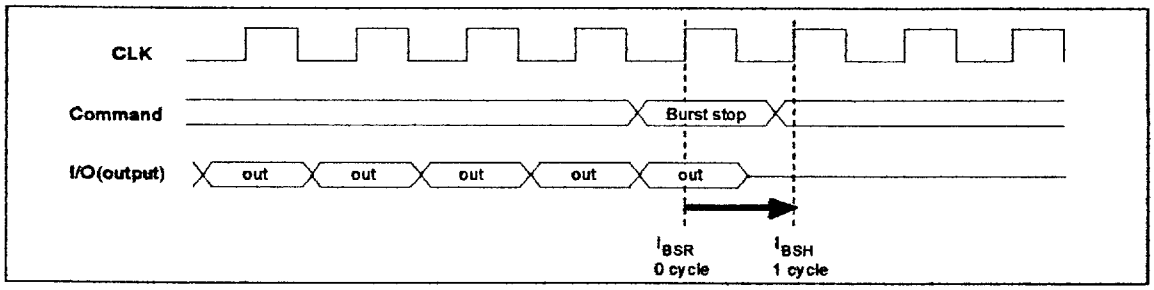
- Burst stop command during burst read:

  The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read.

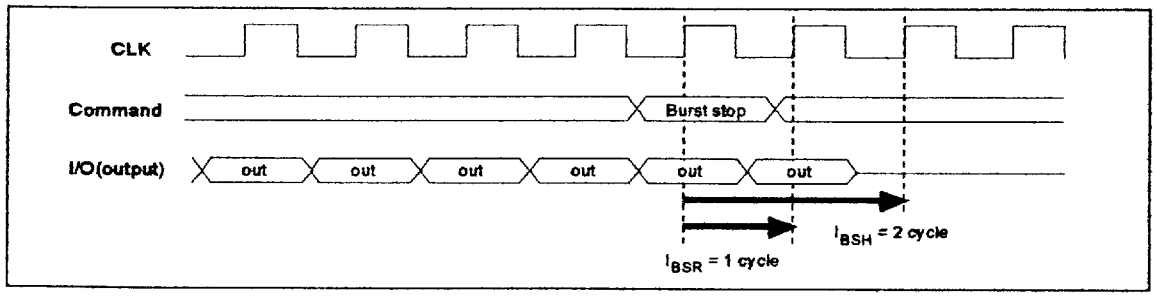
The timing from command input to the last data changes depending on the $\overline{CAS}$ latency setting. When the $\overline{CAS}$ latency is 3, the data becomes invalid two cycles after the BST command. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8.

$\overline{CAS}$ latency	BST to valid data	BST to high impedance
1	0	1
2	1	2
3	1	3

$\overline{CAS}$ Latency = 1, Burst Length = full page

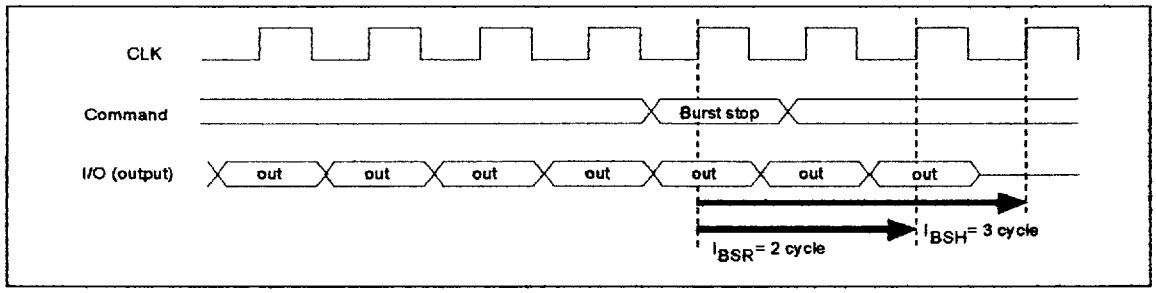


$\overline{CAS}$ Latency = 2, Burst Length = full page



Full-page Burst Stop (cont)

$\overline{\text{CAS}}$ Latency = 3, Burst Length = full page

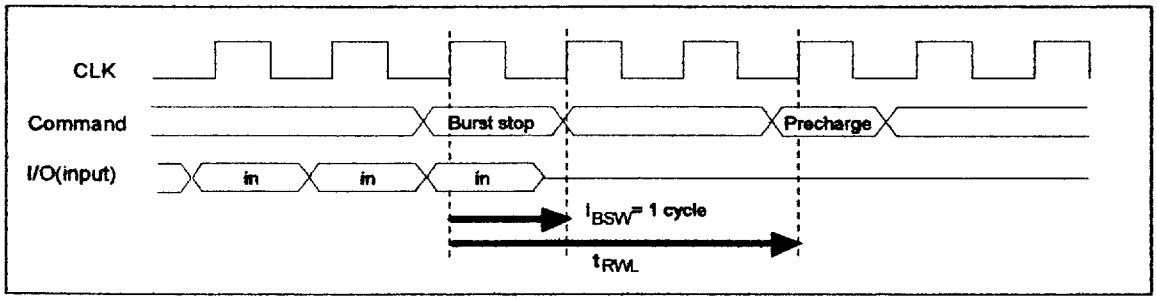


- Burst stop command at burst write:

  The burst stop command (BST command) is used to stop data input during a full-page burst write. Data is still written in the same cycle as the BST command, but no data is written in subsequent cycles.

  In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8. And an interval of t_{RWL} is required between the BST command and the next precharge command.

Burst Length = full page



Command Intervals

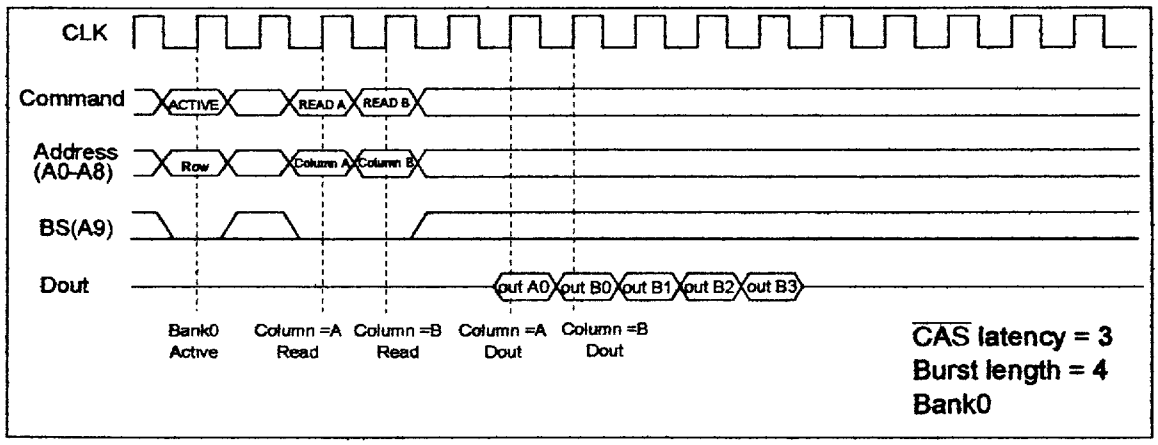
- Read command to Read command interval

1. Same bank, same ROW address:

   When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle.

   Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (same ROW address in same bank)



2. Same bank, different ROW address:

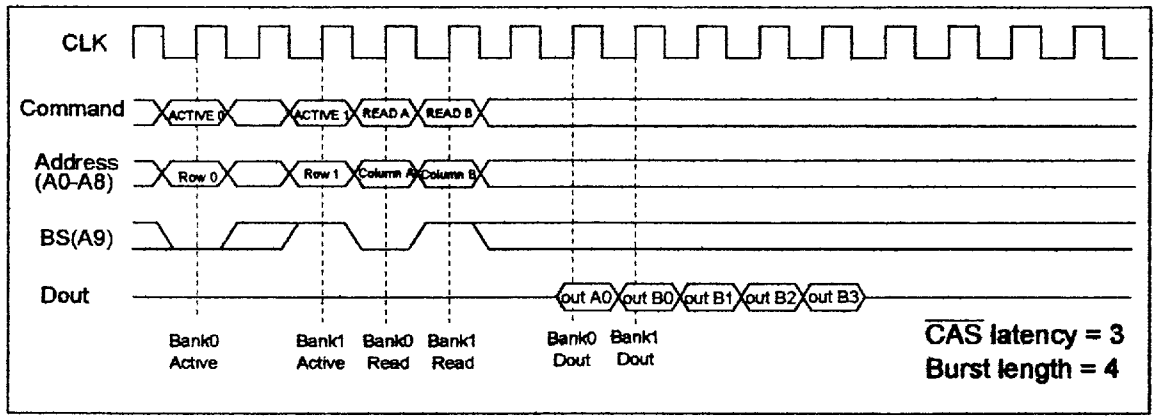
   When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

3. Different bank:

   When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

Command Intervals (cont)

READ to READ Command Interval (different bank)



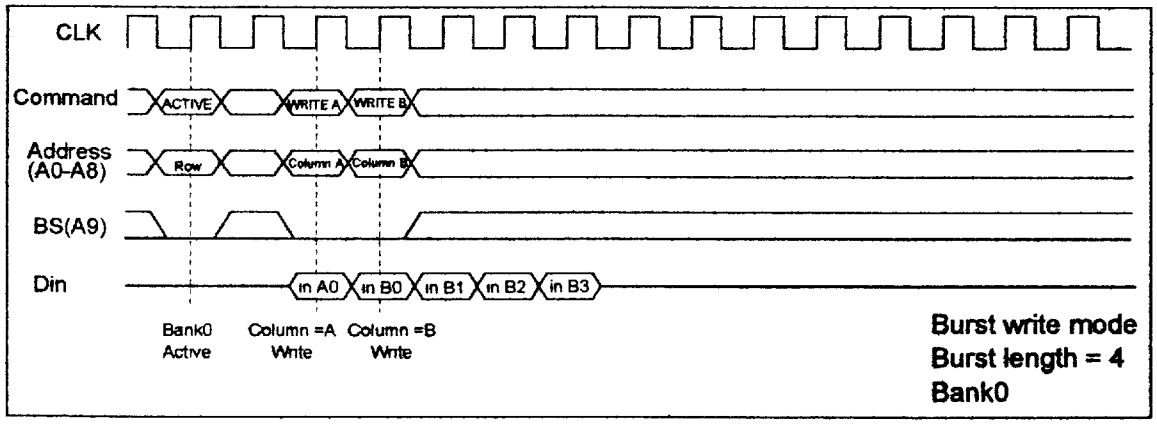
- Write command to Write command interval

1. Same bank, same ROW address:

   When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle.

   In the case of burst writes, the second write command has priority.

WRITE to WRITE Command Interval (same ROW address in same bank)



Command Intervals (cont)

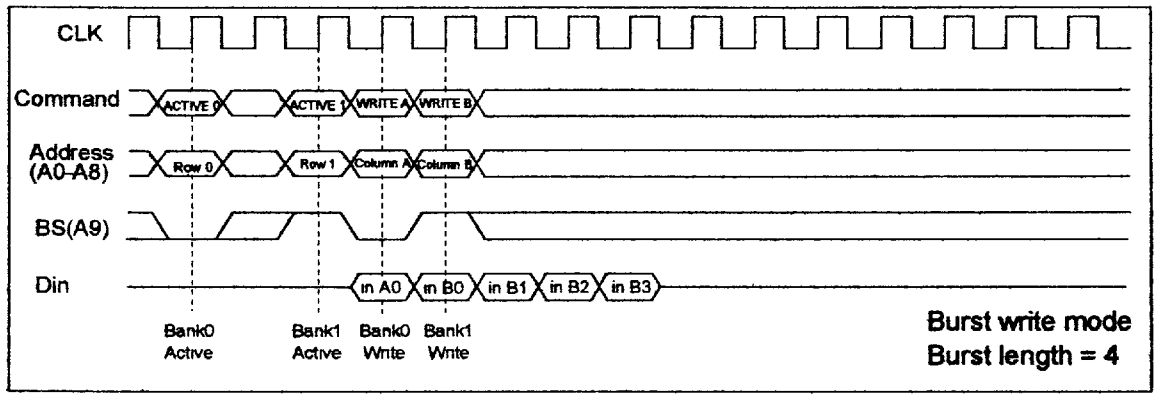
2. Same bank, different ROW address:

   When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

3. Different bank:

   When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE Command Interval (different bank)



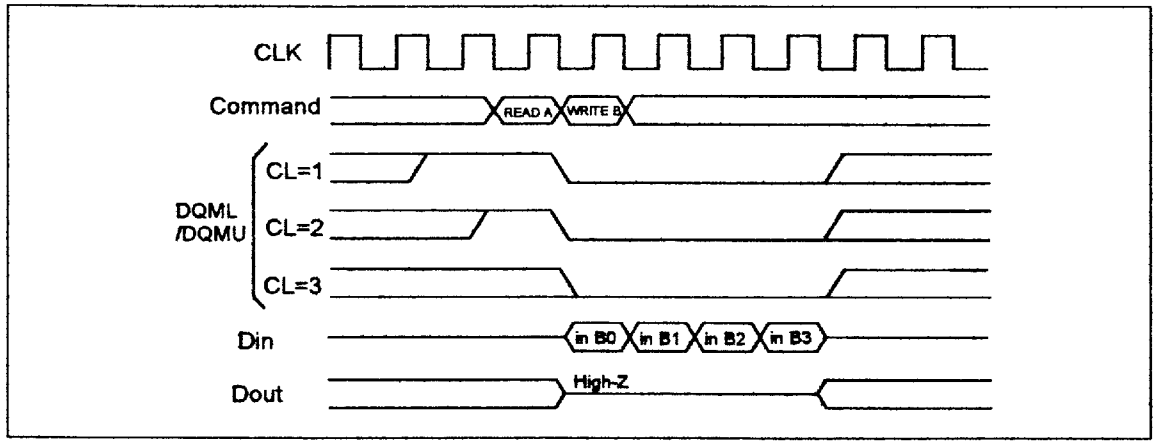
- Read command to Write command interval

1. Same bank, same ROW address:

   When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle.

   However, DQML/DQMU must be set High so that the output buffer becomes High-Z before data input.

READ to Write Command Interval



Command Intervals (cont)

2. Same bank, different ROW address:

   When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command or a bank-active command.

3. Different bank:

   When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQML/DQMU must be set High so that the output buffer becomes High-Z before data input.

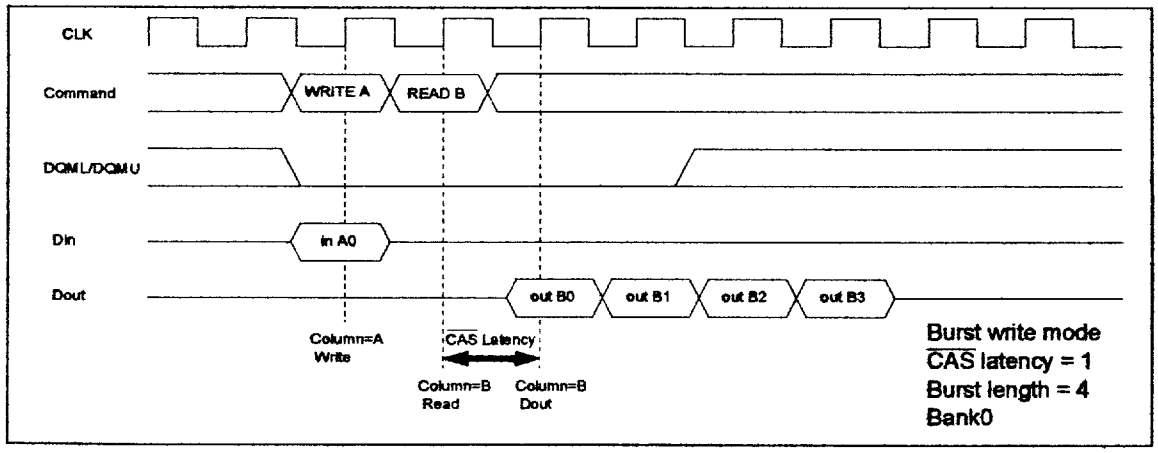
- Write command to Read command interval

1. Same bank, same ROW address:

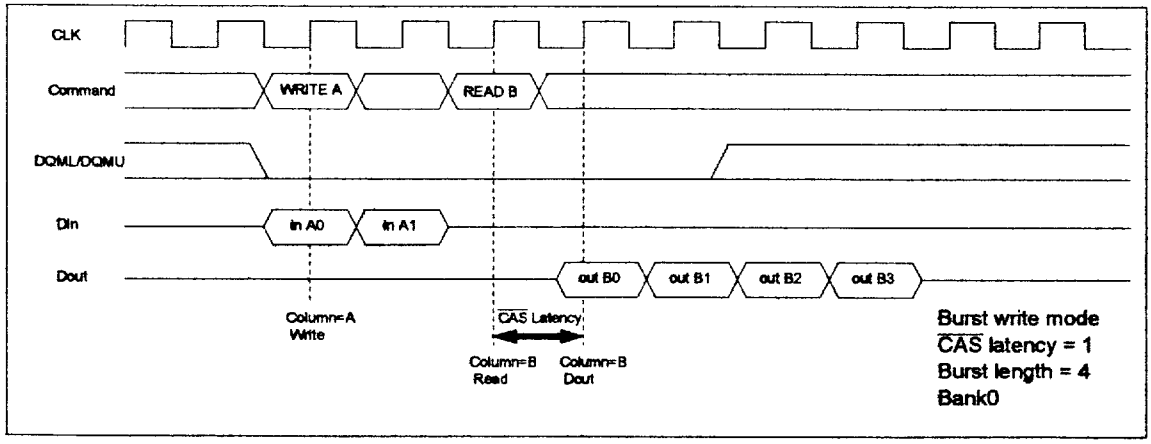
   When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle.

   However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



Command Intervals (cont)

2. Same bank, different ROW address:

   When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

3. Different bank:

   When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address).

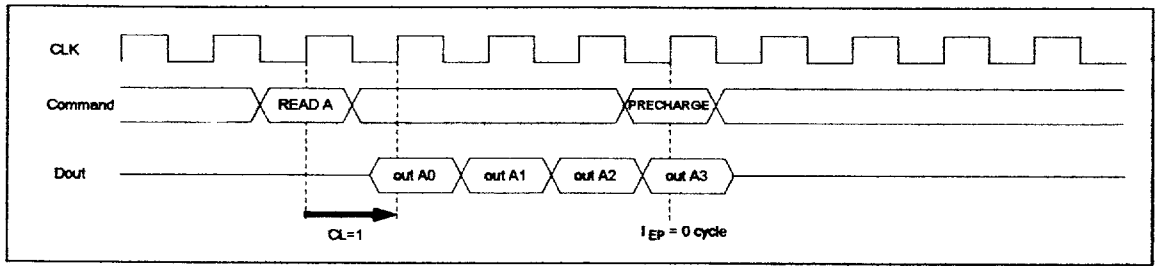
- Read command to Precharge command interval (same bank):

  When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by IHZP, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read.

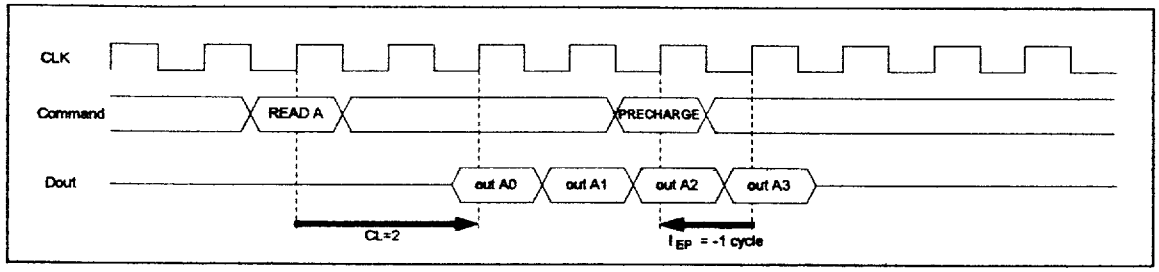
  To read all data by burst read, the cycles defined by IEP must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{CAS}$ Latency = 1, Burst Length = 4

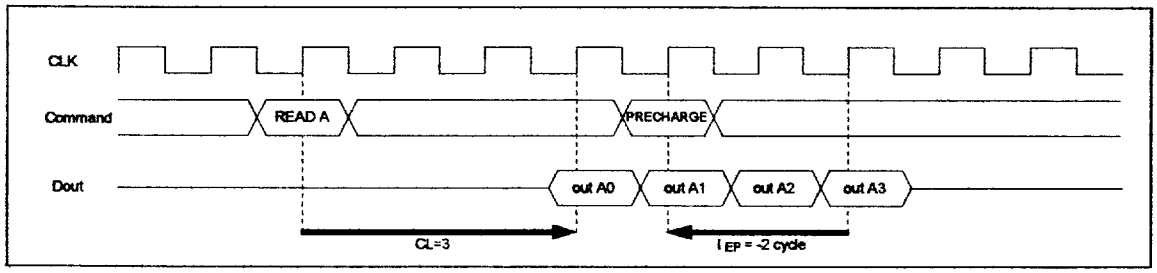


$\overline{CAS}$ Latency = 2, Burst Length = 4



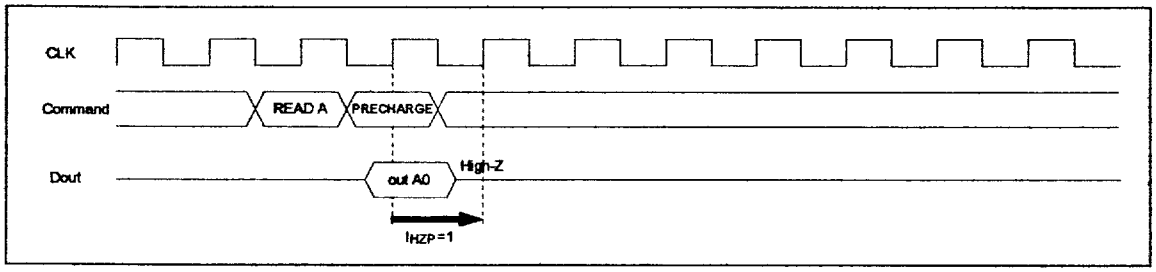
Command Intervals (cont)

$\overline{CAS}$ Latency = 3, Burst Length = 4

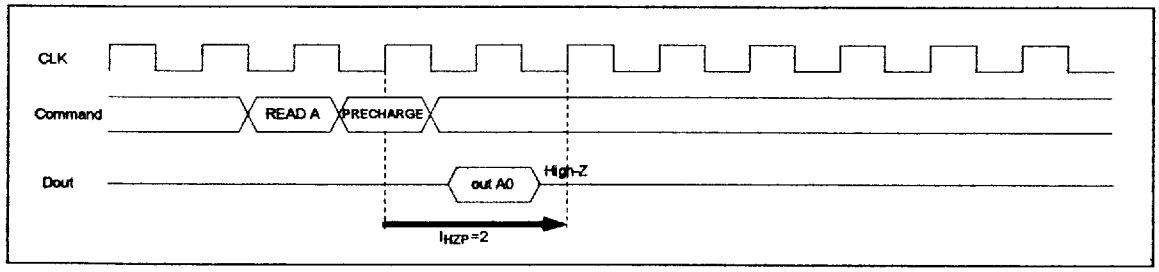


READ to PRECHARGE Command Interval (same bank): To stop output data

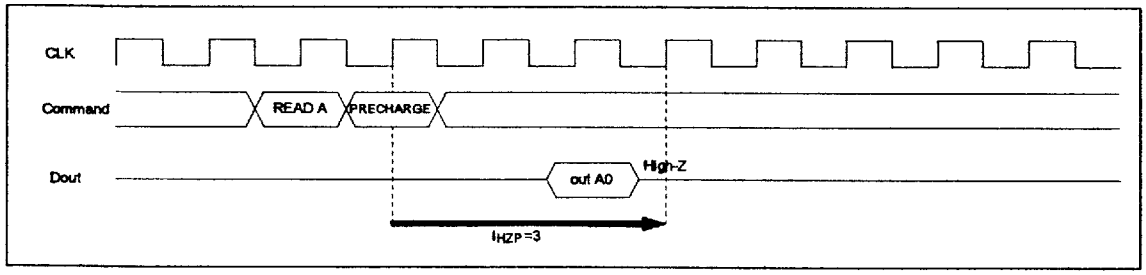
$\overline{CAS}$ Latency = 1, Burst Length = 1, 2, 4, 8



$\overline{CAS}$ Latency = 2, Burst Length = 1, 2, 4, 8



$\overline{CAS}$ Latency = 3, Burst Length = 1, 2, 4, 8



Command Intervals (cont)

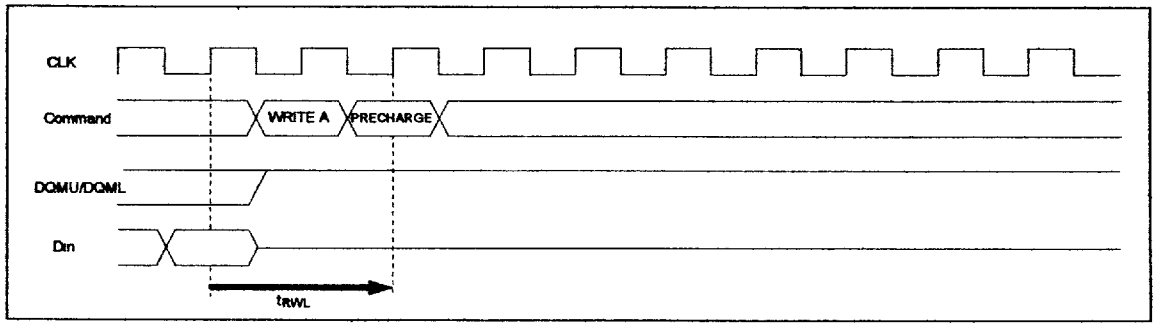
- Write command to Precharge command interval (same bank):

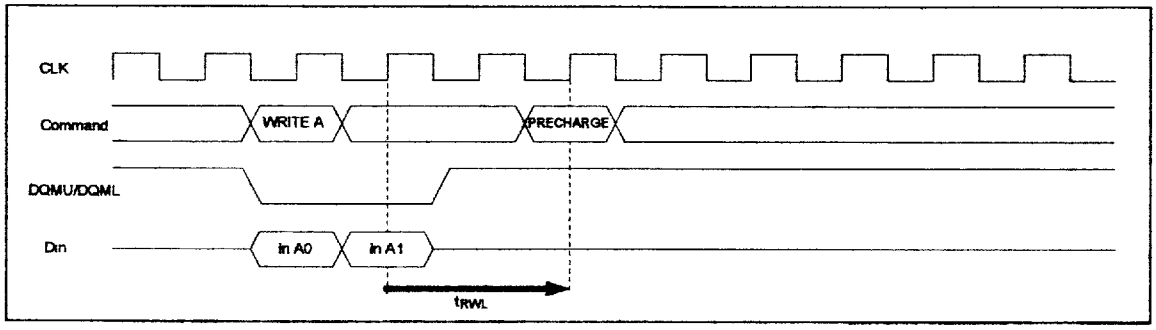
  When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle.

  However, if the burst write operation is unfinished, the input data must be masked by means of DQMU and DQML for assurance of the cycle defined by t_{RWL}.

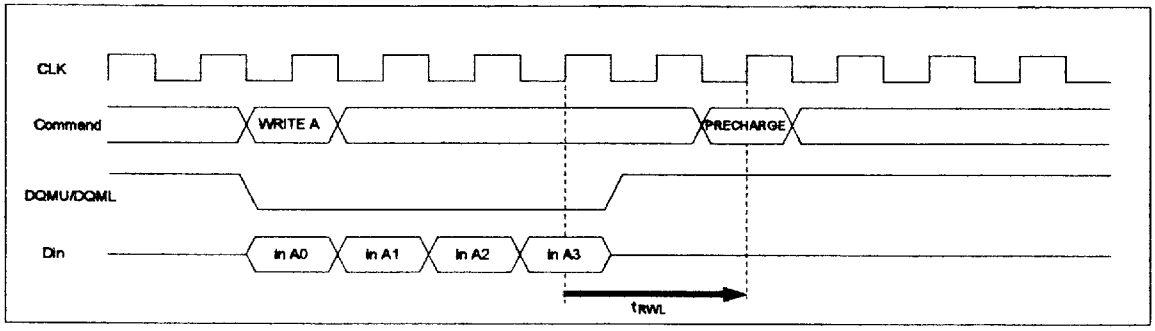
WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)





Burst Length = 4 (To write all data)



Command Intervals (cont)

- Bank active command interval

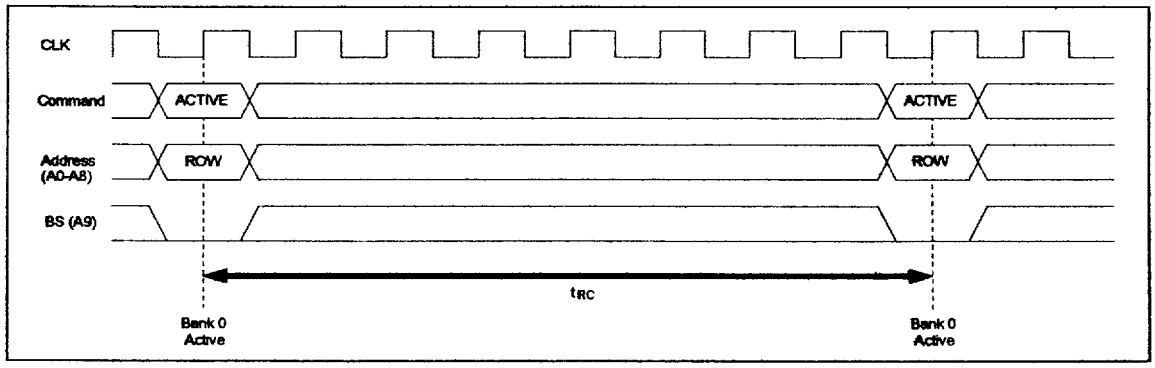
1. Same bank:

   The interval between the two bank-active commands must be no less than t_{RC}.

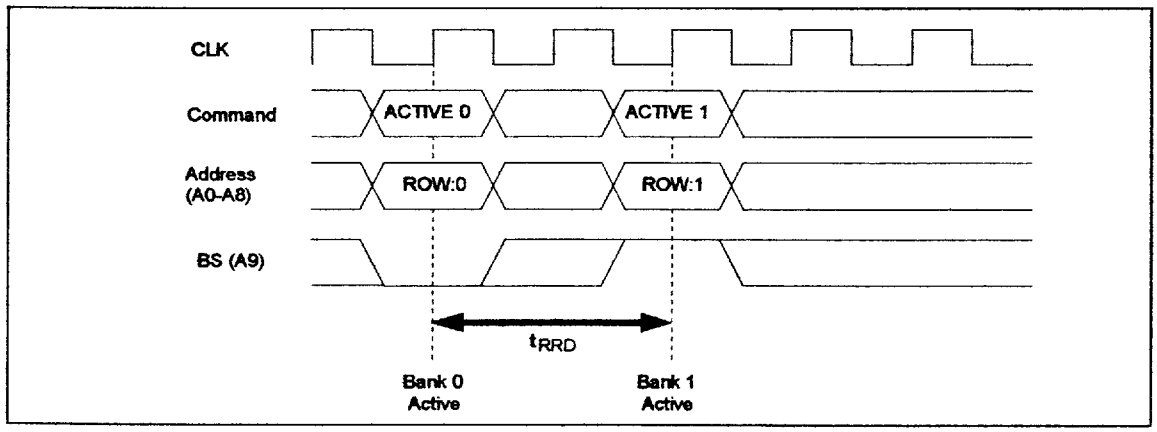
2. In the case of different bank-active commands:

   The interval between the two bank-active commands must be no less than t_{RRD}.

Bank active to bank active for same bank



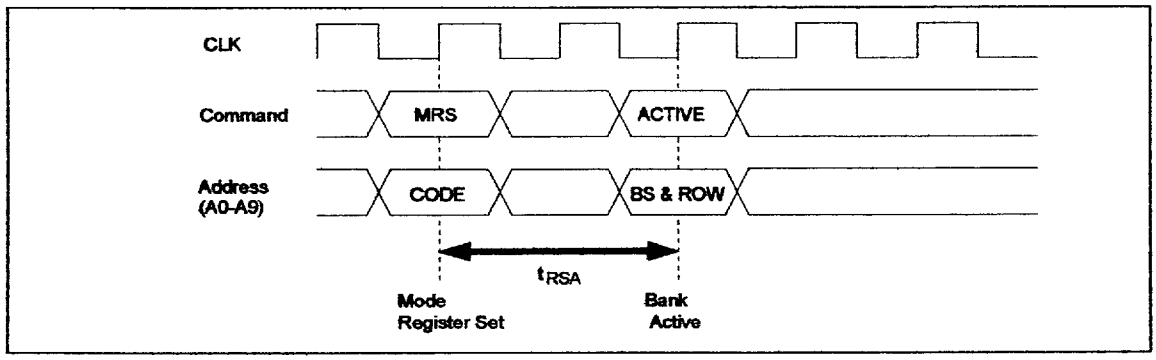
Bank active to bank active for different bank



Command Intervals (cont)

- Mode register set to Bank-active command interval:

  The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



DQM Control

The DQML and DQMU mask the lower and upper bytes of the I/O data, respectively. The timing of DQML/DQMU is different during reading and writing.

- Reading:

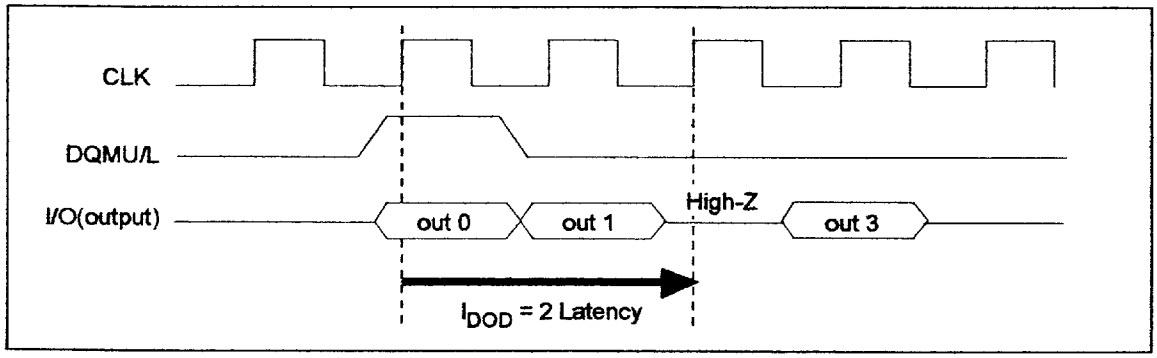
  When data is read, the output buffer can be controlled by DQML/DQMU.

  By setting DQML/DQMU to Low, the output buffer becomes Low-Z, enabling data output. By setting DQML/DQMU to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQML/DQMU during reading is 2.

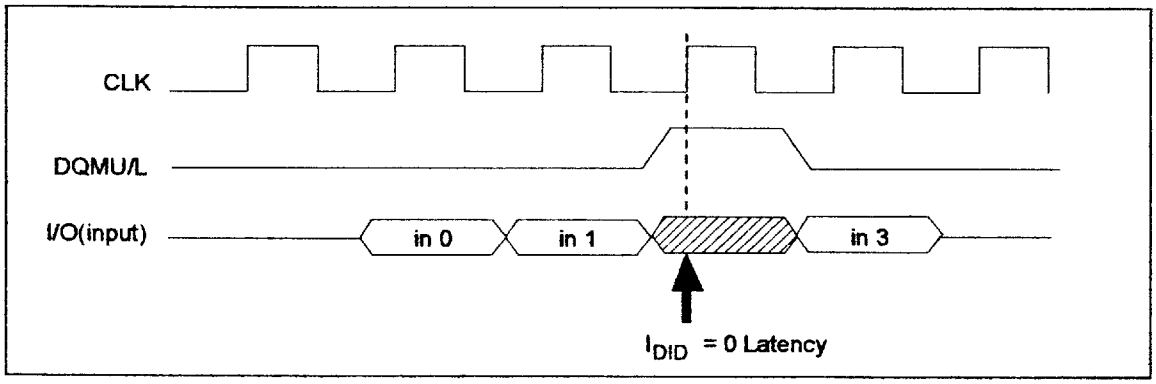
- Writing:

  Input data can be masked by DQML/DQMU. By setting DQML/DQMU to Low, data can be written. In addition, when DQML/DQMU is set to High, the corresponding data is not written, and the previous data is held. The latency of DQML/DQMU during writing is 0.

Reading



Writing



Refresh

- Auto-refresh

  All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the interval counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 1,024 cycles/16 ms. (1,024 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

- Self-refresh

  After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. After the self-refresh, since it is impossible to determine the address of the last ROW to be refreshed, an auto-refresh should immediately be performed for all addresses (1,024 cycles).

Others

- Power-down mode

  The synchronous DRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

- Clock suspend mode

  By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

- Power-up sequence

  HM5241605 series has two types of power-up sequence. Hitachi recommends that the DQML/DQMU and the CKE are set to High to ensure output to be in the high impedance and to prevent from bus contention.

1. During power-up sequence, the DQML/DQMU and the CKE must be set to High. When 100 µs has past after power on, all banks must be precharged using the precharge command. After tRP delay, set the mode register. And after tRSA delay, execute two or more cycles of auto-refresh operation as dummy, an interval of tRC is required between two auto-refresh commands.

2. During power-up sequence, the DQML/DQMU and the CKE must be set to High. When 200 µs has past after power on, all banks must be precharged using the precharge command. After tRP delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +5.5	V	1
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +4.6	V	
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. V_{IH} (max) = 5.75 V for pulse width ≤ 5 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, $V_{CC}Q$	3.0	3.6	V	1
	V_{SS}, $V_{SS}Q$	0	0	V	
Input high voltage	V_{IH}	2.0	5.5	V	1, 2
Input low voltage	V_{IL}	–0.3	0.8	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.75 V for pulse width ≤ 5 ns
3. V_{IL} (min) = –1.0 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5241605								
		-15		-17		-20				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	85	—	75	—	70	mA	Burst length=1 t_{RC} = min	1, 2, 4
Standby current	I_{CC2}	—	3	—	3	—	3	mA	CKE=V_{IL}, t_{CK} = min	5
(Bank Disable)		—	2	—	2	—	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
		—	33	—	30	—	26	mA	CKE=V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	7	—	7	—	7	mA	CKE=V_{IL}, t_{CK} = min, I/O=High-Z	1, 2
		—	34	—	31	—	26	mA	CKE=V_{IH}, NOP command t_{CK} = min, I/O = High-Z	1, 2, 3
Burst (CL=1)	I_{CC4}	—	65	—	60	—	50	mA	t_{CK} = min	1, 2, 4
operating (CL=2)		—	100	—	95	—	80	mA	BL = 4	
current (CL=3)		—	105	—	95	—	85	mA		
Auto refresh current	I_{CC5}	—	70	—	65	—	60	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	2	—	2	—	2	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	7
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	$0 \leq Vout \leq V_{CC}$ I/O = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per one CLK cycle.
5. After power down mode set, CLK operating current.
6. After power down mode set, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	—	5	pF	1, 3
Output capacitance (I/O)	C_O	—	7	pF	1, 2, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMU/L = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

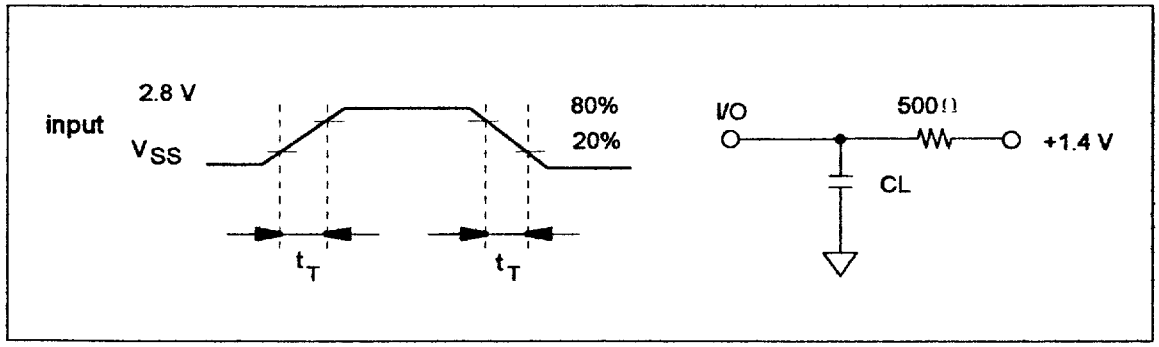
			HM5241605							
			-15		-17		-20			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock cycle time	(CL=1)	t_{CK}	30	—	35	—	40	—	ns	
	(CL=2, 3)		15	—	17.5	—	20	—	ns	1
CLK high pulse width		t_{CKH}	6	—	7	—	8	—	ns	1
CLK low pulse width		t_{CKL}	6	—	7	—	8	—	ns	1
Access time from CLK	(CL=1)	t_{AC}	—	30	—	34	—	38	ns	1, 2
	(CL=2)		—	15	—	16.5	—	18	ns	1, 2
	(CL=3)		—	13	—	15.5	—	18	ns	1, 2
Read command to data valid time	(CL=1, 2)	t_{ACK}	—	30	—	34	—	38	ns	1
	(CL=3)		—	43	—	50.5	—	58	ns	1
Data-out hold time	(CL=1)	t_{OH}	4	—	4	—	4	—	ns	1, 2
	(CL=2, 3)		2	—	2	—	2	—	ns	
CLK to Data-out low impedance		t_{LZ}	0	—	0	—	0	—	ns	1, 2
CLK to Data-out high impedance	(CL=1)	t_{HZ}	4	15	4	17	4	19	ns	
	(CL=2, 3)		2	10	2	12	2	14	ns	1, 3
Data-in setup time		t_{DS}	4	—	4	—	4	—	ns	1
Data in hold time		t_{DH}	2	—	2	—	2	—	ns	1
Address setup time		t_{AS}	4	—	4	—	4	—	ns	1
Address hold time		t_{AH}	2	—	2	—	2	—	ns	1
CKE setup time		t_{CES}	4	—	4	—	4	—	ns	1
CKE setup time for power down exit		t_{CESP}	13	—	15	—	17	—	ns	1
CKE hold time		t_{CEH}	2	—	2	—	2	—	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	4	—	4	—	4	—	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	2	—	2	—	2	—	ns	1
Ref/Active to Ref/Active command period		t_{RC}	110	—	120	—	130	—	ns	1

AC Characteristics (Ta = 0 to 70 °C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V) (cont)

		HM5241605							
		-15		-17		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Active to Precharge command period	t_{RAS}	70	10000	75	10000	80	10000	ns	1
Active to precharge on full page mode	t_{RASC}	—	80000	—	80000	—	80000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	35	—	40	—	ns	1
Precharge to active command period	t_{RP}	34	—	34	—	40	—	ns	1
The last data-in to Precharge lead time	t_{RWL}	30	—	35	—	40	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	30	—	35	—	40	—	ns	1
Register set to active command	t_{RSA}	30	—	35	—	40	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is CL = 50 pF with current source.
3. t_{HZ} (max) defines the time at which the outputs achieves ± 200 mV.
Load condition is CL = 5 pF with current source.
4. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

HM5241605 (LVTTL)



Relationship Between Frequency and Minimum Latency

Parameter	Symbol	HM5241605 -15		HM5241605 -17		HM5241605 -20		Notes
Frequency (MHz)		66	33	57	28.5	50	25	
t_{CK} (ns)		15	30	17.5	35	20	40	
Active command to column command (same bank)	t_{RCD}	2	1	2	1	2	1	
Active command to active command (same bank)	t_{RC}	8	5	7	4	7	4	= [t_{RAS} + t_{RP}]
Active command to precharge command (same bank)	t_{RAS}	5	3	5	3	4	2	
Precharge command to active command (same bank)	t_{RP}	3	2	2	1	2	1	
Last data input to precharge command (same bank)	t_{RWL}	2	1	2	1	2	1	
Active command to active command (different bank)	t_{RRD}	2	1	2	1	2	1	
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	4	2	4	2	= [t_{RWL} + t_{RP}]
Self refresh exit to command input	l_{SEC}	8	4	7	4	7	4	= [t_{RC}]
Precharge command to high impedance	l_{HZP}							
($\overline{CAS}$ latency = 3)		3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)		2	2	2	2	2	2	
($\overline{CAS}$ latency = 1)		—	1	—	1	—	1	
Last data out to active command	l_{APR}							
(auto precharge) ($\overline{CAS}$ latency = 2, 3)		2	1	1	0	1	0	= [t_{RP}] – 1
(same bank) ($\overline{CAS}$ latency = 1)		—	2	—	1	—	1	= [t_{RP}]
Last data out to precharge	l_{EP}							
(early precharge) ($\overline{CAS}$ latency = 3)		–2	–2	–2	–2	–2	–2	
($\overline{CAS}$ latency = 2)		–1	–1	–1	–1	–1	–1	
($\overline{CAS}$ latency = 1)		—	0	—	0	—	0	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable	l_{CLE}	1	1	1	1	1	1	
Register set to active command	t_{RSA}	2	1	2	1	2	1	
CS to command disable	l_{CDD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	l_{BSR}							
($\overline{CAS}$ latency = 1)		—	0	—	0	—	0	
($\overline{CAS}$ latency = 2)		1	1	1	1	1	1	
($\overline{CAS}$ latency = 3)		2	2	2	2	2	2	

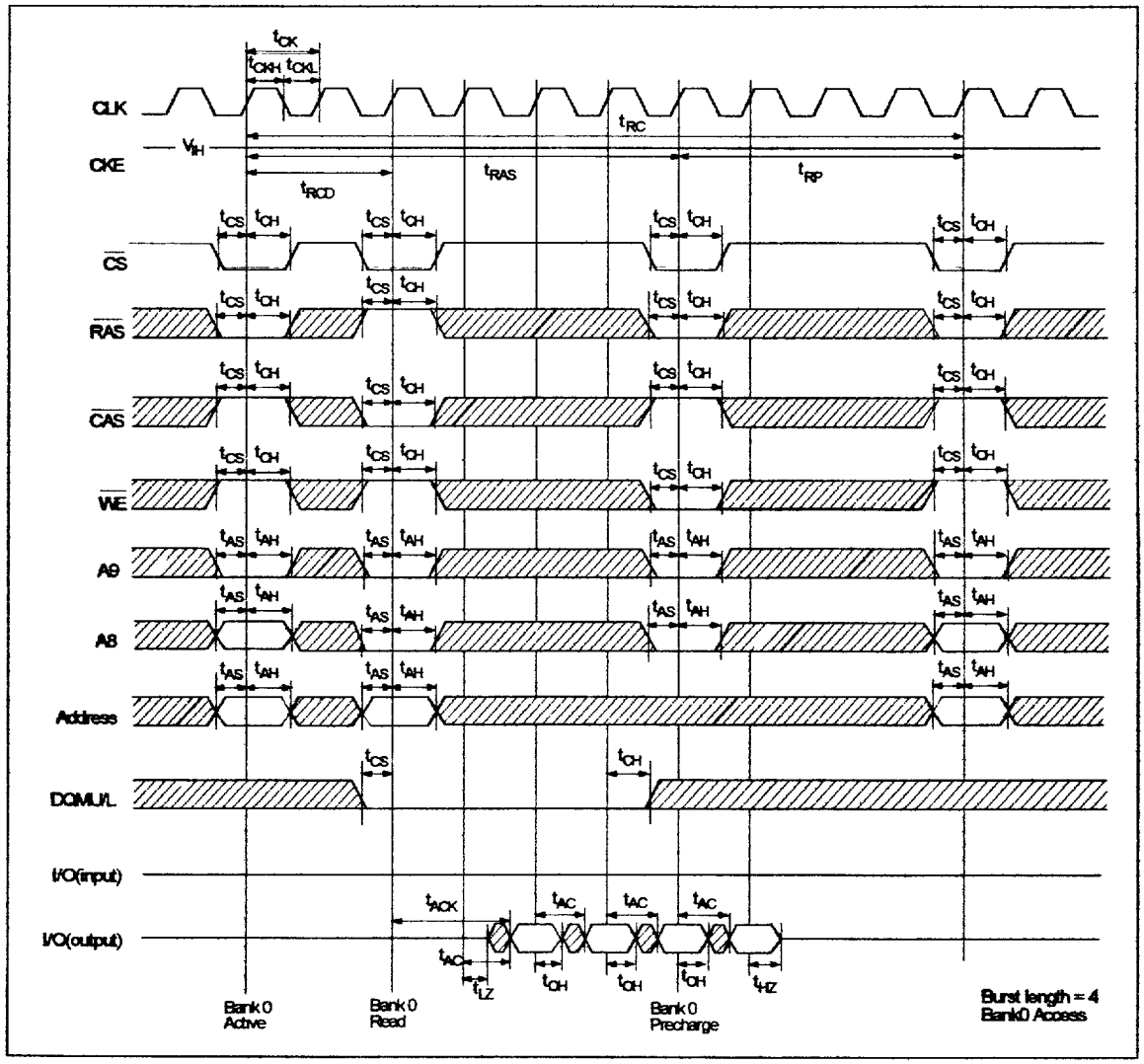
Relationship Between Frequency and Minimum Latency (cont)

Parameter		HM5241605						
		-15		-17		-20		
Frequency (MHz)		66	33	57	28.5	50	25	
t_{CK} (ns)	Symbol	15	30	17.5	35	20	40	Notes
Burst stop to output high impedance	I_{BSH}							
($\overline{CAS}$ latency = 1)		—	1	—	1	—	1	
($\overline{CAS}$ latency = 2)		2	2	2	2	2	2	
($\overline{CAS}$ latency = 3)		3	3	3	3	3	3	
Burst stop to write data ignore	I_{BSW}	1	1	1	1	1	1	

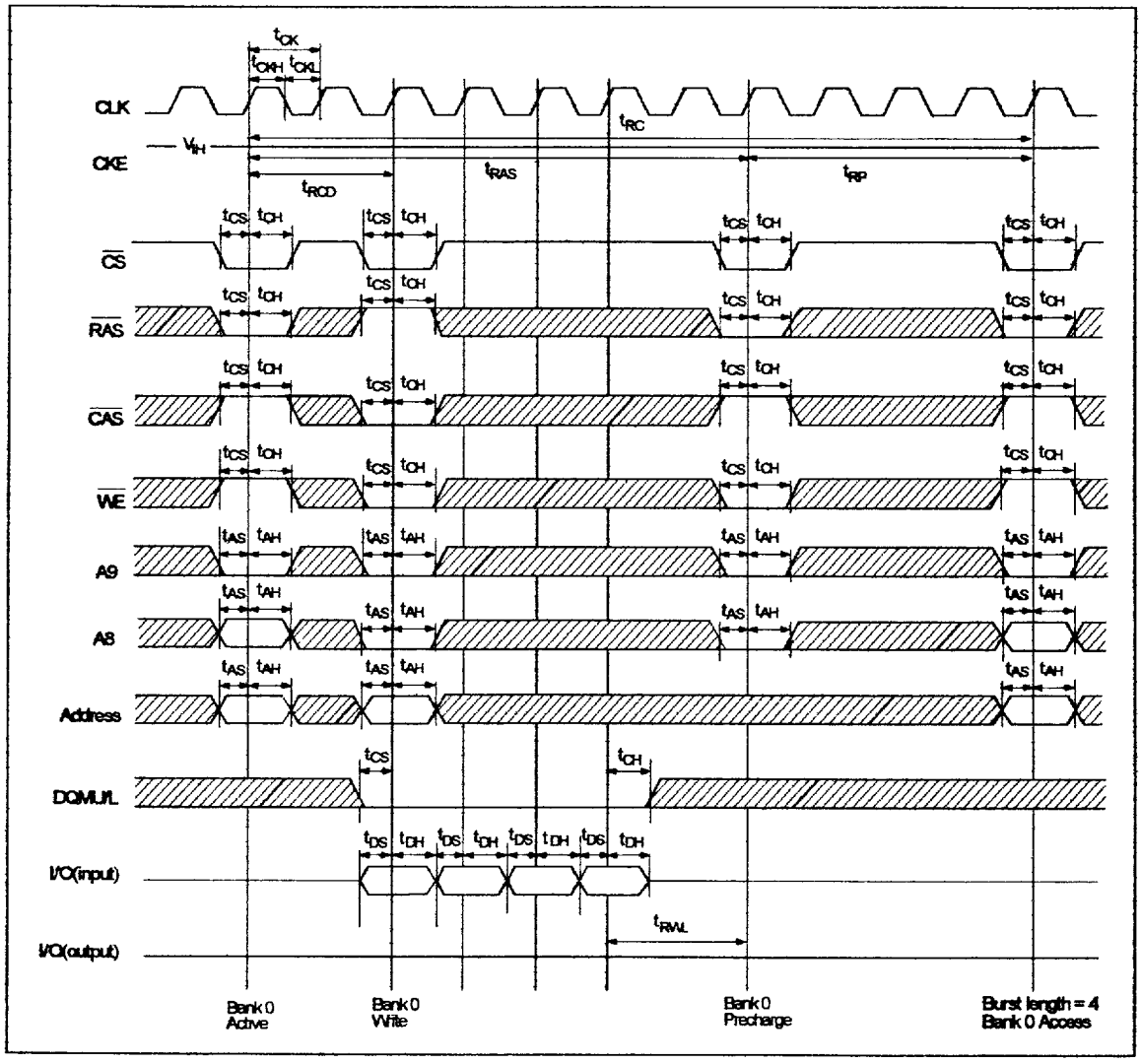
Note: 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ latency.

Timing Waveforms

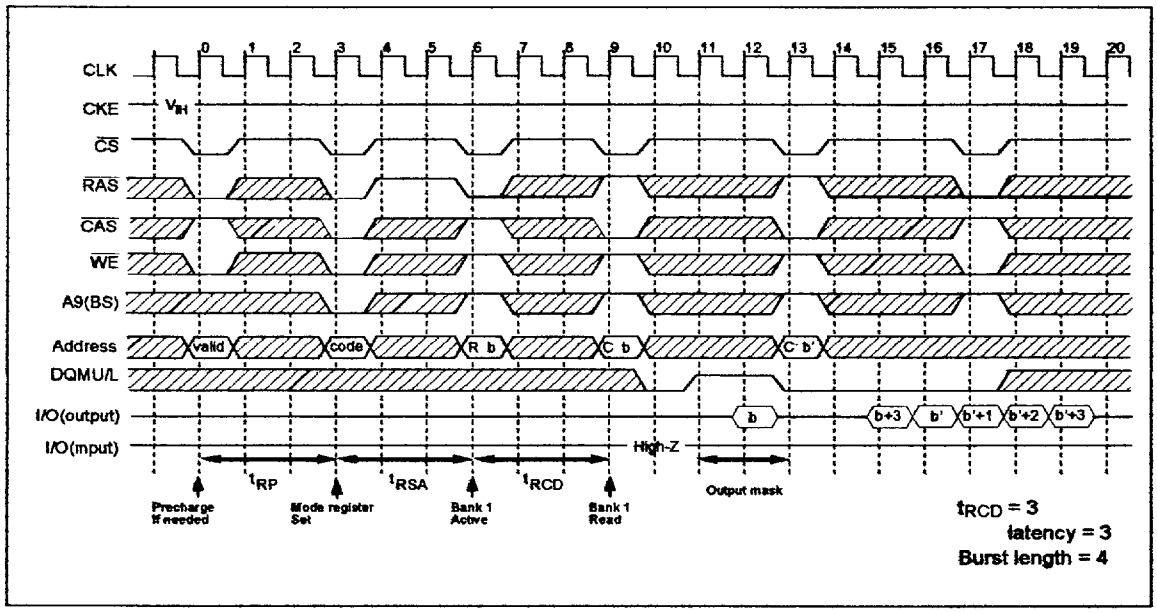
Read Cycle



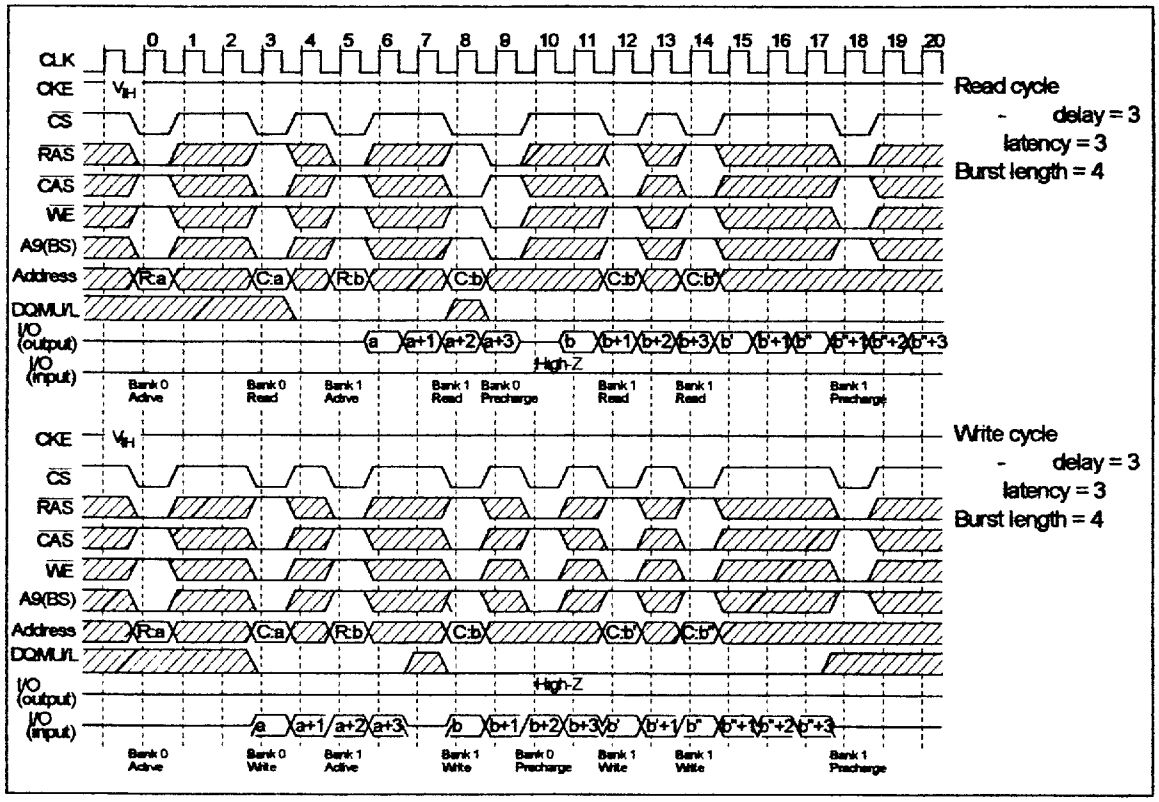
Write Cycle



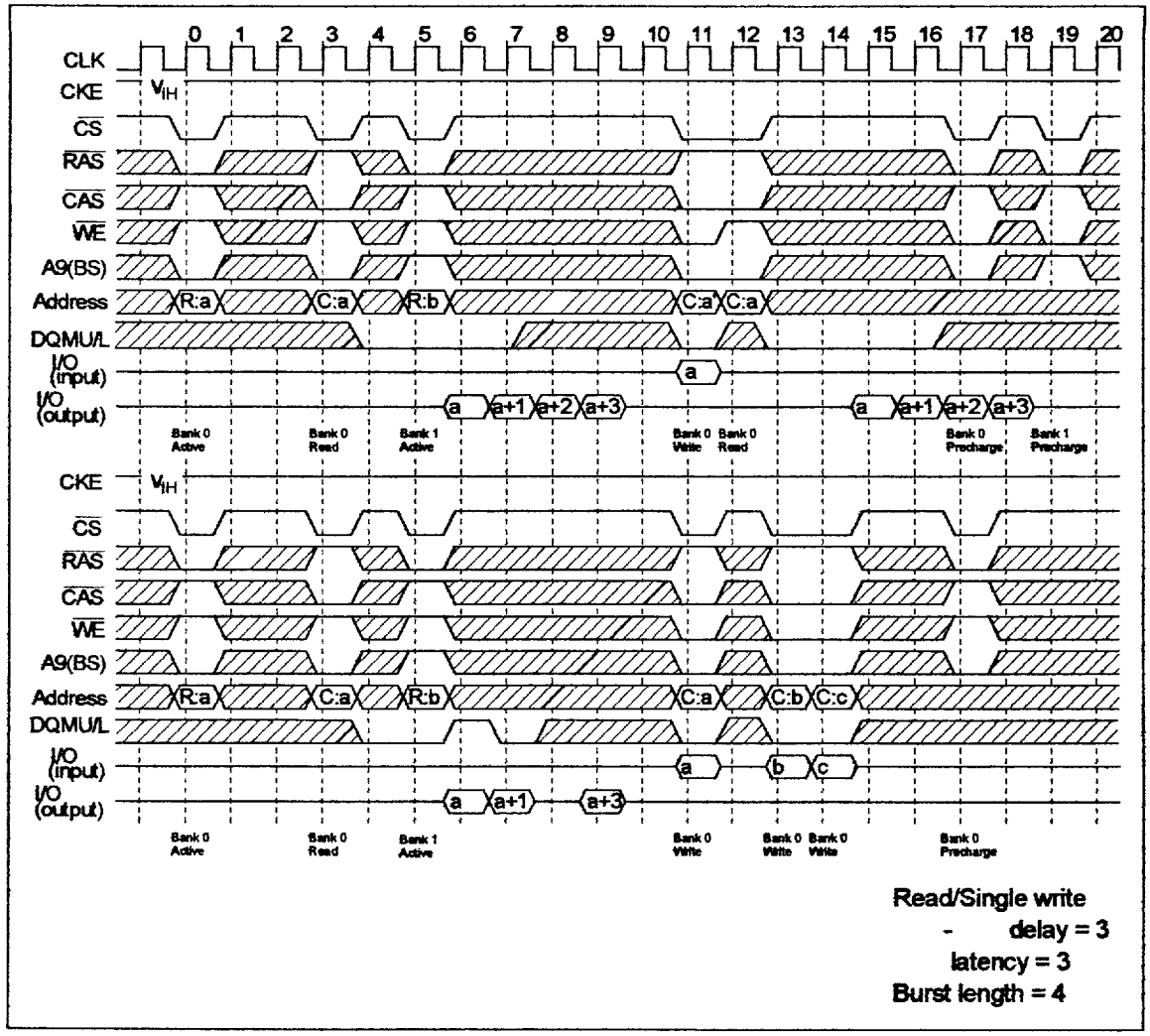
Mode Register Set Cycle



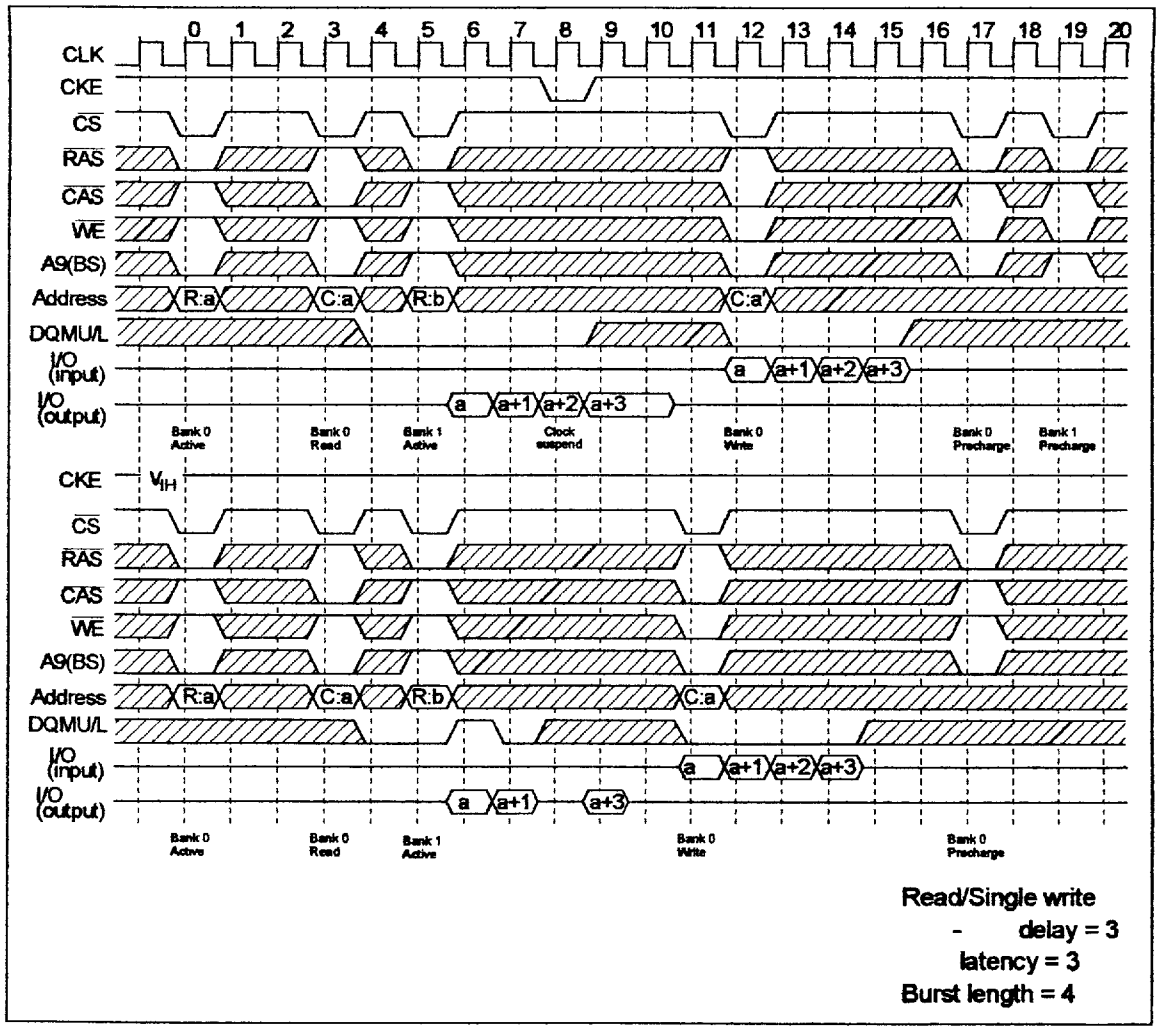
Read Cycle/Write Cycle



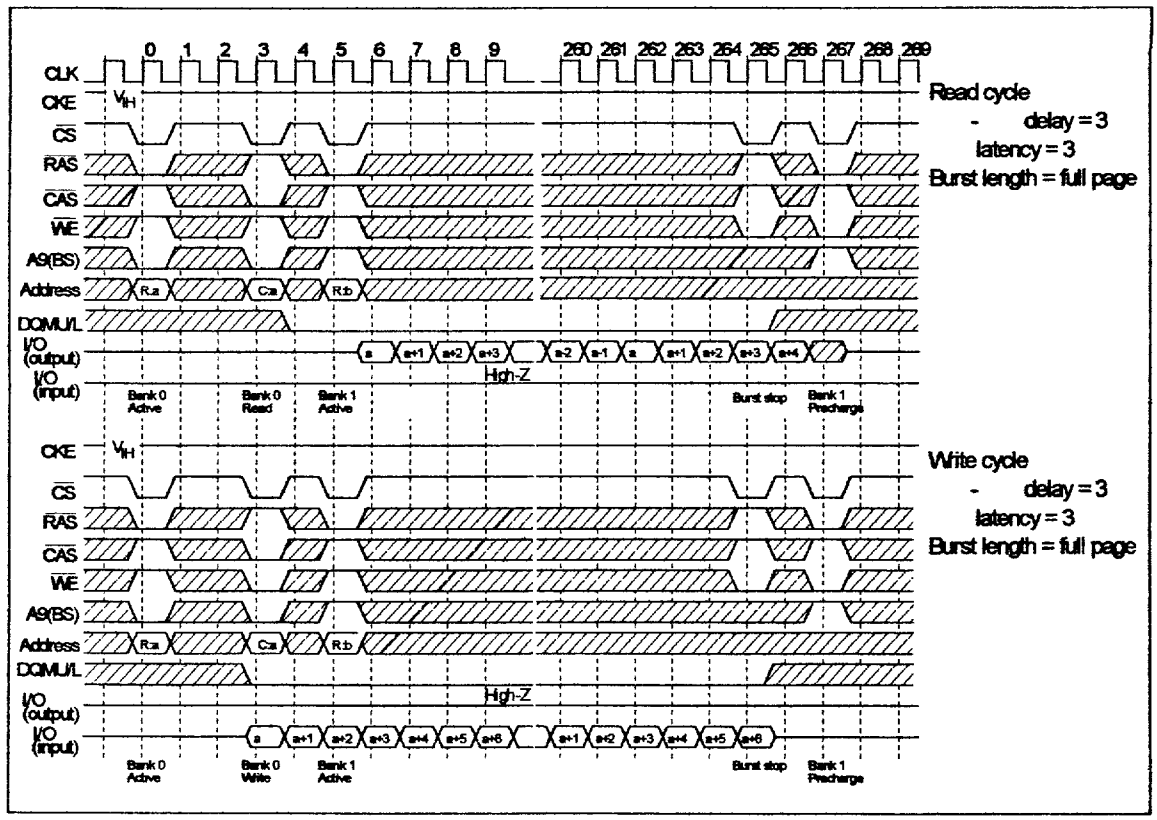
Read/Single Write Cycle



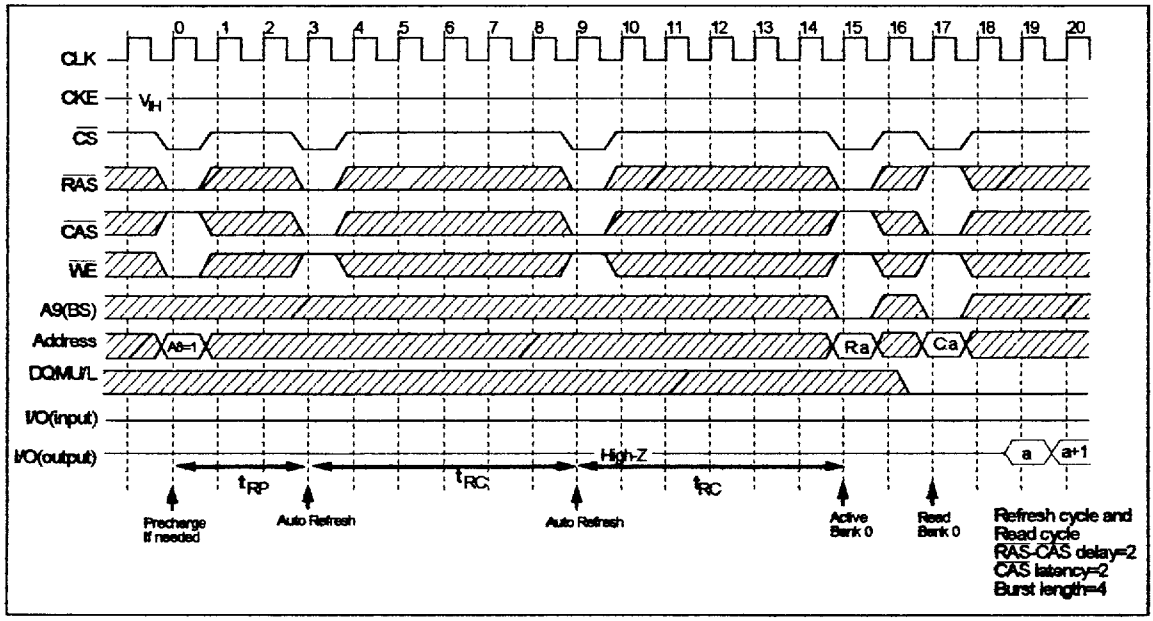
Read/Burst Write Cycle



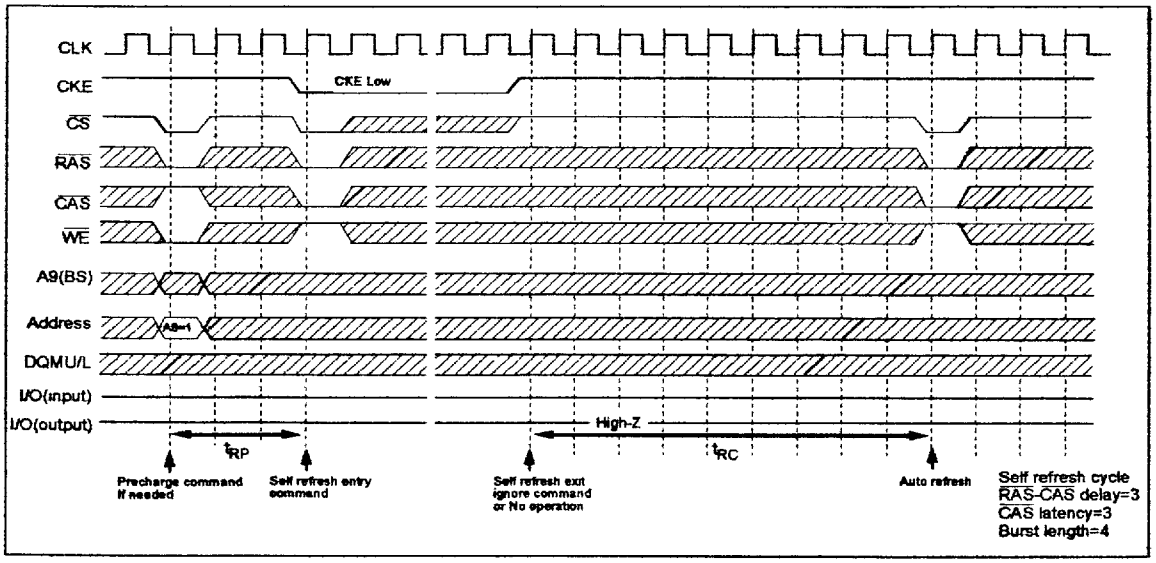
Full Page Read/Write Cycle



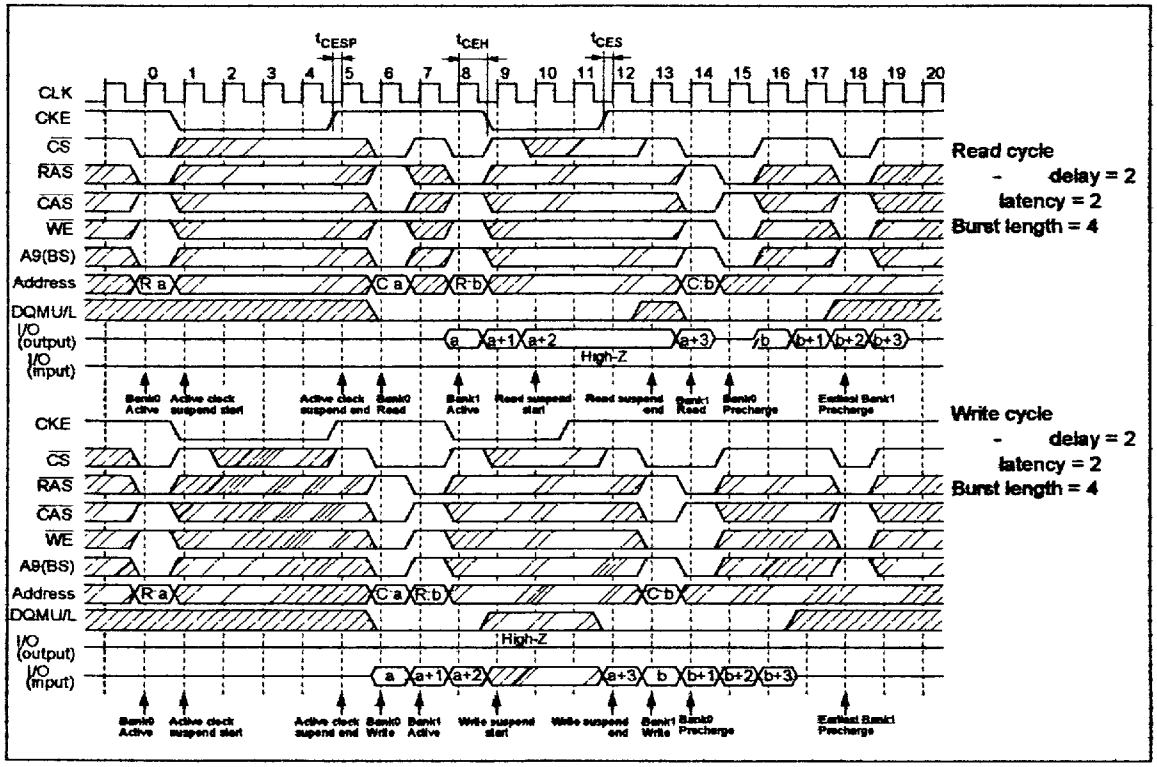
Auto Refresh Cycle



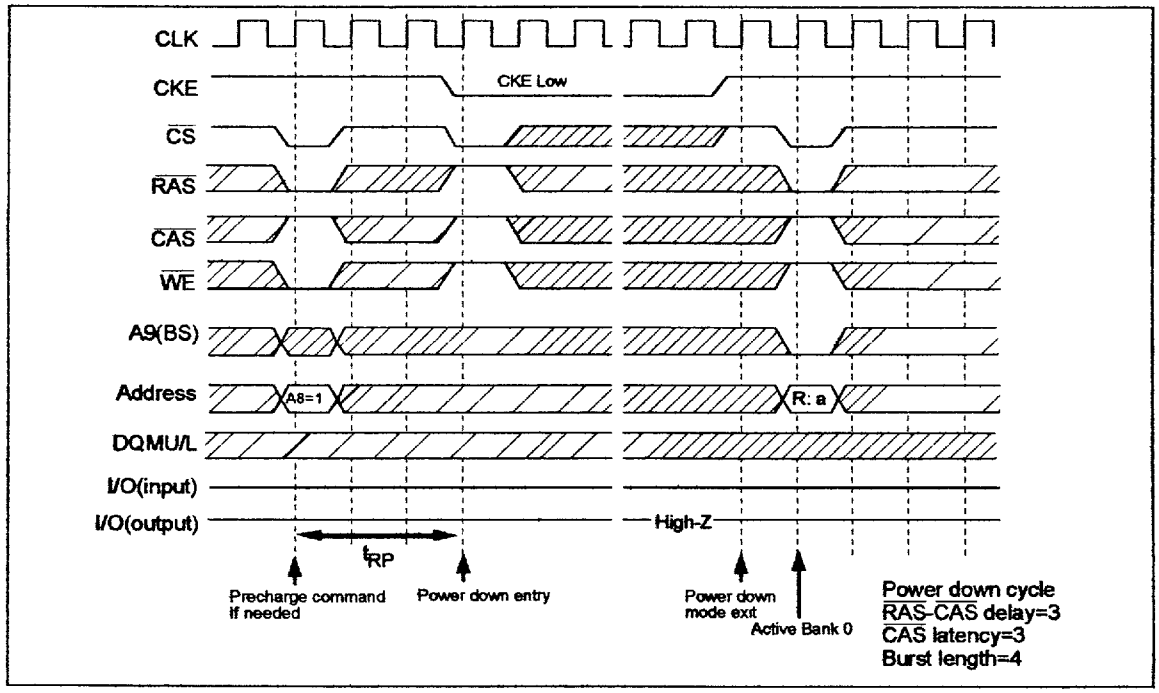
Self Refresh Cycle



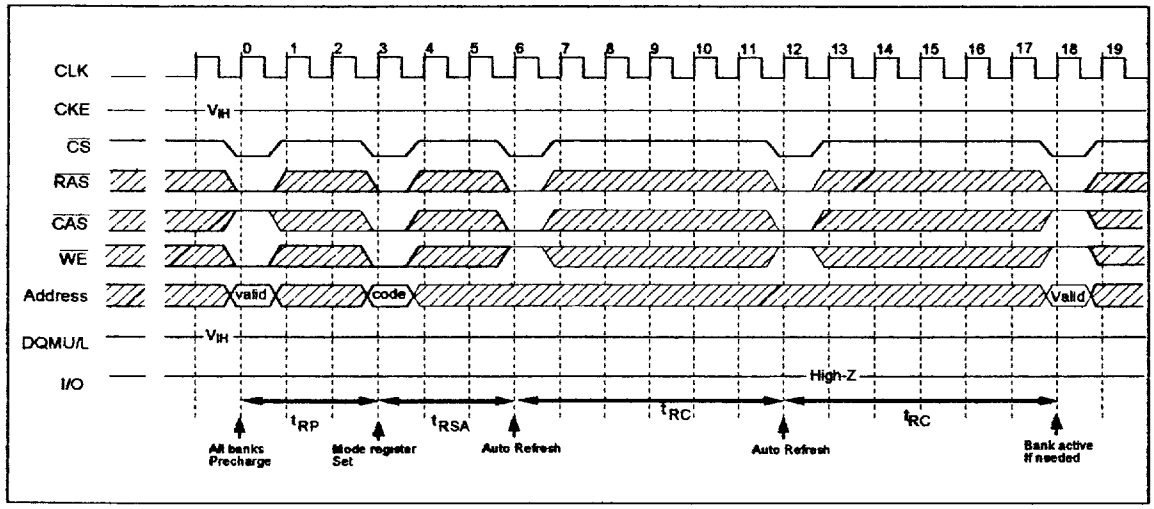
Clock Suspend Mode



Power Down Mode



Power Up Sequence (1)



Power Up Sequence (2)