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# HM5283206 Series

8M LVTTTL interface SGRAM  
125 MHz/100 MHz/83 MHz  
128-kword × 32-bit × 2-bank

# HITACHI

ADE-203-223F (Z)  
Rev. 6.0  
Oct. 2, 1998

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## Description

All inputs and outputs signals refers to the rising edge of the clock input. The HM5283206 provides 2 banks to realize better performance. 8 column block write function and write per bit function are provided for graphic applications.

## Features

- 3.3V Power supply
- Clock frequency: 125 MHz/100 MHz/83 MHz (max)
- LVTTTL interface
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length: 1/2/4/8/full page
- 2 variations of burst sequence
  - Sequential (BL = 1/2/4/8/full page)
  - Interleave (BL = 1/2/4/8)
- Programmable  $\overline{\text{CAS}}$  latency: 1/2/3
- Byte control by DQM
- 8 column block write function with column address mask
- Write per bit function (old mask)
- Refresh cycles: 1024 refresh cycle/16 ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh

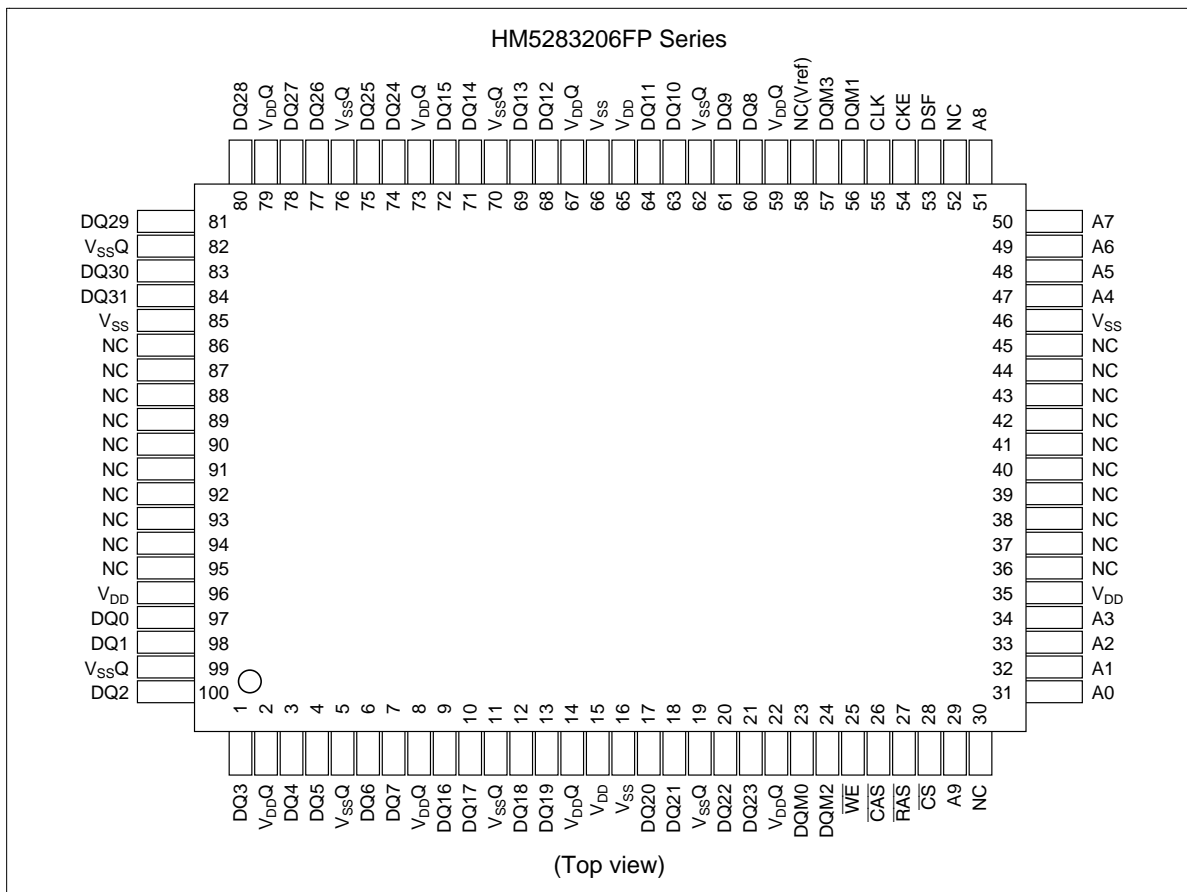
## HM5283206 Series

### Ordering Information

Type No.	Frequency	Package
HM5283206FP-8* <sup>1</sup>	125 MHz* <sup>1</sup>	100-pin plastic QFP (FP-100J)
HM5283206FP-10	100 MHz	
HM5283206FP-12	83 MHz	

Note: 1. Under development

### Pin Arrangement

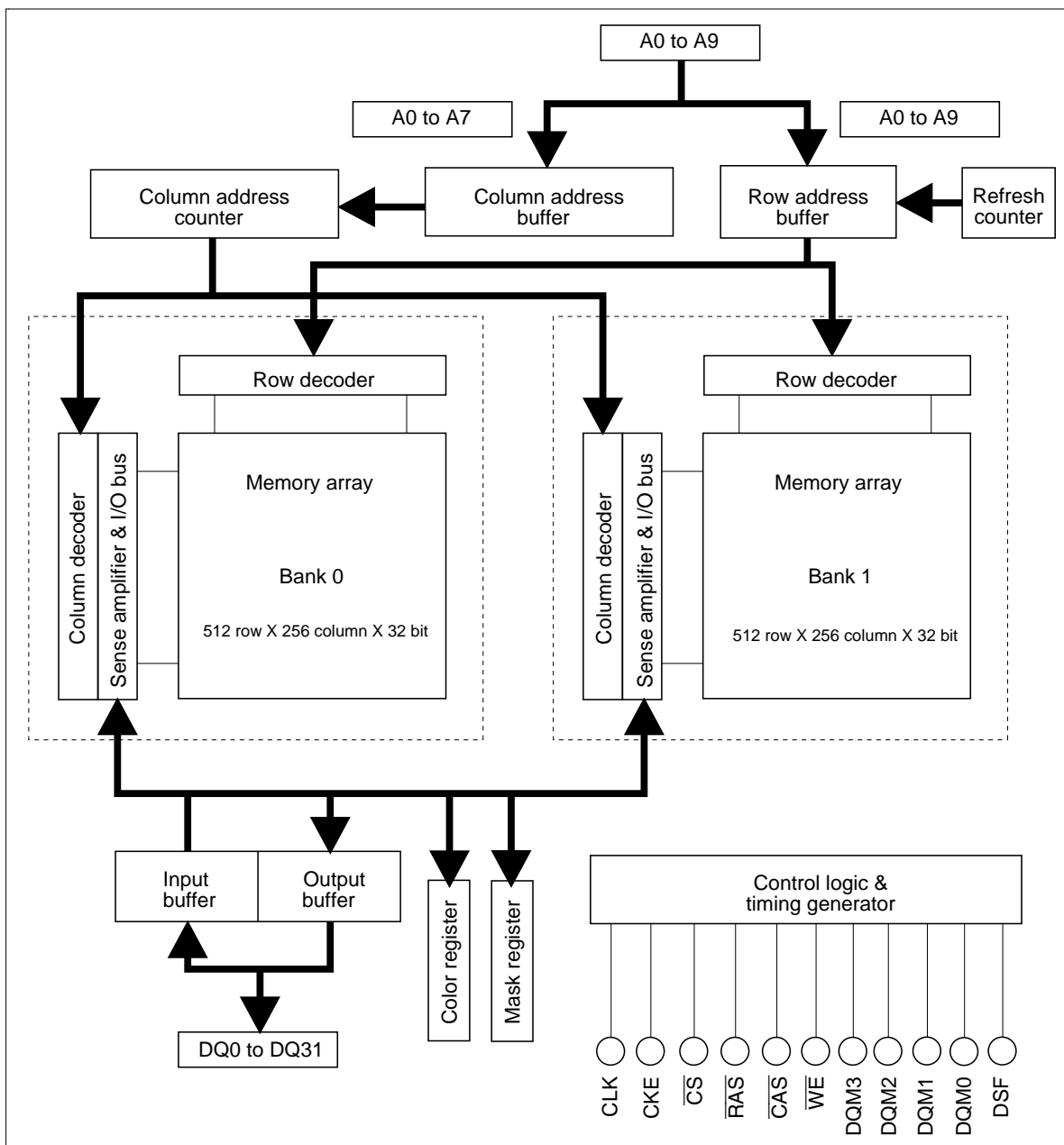


**Pin Description**

Pin name	Function
A0 to A9	Address input Row address     A0 to A8 Column address A0 to A7 Bank select address (BS) A9
DQ0 to DQ31	Data-input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{RAS}}$	Row address asserted bank enable
$\overline{\text{CAS}}$	Column address asserted
$\overline{\text{WE}}$	Write enable
DQM0 to DQM3	Byte input/output mask
CLK	Clock input
CKE	Clock enable
$V_{\text{DD}}$	Power for internal circuit
$V_{\text{SS}}$	Ground for internal circuit
$V_{\text{DDQ}}$	Power for DQ internal circuit
$V_{\text{SSQ}}$	Ground for DQ internal circuit
DSF	Special function input flag
NC	No connection

# HM5283206 Series

## Block Diagram



## **Pin Functions**

**CLK (input pin):** CLK is the master clock input pin. The other input signals are referred at CLK rising edge.

**$\overline{\text{CS}}$  (input pin):** When  $\overline{\text{CS}}$  is Low, the command input cycle becomes valid. When  $\overline{\text{CS}}$  is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

**$\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and  $\overline{\text{WE}}$  (input pins):** These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

**DSF (input pin):** DSF is a part of inputs of graphic commands of the HM5283206. If DSF is LOW, the HM5283206 operates as standard synchronous DRAM.

**A0 to A8 (input pins):** Row address (AX0 to AX8) is determined by A0 to A8 pins at the CLK rising edge when a bank active command is input. Column address (AY0 to AY7) is determined by levels on A0 to A7 pins at the CLK rising edge when a read or write command is input. A8 determines precharge mode. When A8 is low, only the bank selected by A9 (BS) is precharged by a precharge command. When A8 is high, both banks are precharged by a precharge command.

**A9 (input pin):** A9 is the bank select signal (BS). The memory array of the HM5283206 is divided into the bank 0 and the bank 1, both contain 512 row  $\times$  256 column  $\times$  32 bits. If A9 is Low, the bank 0 is selected, and if A9 is High, the bank 1 is selected.

**CKE (input pin):** By referring low level on CKE pin, HM5283206 determines to go into clock suspend modes or power down modes. In self refresh mode, low level on this pin is also referred to turn on refresh process.

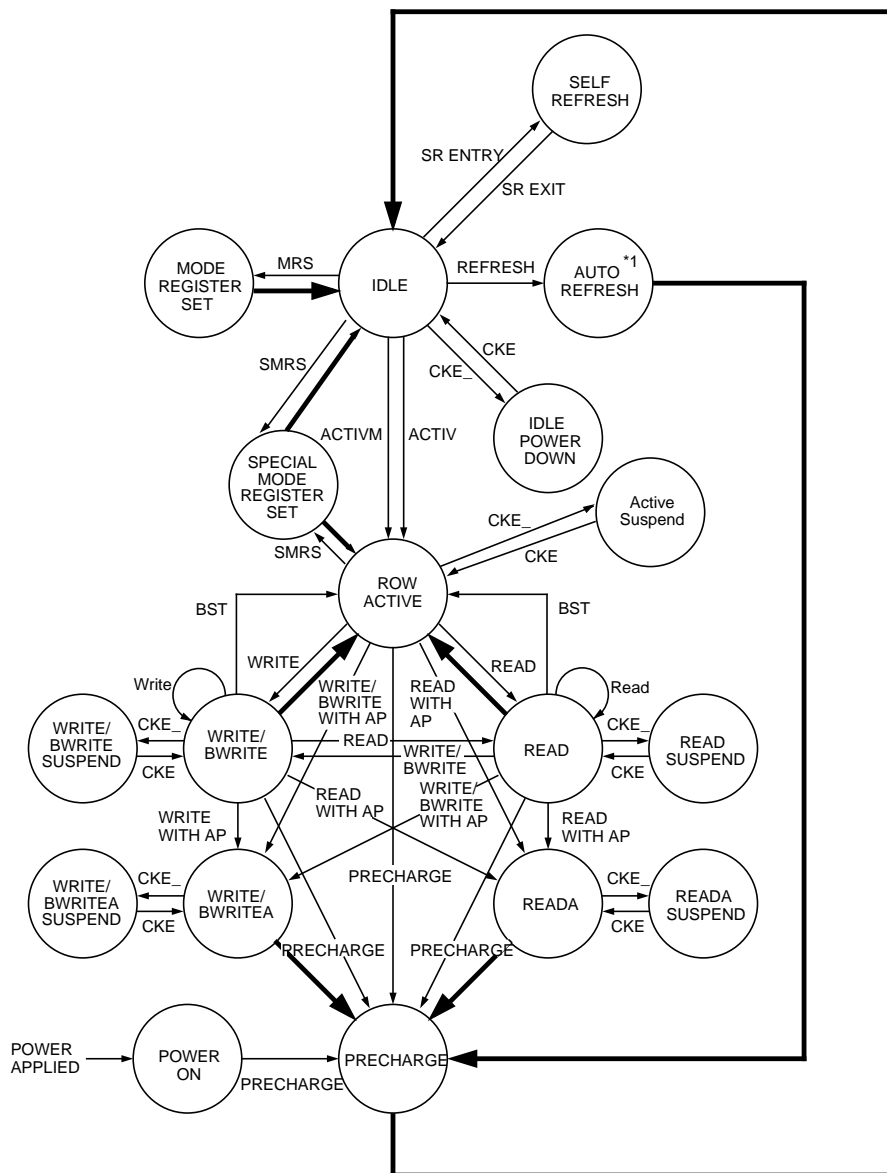
**DQM0, DQM1, DQM2 and DQM3 (input pins):** DQM0 applies to DQ0 to DQ7. DQM1 applies to DQ8 to DQ15. DQM2 applies to DQ16 to DQ23. DQM3 applies to DQ24 to DQ31. In read mode, referring high level on DQM pins, HM5283206 floats related DQ pins. In write mode, referring high level on DQM pins, HM5283206 ignores input data through related DQ pins.

**DQ0 to DQ31 (input/output):** These are the data line for the HM5283206.

**$V_{\text{DD}}$  and  $V_{\text{DDQ}}$  (power supply pins):** 3.3 V is applied. ( $V_{\text{DD}}$  is for the internal circuit and  $V_{\text{DDQ}}$  is power supply pin for DQ output buffer.)

**$V_{\text{SS}}$  and  $V_{\text{SSQ}}$  (power supply pins):** Ground is connected. ( $V_{\text{SS}}$  is for the internal circuit and  $V_{\text{SSQ}}$  is for DQ output buffer.)

## Simplified State Diagram



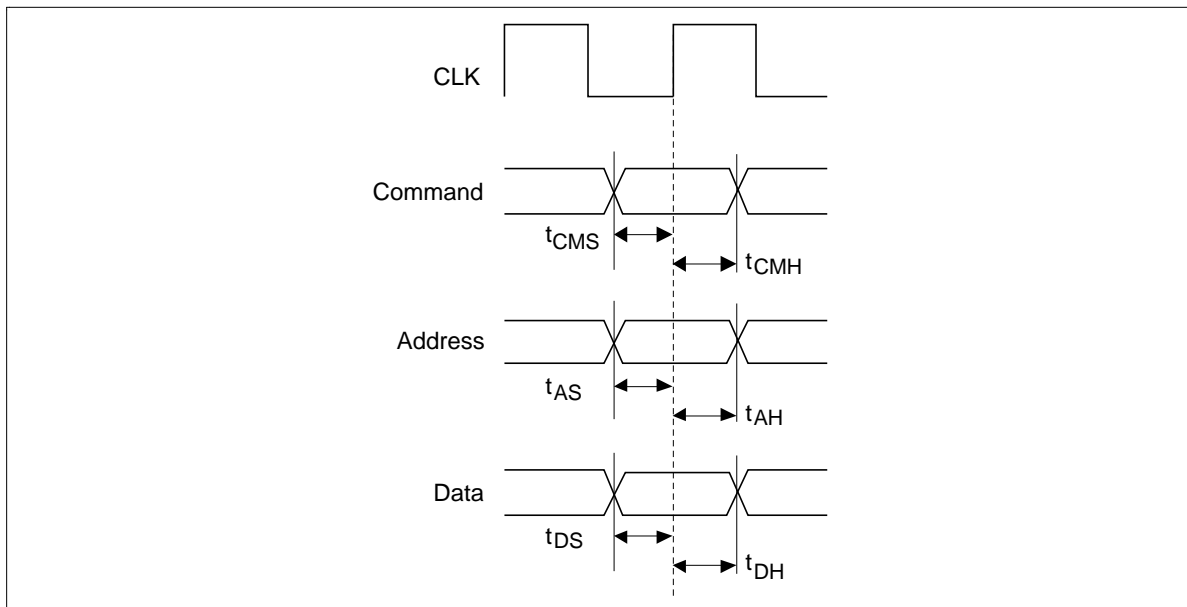
## Commands Operation

### Commands Explanation

Every operations of HM5283206 are executed by input commands. A command is input, at the rising edge of CLK, by setting the levels on  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ , A8 (auto precharge) and DSF pins, HIGH ( $V_{\text{IH}}$ ) or LOW ( $V_{\text{IL}}$ ).

Note: The setup and hold condition should be obeyed when command, address or data is input.

### Setup and Hold Condition of Command, Address and Data Input



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## HM5283206 Series

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**Precharge command [PRE, PALL]:** At the CLK rising edge, by setting

$\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{WE}}$ , DSF are LOW,  
 $\overline{\text{CAS}}$  is HIGH

bank can be precharged to idle state.

A8 = LOW: the bank selected by A9 is precharged.

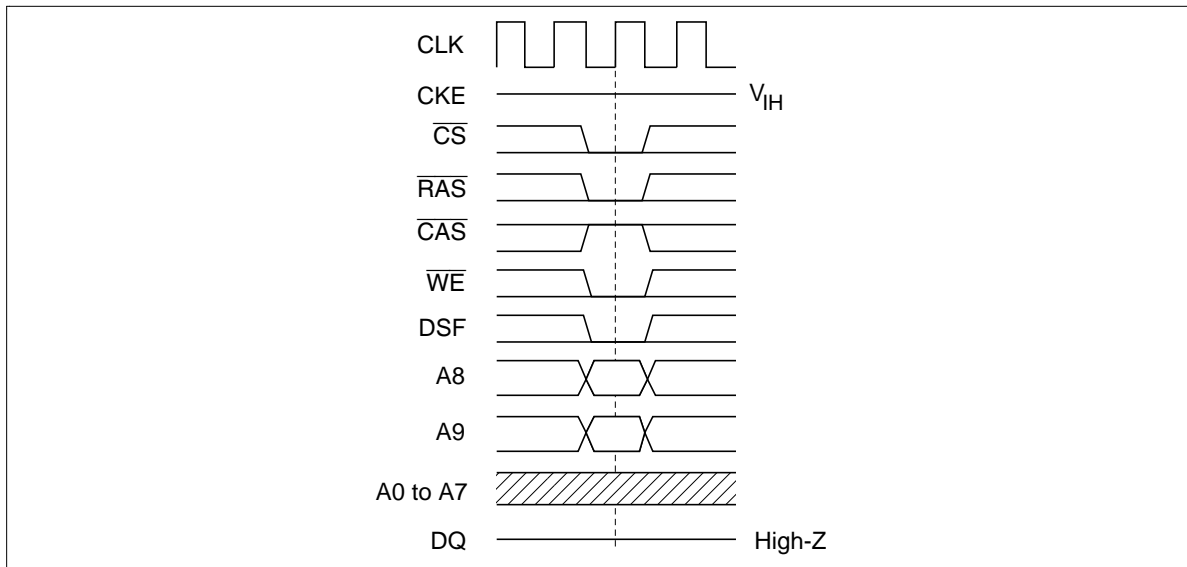
A8 = HIGH: both banks are precharged.

[State transition]

power on — (precharge) -> Idle

Row active — (precharge) -> Idle

### Precharge Command



**Mode register set command [MRS]:** If both banks have been precharged or are in idle state, at the CLK rising edge, by setting

$\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ , DSF; LOW

an internal register (the mode register; MRS) are set.

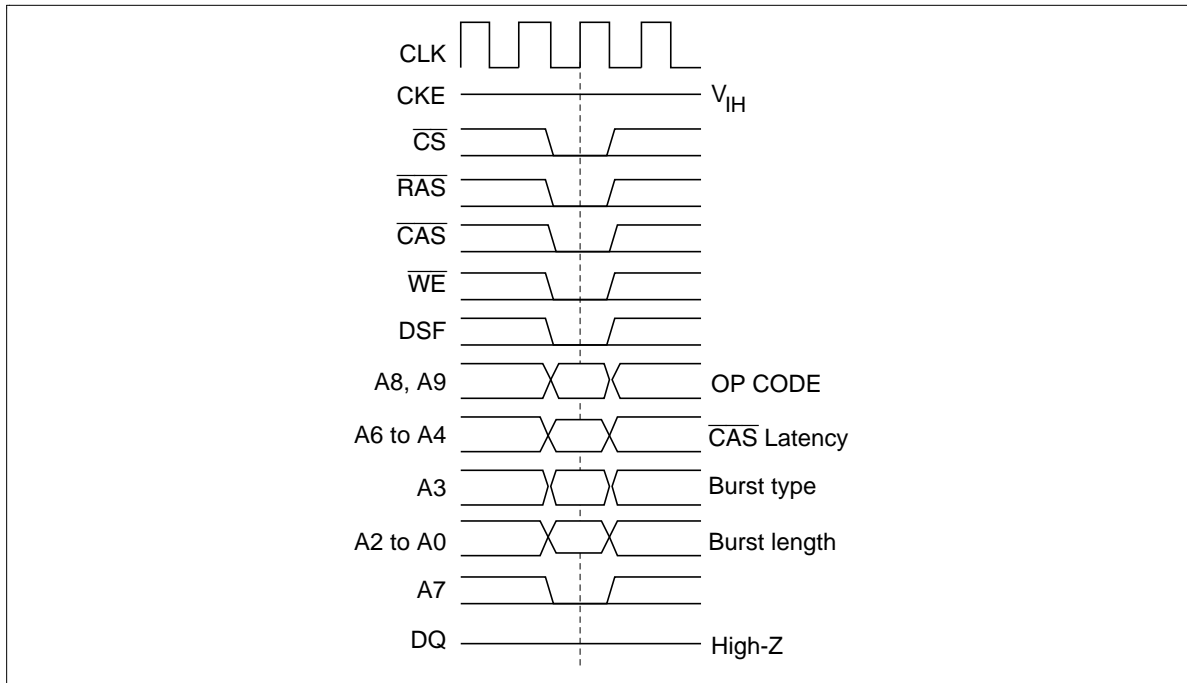
The data through address pins, at the cycle when this command is input, are stored in the mode register.

A8, A9 bits determine burst write or single write. A6 to A4 bits determine  $\overline{\text{CAS}}$  latency. A3 bit determines burst type, sequential or interleave. A2 to A0 bits determine burst length. A7 bit should be set to low. See table below for details.

[State transition]

Idle — (Mode register set) -> Idle

### Mode Register Set Command



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### Mode Register Configuration

A9	A8	Operation CODE
0	0	Burst read and burst write
0	1	R
1	0	Burst read and single write
1	1	R

A6	A5	A4	CAS latency
0	0	0	R
0	0	1	1
0	1	0	2
0	1	1	3
1	×	×	R

A3	Burst type
0	Sequential
1	Interleave

A2	A1	A0	Burst length	
			BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	Full page	R

Note: R: Reserved

**Bank and row active command [ACTV, ACTVM]:** If a bank has been precharged or is in idle state. At the CLK rising edge, by setting

$\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ; LOW,

$\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ : HIGH

a row of the bank is activated. The bank is selected by setting the level on A9 pin HIGH (bank 1) or LOW (bank 0) at this timing. A0 to A8 determine the row address.

[Option]

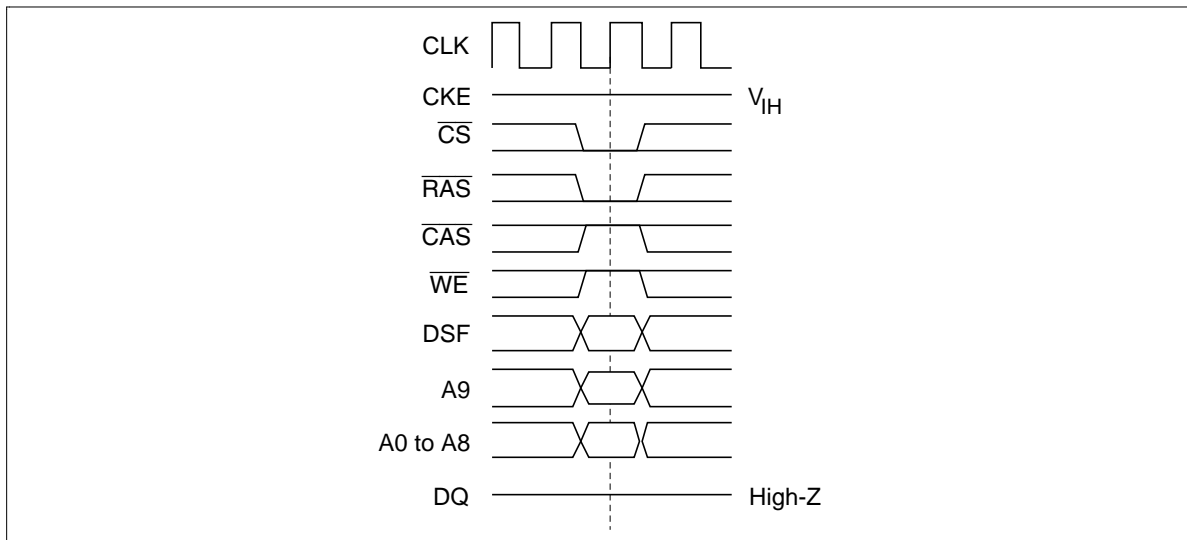
DSF = LOW; write per bit function disable (ACTV)

DSF = HIGH; write per bit function enable (ACTVM)

[State transition]

Idle — (row active) -> Row active

### Bank and Row Active Command



## HM5283206 Series

**Column address and read command:** For a row of one of two banks activated by ACTV or ACTVM, at the CLK rising edge, by setting  $\overline{\text{CS}}$ ,  $\overline{\text{CAS}}$ , DSF; LOW,  $\overline{\text{RAS}}$ ,  $\overline{\text{WE}}$ ; HIGH, data is output through DQ pins.

A9 determines the bank address.

A0 to A7 determine the column address.

$\overline{\text{CAS}}$  latency stored in MRS determines the timing when data are driven.

In case, CL ( $\overline{\text{CAS}}$  latency) = 1, 1 clock cycle after the command input, data start to be output.

In case CL = 2, 2 clock cycle after the command input, data start to be output.

In case CL = 3, 3 clock cycle after the command input, data start to be output.

Burst Length (BL) stored in MRS determines data length of output.

[Option]

A8 = HIGH; auto precharge mode or execute precharge automatically after finishing data output.

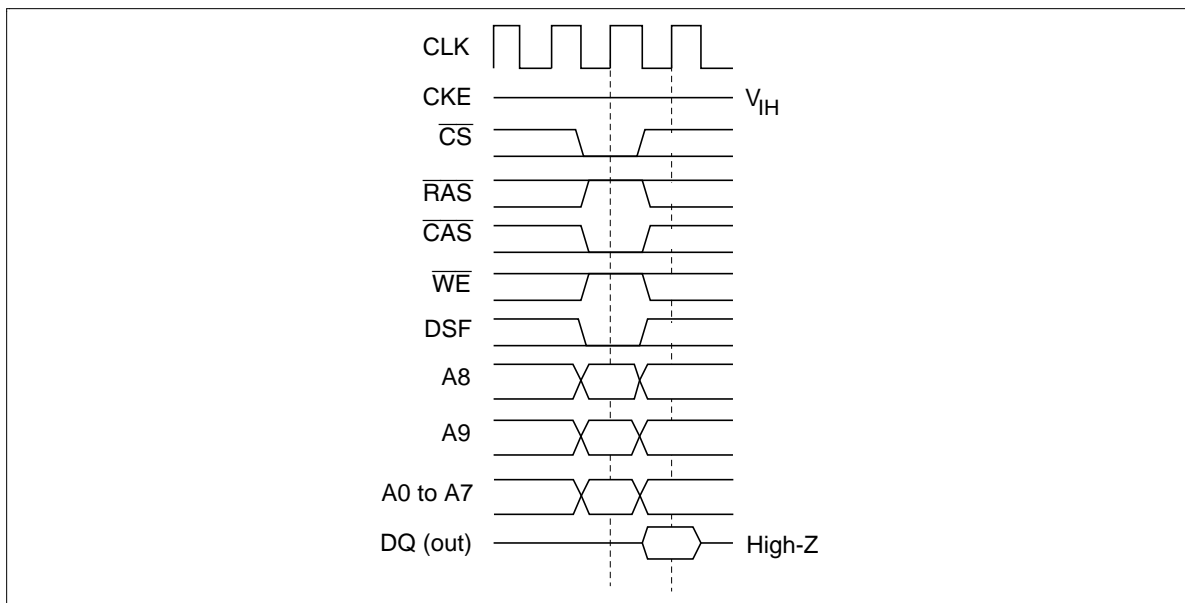
A8 = LOW; Read mode without auto precharge.

[State transition]

Row active — (Column address and read command) -> Row active

Row active — (Column address and read command) -> Idle (auto precharge)

### Column Address and Read Command CL = 1, BL = 1.



**Column address and write command:** For a row of one of two banks activated by ACTV or ACTVM, at the CLK rising edge, by setting CS, CAS, DSF, WE; LOW, RAS; HIGH, the data on DQ pins are input. A9 determines the bank address. A0 to A7 determine the column address.

For write, data should start to be input at the same cycle of the command input.

Burst length stored in MRS determines the expected data length to be input.

If the bank, for which command is input, is activated by ACTVM, then I/O bit mask function or write per bit is available.

[Option]

A8 = HIGH; auto precharge mode or execute precharge automatically after finishing data input.

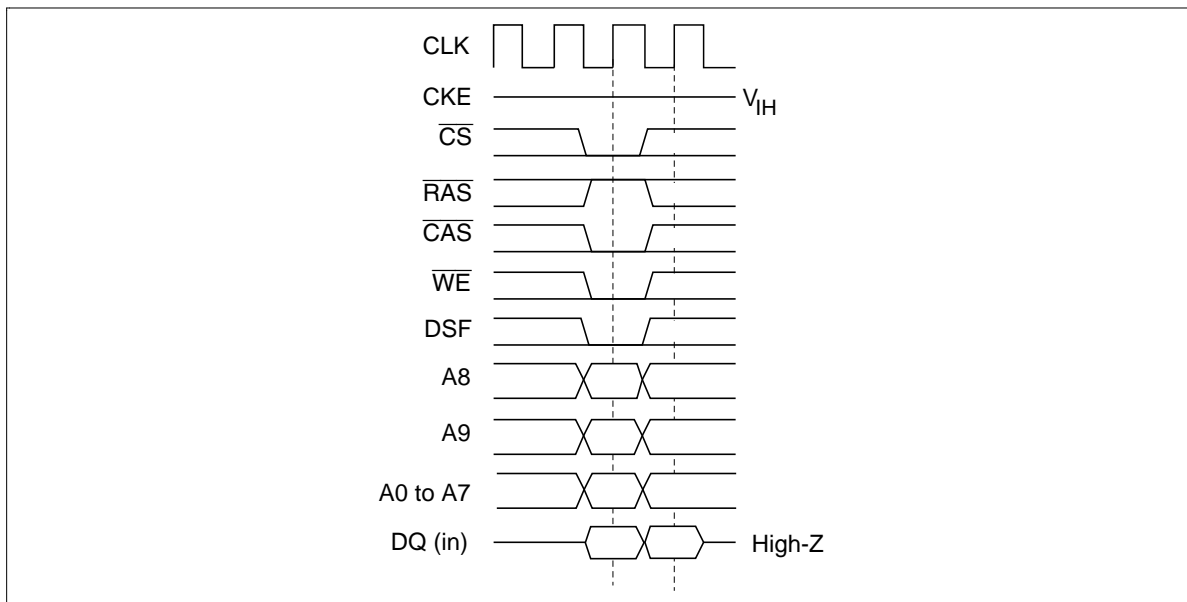
A8 = LOW; write mode without auto precharge.

[State transition]

Row active — (Column address and write command) ->Row active

Row active — (Column address and write command) ->Idle (auto precharge case)

#### Column Address and Write Command (BL = 2)



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## HM5283206 Series

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**Burst stop command (BST):** At the CLK rising edge, by setting  $\overline{\text{CS}}$ ,  $\overline{\text{WE}}$ , DSF: LOW,

$\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ; HIGH,

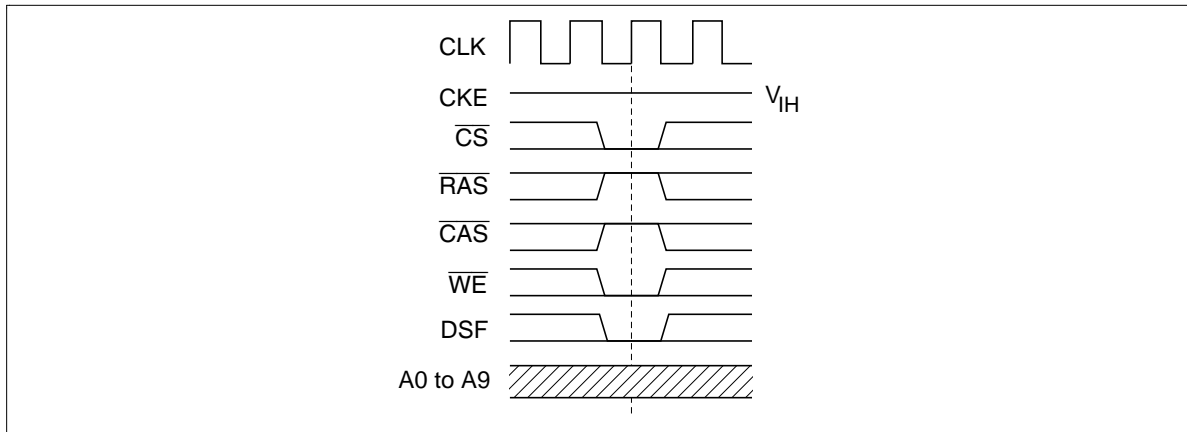
full page burst (BL = 256) read/write is interrupted.

If BL is set to 1, 2, 4, 8, to try to execute this command is illegal.

[State transition]

Row active — (Burst stop command) -> Row active

### Burst Stop Command

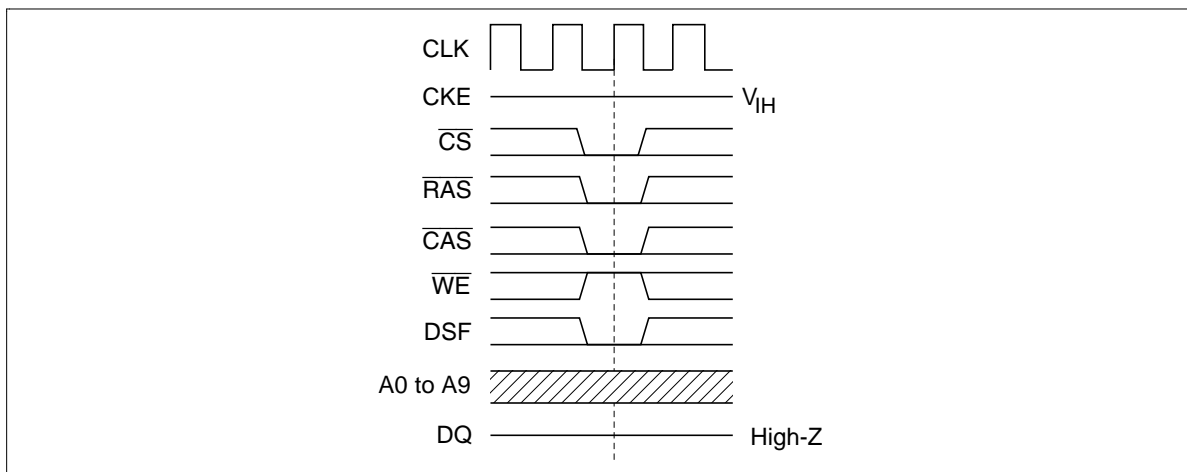


**Auto refresh command (REF):** If both banks are in idle state, at the CLK rising edge, by setting  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , DSF; LOW,  $\overline{\text{WE}}$ ; HIGH, the HM5283206 starts auto-refresh (CBR type) operation. Refresh address is internally generated. No precharge commands are required after autorefresh, since precharge is automatically performed for both banks.

[State transition]

Idle — (Auto refresh command) -> Idle

#### Auto Refresh Command



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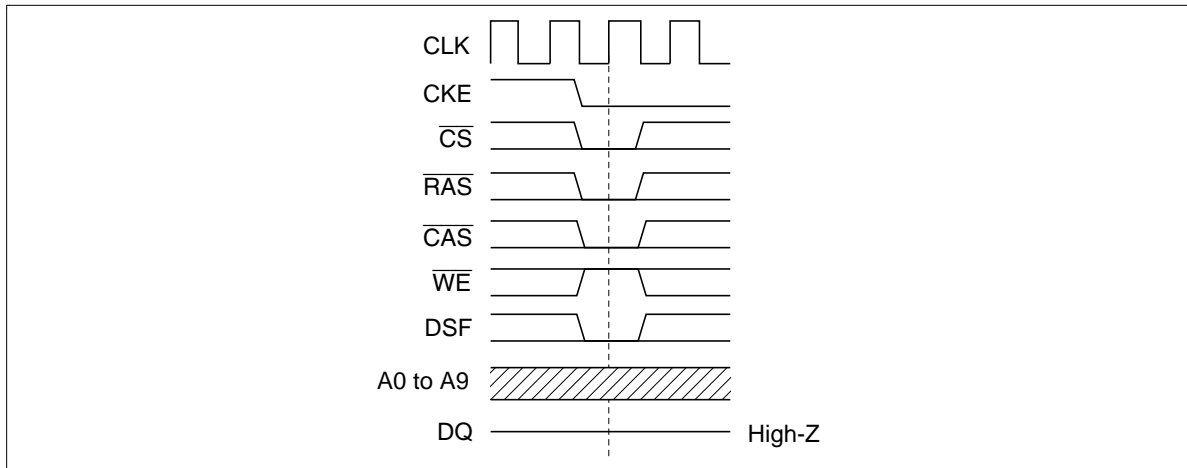
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**Self refresh command (REF):** If both banks are in idle state, at the CLK rising edge, by setting  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , DSF; LOW,  $\overline{\text{WE}}$ ; HIGH, and if CKE's falling edge is detected, the HM5283206 starts self-refresh operation. Self-refresh operation is kept while CKE is LOW.

[State transition]

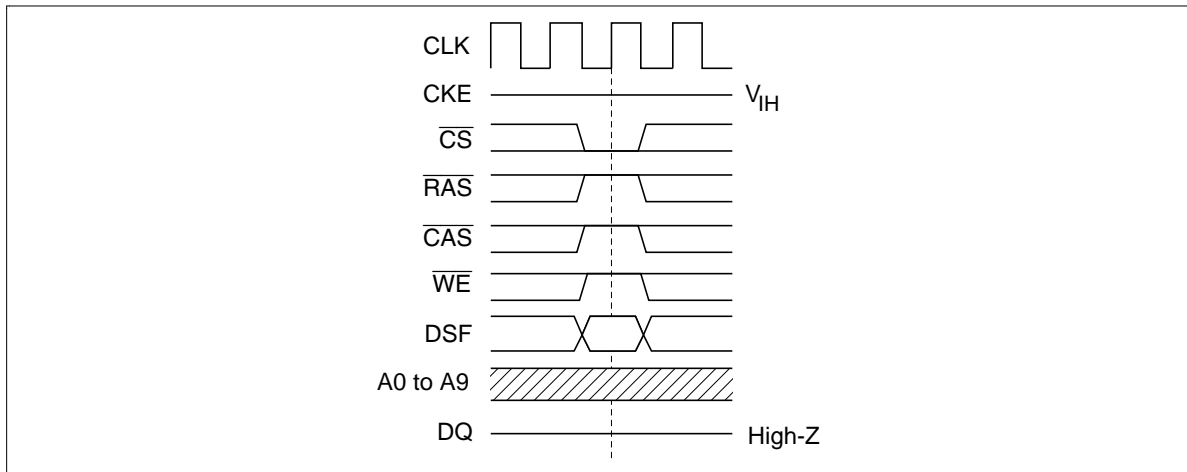
Idle — (Self refresh command) -> Self refresh mode

### Self Refresh Command



**No operation command (NOP):** At the CLK rising edge, by setting  
 $\overline{\text{CS}}$ ; LOW,  
 $\overline{\text{WE}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ; HIGH,  
 [State transition]  
 No transition

#### No Operation Command



**Ignore command (DESL):** At the CLK rising edge, by setting  
 $\overline{\text{CS}}$ ; HIGH, any input is ignored.

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## HM5283206 Series

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### Graphic Commands

**Special mode register set command (SMRS):** If each banks is in idle state or activated, at the CLK rising edge, by setting  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ; LOW, DSF; HIGH, an internal register (the special mode register; SMRS) are set. The data through address pins, at the cycle when this command is input, are stored in the special mode register.

A0 to A4: reserved. should be LOW when SMRS is issued.

A5: determines whether loading mask data or not when SMRS is issued.

A6: determines whether loading color data or not when SMRS is issued.

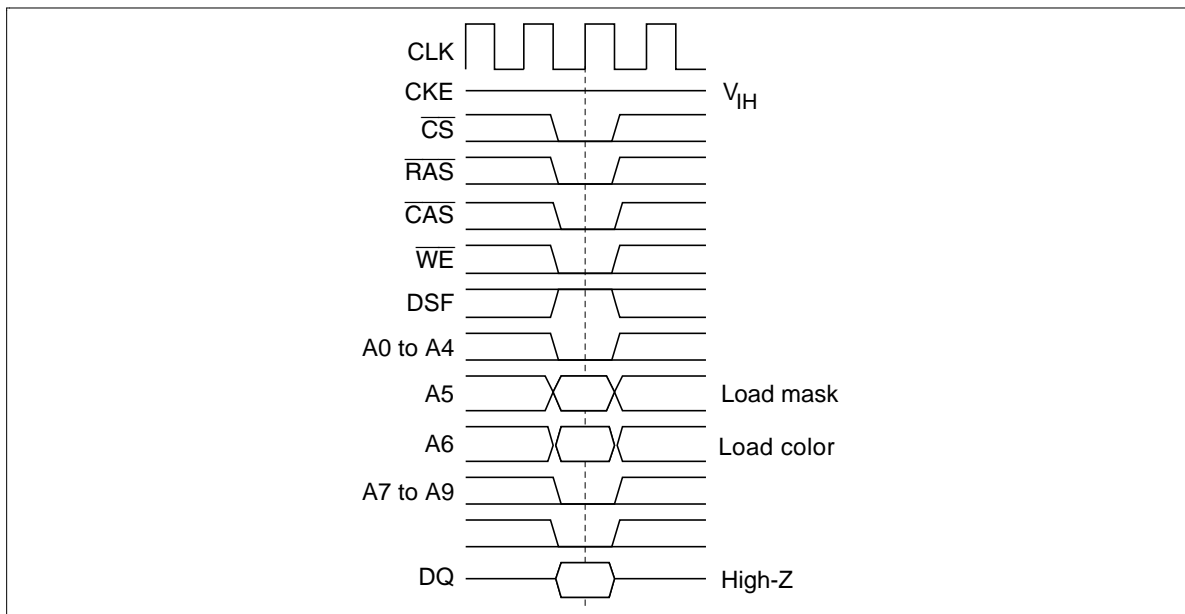
A7 to A9: reserved. should be set LOW when SMRS is issued.

In case A5 bit of the mode register = HIGH, the data through DQ pins, at the cycle this command is issued, are stored in the MASK register (32 bits). If write per bit function is available\*, and DQi (i = 0,...,31) bit of the MASK register = LOW, DQi data path to memory array is masked.

In case A6 bit of the mode register HIGH, the data through DQ pins, at the cycle when this command is issued, are stored in the COLOR register (32 bits). This specific data is written to 8 columns in one clock cycle by block write command.

Note: When bank active command is issued and DSF set to HIGH, write per bit function is enabled.

### Special Mode Register Set Command



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## HM5283206 Series

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### Special Mode Register Configuration

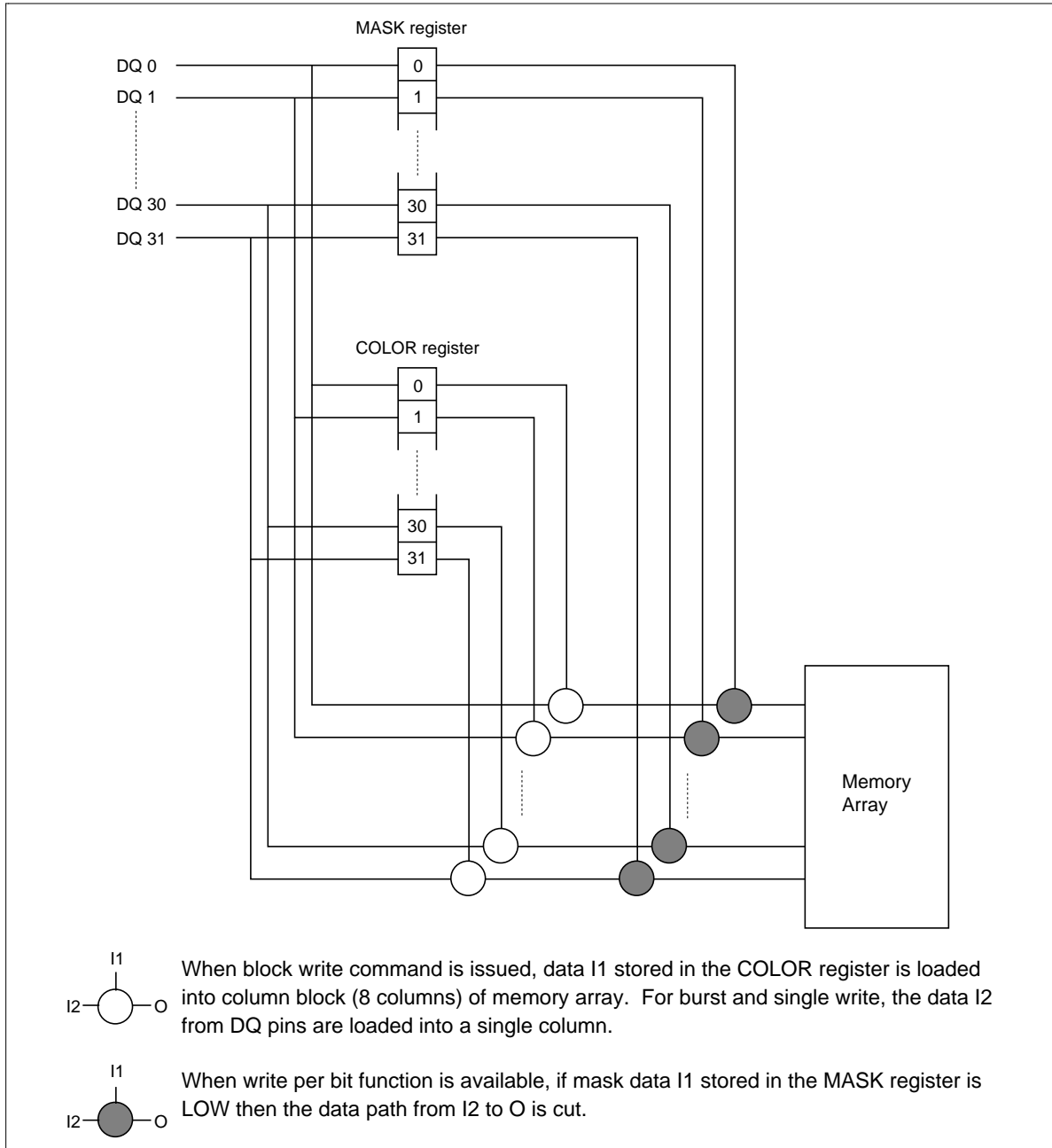
A5	A6	Function	
0	×	Disable	Load Mask
1	0	Enable	
×	0	Disable	Load Color
0	1	Enable	
1	1	ILLEGAL	

Note: ×:  $V_{IH}$  or  $V_{IL}$

### Reserved Bits

A0	A1	A2	A3	A4	A7	A8	A9
0	0	0	0	0	0	0	0

## Graphic Function Block Diagram



**Column address and block write command:** For a row of one of two banks activated by ACTV or ACTVM, at the CLK rising edge, by setting

$\overline{\text{CS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ; LOW,

$\overline{\text{RAS}}$ , DSF; HIGH,

a block write \*<sup>2</sup> is executed.

A9 determines the bank address.

A0 to A2 HIGH or LOW (ignored).

A3 to A7 determine the column block address.

The data through DQ pins, at the cycle when the block write command input, are referred to stop the color data to be written onto the specific column. (Column mask)

[Option]

A8 = HIGH; Auto precharge mode or execute precharge automatically after finishing a block write execution.

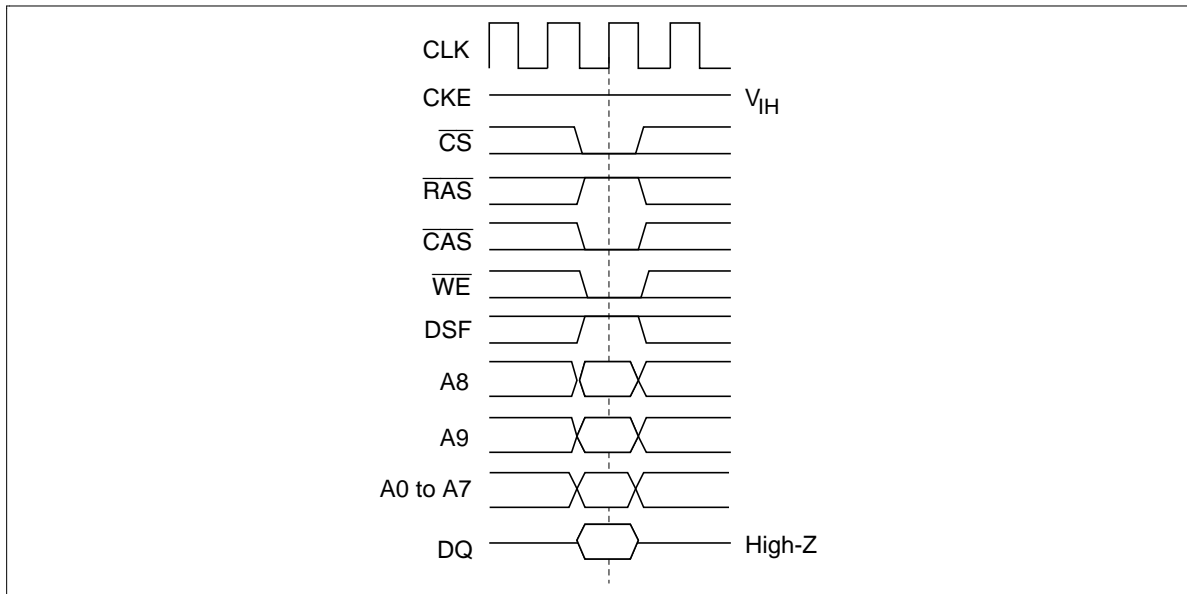
A8 = LOW; Write mode without auto precharge.

[State transition]

Row active — (Block write command) -> Row active

Row active — (Block write command) -> Idle(auto precharge case)

## Column Address and Block Write Command



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## HM5283206 Series

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### Column Block

Column location			Column block location				
A0	A1	A2	A3	A4	A5	A6	A7
0	0	0	a3	a4	a5	a6	a7
1	0	0	a3	a4	a5	a6	a7
0	1	0	a3	a4	a5	a6	a7
1	1	0	a3	a4	a5	a6	a7
0	0	1	a3	a4	a5	a6	a7
1	0	1	a3	a4	a5	a6	a7
0	1	1	a3	a4	a5	a6	a7
1	1	1	a3	a4	a5	a6	a7

Note: 1. a3, a4, a5, a6, a7;  $V_{IH}$  or  $V_{IL}$ .

**DQ Input at the Block Write Cycle and Column Mask Location**

DQ pin NO.	DQ group* <sup>1</sup>	Column location			Column mask	
		A0	A1	A2	No mask	Mask
DQ0	00	0	0	0	High	Low
DQ1	00	1	0	0	High	Low
DQ2	00	0	1	0	High	Low
DQ3	00	1	1	0	High	Low
DQ4	00	0	0	1	High	Low
DQ5	00	1	0	1	High	Low
DQ6	00	0	1	1	High	Low
DQ7	00	1	1	1	High	Low
DQ8	01	0	0	0	High	Low
DQ9	01	1	0	0	High	Low
DQ10	01	0	1	0	High	Low
DQ11	01	1	1	0	High	Low
DQ12	01	0	0	1	High	Low
DQ13	01	1	0	1	High	Low
DQ14	01	0	1	1	High	Low
DQ15	01	1	1	1	High	Low
DQ16	10	0	0	0	High	Low
DQ17	10	1	0	0	High	Low
DQ18	10	0	1	0	High	Low
DQ19	10	1	1	0	High	Low
DQ20	10	0	0	1	High	Low
DQ21	10	1	0	1	High	Low
DQ22	10	0	1	1	High	Low
DQ23	10	1	1	1	High	Low
DQ24	11	0	0	0	High	Low
DQ25	11	1	0	0	High	Low
DQ26	11	0	1	0	High	Low
DQ27	11	1	1	0	High	Low
DQ28	11	0	0	1	High	Low
DQ29	11	1	0	1	High	Low
DQ30	11	0	1	1	High	Low
DQ31	11	1	1	1	High	Low

Note: DQ group: 00; DQ0 to DQ7, 01; DQ8 to DQ15, 10; DQ16 to DQ23, 11; DQ24 to DQ31

## HM5283206 Series

### Command Truth Table

The HM5283206 recognizes the following commands specified by the  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ , DSF and address pins. All other combinations than those in the table below are illegal.

Function	Symbol	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DSF	A9	A8	A0 to A7
		n - 1	n								
Ignore command	DESL* <sup>2</sup>	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop in full page	BST* <sup>3</sup>	H	×	L	H	H	L	L	×	×	×
Column address and read command	READ	H	×	L	H	L	H	L	V	L	V
Read with auto precharge	READ A	H	×	L	H	L	H	L	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	L	V	L	V
Write with auto precharge	WRIT A	H	×	L	H	L	L	L	V	H	V
Row address strobe and bank active	ACTV	H	×	L	L	H	H	L	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	L	×	H	×
Refresh (auto, self)	REF, SELF	H	×	L	L	L	H	L	×	×	×
Mode register set	MRS	H	×	L	L	L	L	L	V	V	V
Row address strobe and bank active and Masked write enable	ACTVM	H	×	L	L	H	H	H	V	V	V
Column address and block write command	BWRIT	H	×	L	H	L	L	H	V	L	V
Block write with auto precharge	BWRITA	H	×	L	H	L	L	H	V	H	V
Special mode register set	SMRS	H	×	L	L	L	L	H	L	L	V

Notes: 1. H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ . V: Valid address input.

2. When  $\overline{\text{CS}}$  is high, the HM5283206 ignores command input. Internal operation is held.

3. Illegal if the burst length is 1, 2, 4 or 8.

**DQM Truth Table**

Function	Symbol	CKE		DQM i
		n – 1	n	
lth byte write enable/output enable	ENB i	H	×	L
lth byte write input/output disable	MASK i	H	×	H

Note: H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ . i = 0, 1, 2, 3.

DQM0 for DQ0 to DQ7, DQM1 for DQ8 to DQ15, DQM2 for DQ16 to DQ23, DQM3 for DQ24 to DQ31

**CKE Truth Table**

Current state	Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address
		n – 1	n						
Active	Clock suspend mode entry	H	L	×	×	×	×	×	×
Any	Clock suspend	L	L	×	×	×	×	×	×
Clock suspend	Clock suspend mode exit	L	H	×	×	×	×	×	×
Idle	Auto refresh command REF	H	H	L	L	L	H	L	×
Idle	Self refresh entry SELF	H	L	L	L	L	H	L	×
Idle	Power down entry	H	L	×	×	×	×	×	×
Self refresh	Self refresh exit	L	H	L	H	H	H	×	×
		L	H	H	×	×	×	×	×
Power down	Power down exit	L	H	L	H	H	H	×	×
		L	H	H	×	×	×	×	×

Note: H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ .

## HM5283206 Series

### Function Truth Table

The following tables show how each command works and what command can be executed in the state given.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Operation
Precharge	H	×	×	×	×	×	DESL	NOP -> Idle after $t_{RP}$
	L	H	H	H	×	×	NOP	NOP -> Idle after $t_{RP}$
	L	H	H	L	L	×	BST	ILLEGAL <sup>*2, *6</sup>
	L	H	L	H	L	BA, CA, A8	READ/READ A	ILLEGAL <sup>*2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL <sup>*2</sup>
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL <sup>*2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	NOP <sup>*3</sup>
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL <sup>*2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL <sup>*2</sup>
Idle	H	×	×	×	×	×	DESL	NOP
	L	H	H	H	×	×	NOP	NOP
	L	H	H	L	L	×	BST	NOP <sup>*6</sup>
	L	H	L	H	L	BA, CA, A8	READ/READ A	ILLEGAL <sup>*2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL <sup>*2</sup>
	L	L	H	H	L	BA, RA	ACTV	Bank and row active
	L	L	H	L	L	BA, A8	PRE, PALL	NOP <sup>*3</sup>
	L	L	L	H	L	×	REF, SELF	Auto self refresh <sup>*4</sup>
	L	L	L	L	L	MODE	MRS	Mode register set <sup>*4</sup>
	L	L	H	H	H	BA, RA	ACTVM	Bank and row active and write per bit enable
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL <sup>*2</sup>
	L	L	L	L	H	Special MODE	SMRS	Special mode register set <sup>*5</sup>

## HM5283206 Series

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Operation
Row active	H	×	×	×	×	×	DESL	NOP
	L	H	H	H	×	×	NOP	NOP
	L	H	H	L	L	×	BST	NOP* <sup>6</sup>
	L	H	L	H	L	BA, CA, A8	READ/READ A	Start read
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	Start write
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL* <sup>2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	Precharge
	L	L	L	×	L			ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL* <sup>2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	Start block write
	L	L	L	L	H	Special MODE	SMRS	Special mode register set* <sup>5</sup>
Read	H	×	×	×	×	×	DESL	NOP -> Burst end -> Row active
	L	H	H	H	×	×	NOP	NOP -> Burst end -> Row active
	L	H	H	L	L	×	BST	Burst stop -> Row active* <sup>6</sup>
	L	H	L	H	L	BA, CA, A8	READ/READ A	Term burst -> Start new read
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	Term burst -> Start write
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL* <sup>2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	Term burst -> Precharge
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL* <sup>2</sup>
Read with auto precharge	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	Term burst -> Start block write
	H	×	×	×	×	×	DESL	NOP -> Burst end -> Precharge
	L	H	H	H	×	×	NOP	NOP -> Burst end -> Precharge
	L	H	H	L	L	×	BST	ILLEGAL
	L	H	L	H	L	BA, CA, A8	READ/READ A	ILLEGAL* <sup>2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL* <sup>2</sup>
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL* <sup>2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL* <sup>2</sup>
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL* <sup>2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL* <sup>2</sup>

## HM5283206 Series

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Operation
Write/BWrite	H	×	×	×	×	×	DESL	NOP -> Burst end -> Write recovering
	L	H	H	H	×	×	NOP	NOP -> Burst end -> Write recovering
	L	H	H	L	L	×	BST	Burst stop -> Row active <sup>*6</sup>
	L	H	L	H	L	BA, CA, A8	READ/READ A	Term burst -> Start read
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	Term burst -> Start new write
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL <sup>*2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	Term burst -> Precharge
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL <sup>*2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	Term burst -> Start block write
Write/Bwrite with auto precharge	H	×	×	×	×	×	DESL	NOP -> Burst end -> Write recovering with precharge
	L	H	H	H	×	×	NOP	NOP -> Burst end -> Write recovering with precharge
	L	H	H	L	L	×	BST	ILLEGAL
	L	H	L	H	L	BA, CA, A8	READ/READ A	ILLEGAL <sup>*2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL <sup>*2</sup>
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL <sup>*2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL <sup>*2</sup>
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL <sup>*2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL <sup>*2</sup>
Write/Bwrite recovering	H	×	×	×	×	×	DESL	NOP -> Row active after $t_{WR}/t_{BWR}$
	L	H	H	H	×	×	NOP	NOP -> Row active after $t_{WR}/t_{BWR}$
	L	H	H	L	L	×	BST	NOP -> Row active after $t_{WR}/t_{BWR}$ <sup>*6</sup>
	L	H	L	H	L	BA, CA, A8	READ/READ A	Start read <sup>*2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	Start new write <sup>*2</sup>
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL <sup>*2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL <sup>*2</sup>
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL <sup>*2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL <sup>*2</sup>

## HM5283206 Series

Current state	CS	RAS	CAS	WE	DSF	Address	Command	Operation
Write/Bwrite recovering with precharge	H	×	×	×	×	×	DESL	NOP -> Precharge after $t_{WR}/t_{BWR}$
	L	H	H	H	×	×	NOP	NOP -> Precharge after $t_{WR}/t_{BWR}$
	L	H	H	L	L	×	BST	ILLEGAL
	L	H	L	H	L	BA, CA, A8	READ/READ A	ILLEGAL <sup>*2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL <sup>*2</sup>
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL <sup>*2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL <sup>*2</sup>
	L	L	L	×	×	×		ILLEGAL
	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL <sup>*2</sup>
Row activating	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL <sup>*2</sup>
	H	×	×	×	×	×	DESL	NOP -> Row active after $t_{RCD}$
	L	H	H	H	×	×	NOP	NOP -> Row active after $t_{RCD}$
	L	H	H	L	L	×	BST	NOP -> Row active after $t_{RCD}^{*6}$
	L	H	L	H	L	BA, CA, A8	READ/READ A	ILLEGAL <sup>*2</sup>
	L	H	L	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL <sup>*2</sup>
	L	L	H	H	L	BA, RA	ACTV	ILLEGAL <sup>*2</sup>
	L	L	H	L	L	BA, A8	PRE, PALL	ILLEGAL <sup>*2</sup>
	L	L	L	×	×	×		ILLEGAL
Refresh (auto precharge)	L	L	H	H	H	BA, RA	ACTVM	ILLEGAL <sup>*2</sup>
	L	H	L	L	H	BA, CA, A8	BWRIT/BWRIT A	ILLEGAL <sup>*2</sup>
	H	×	×	×	×	×	DESL	NOP -> Idle after $t_{RC}$
	L	H	H	H	×	×	NOP	NOP -> Idle after $t_{RC}$
	L	H	H	L	L	×	BST	NOP -> Idle after $t_{RC}^{*6}$
Mode register set	L	H	L	×	×	BA, CA, A8		ILLEGAL
	L	L	×	×	×	×		ILLEGAL
	H	×	×	×	×	×	DESL	NOP -> Idle after $t_{RSC}$
	L	H	H	H	×	×	NOP	NOP -> Idle after $t_{RSC}$
	L	H	H	L	L	×	BST	ILLEGAL
	L	H	L	×	×	BA, CA, A8		ILLEGAL
	L	L	×	×	×	×		ILLEGAL

## HM5283206 Series

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	Address	Command	Operation
Special Mode register set	H	×	×	×	×	×	DESL	NOP -> Idle after $t_{RSC}$ or row active after $t_{SBW}$
	L	H	H	H	×	×	NOP	NOP -> Idle after $t_{RSC}$ or row active after $t_{SBW}$
	L	H	H	L	L	×	BST	ILLEGAL
	L	H	L	×	×	BA, CA, A8		ILLEGAL
	L	L	×	×	×	×		ILLEGAL

Notes: 1. H:  $V_{IH}$ . L:  $V_{IL}$ . ×:  $V_{IH}$  or  $V_{IL}$ .

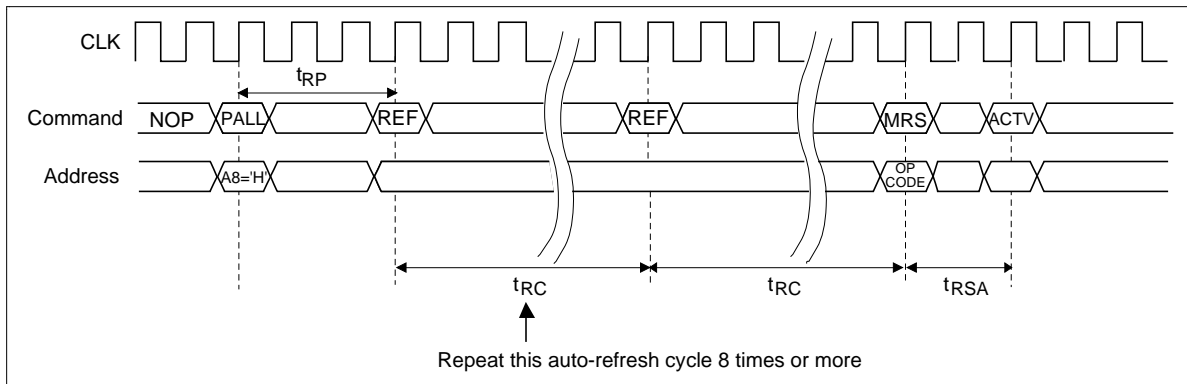
2. To execute this command for the current bank is illegal. However this command can be executed for another bank depends on the state of another bank.
3. NOP for the current bank or the bank in idle state. Precharge for the bank in other state.
4. Illegal, if both banks are not in idle state.
5. Illegal, if another bank is not in active or idle state.
6. In burst read/write, if BL is set to 1, 2, 4, 8, to try to execute BST command is illegal.

## Operations of HM5283206 Series

**Power on sequence:** In order to get rid of data contention of I/O bus when power on, the following power on sequence recommended to be performed before any operation.

1. Apply power and start clock. Keep a NOP condition.
2. Maintain stable power, stable clock, and NOP condition for 200  $\mu$ s.
3. Execute precharge command (PALL: A8 = HIGH).
4. Execute 8 or more auto refresh commands (REF)  $t_{RP}$  after the precharge command as dummy. An interval  $t_{RC}$  is necessary between two consecutive auto refresh commands.
5. Execute a mode register set command (MRS)  $t_{RC}$  after the last auto refresh command input.

### Power on Sequence



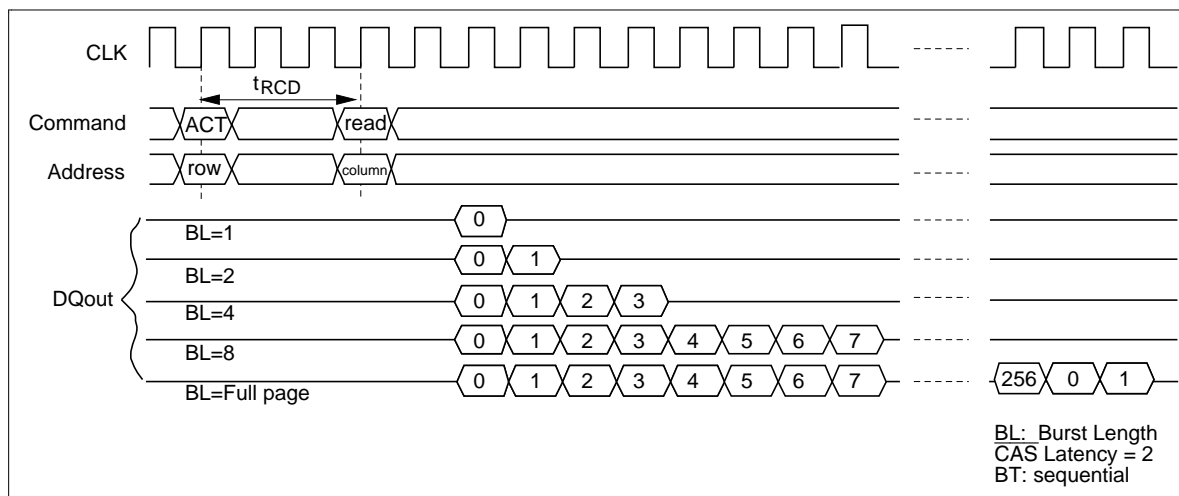
### Read/Write Operations

**Bank active:** A read/write operation begins with a bank active command (ACTV or ACTVM). The bank active command determines a bank (A9) and a row address (AX0 to AX8). For the bank and the row, a read/write command can be applied. An interval not less than  $t_{RCD}$ , after an ACTV/ ACTVM command to a read/write command, is required.

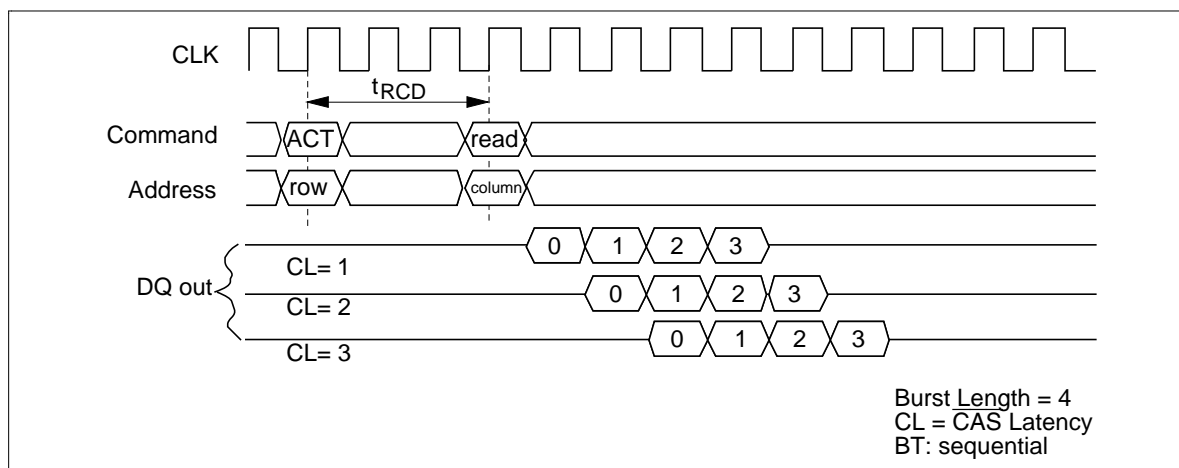
**Read operation:** Burst length (BL),  $\overline{CAS}$  latency (CL) and burst type (BT) of the mode register are referred when read command is executed. Burst length (BL) determines the length of a sequential data by a single read command, which can be set to 1, 2, 4, 8 or 256 (full-page). Starting address of a burst data is defined by column address (AY0 to AY7) and bank select address (A9) loaded through A0 to A9 in the cycle when the read command is issued.  $\overline{CAS}$  latency (CL) determines the delay of data output after read command input. When burst length is 1, 2, 4 or 8, DQ buffers automatically become High-Z at the next cycle after completion of burst read. When burst length is full-page (256), data are repeatedly output until a burst stop command, a read/write command or a precharge command is input.

## HM5283206 Series

### Burst Length



### CAS Latency



**Burst operation (on read or write):** One burst data output/input by one read/write command are included in a column block determined by A1 to A7 in case BL (Burst Length) = 2, by A2 to A7 in case BL = 4 and by A3 to A7 in case BL = 8. Burst type (BT) determines the order how data of the column block are output/input. There are two burst types, sequential (wrap around) or interleave. The order of the burst data depends also on the start column location of the burst data. See tables below for details.

**Column Block**
**BL = 2**

Column location		Column block location					
A0	A1	A2	A3	A4	A5	A6	A7
0	a1	a2	a3	a4	a5	a6	a7
1	a1	a2	a3	a4	a5	a6	a7

Note: a1, a2, a3, a4, a5, a6, a7;  $V_{IH}$  or  $V_{IL}$ .

**BL = 4**

Column location		Column block location					
A0	A1	A2	A3	A4	A5	A6	A7
0	0	a2	a3	a4	a5	a6	a7
1	0	a2	a3	a4	a5	a6	a7
0	1	a2	a3	a4	a5	a6	a7
1	1	a2	a3	a4	a5	a6	a7

Note: a2, a3, a4, a5, a6, a7;  $V_{IH}$  or  $V_{IL}$ .

**BL = 8**

Column location			Column block location				
A0	A1	A2	A3	A4	A5	A6	A7
0	0	0	a3	a4	a5	a6	a7
1	0	0	a3	a4	a5	a6	a7
0	1	0	a3	a4	a5	a6	a7
1	1	0	a3	a4	a5	a6	a7
0	0	1	a3	a4	a5	a6	a7
1	0	1	a3	a4	a5	a6	a7
0	1	1	a3	a4	a5	a6	a7
1	1	1	a3	a4	a5	a6	a7

Note: a3, a4, a5, a6, a7;  $V_{IH}$  or  $V_{IL}$ .

## HM5283206 Series

### The Order of Burst Operation

#### BL = 2

Start column location		Order in decimal BL = 2			
A0		Sequential		Interleave	
0		0	1	0	1
1		1	0	1	0

#### BL = 4

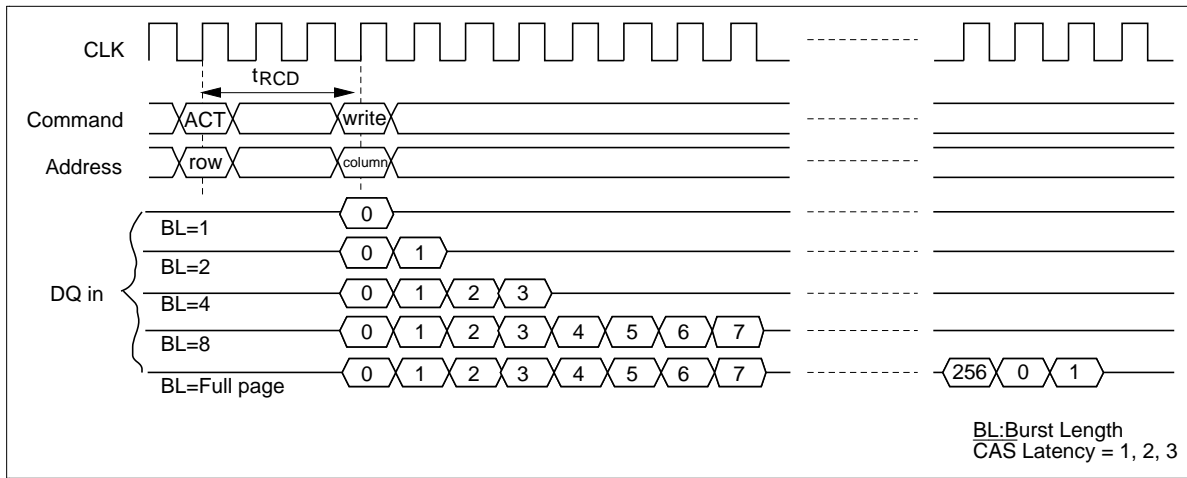
Start column location		Order in decimal BL = 4							
A0      A1		Sequential				Interleave			
0	0	0	1	2	3	0	1	2	3
1	0	1	2	3	0	1	0	3	2
0	1	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

#### BL = 8

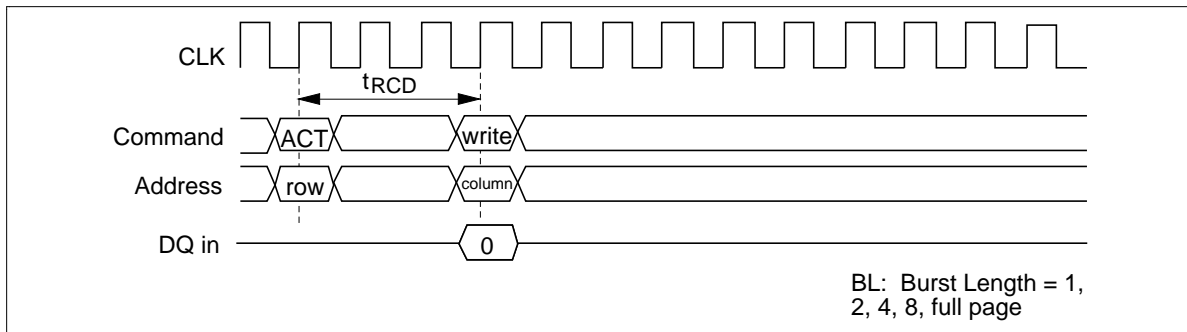
Start column location			Order in decimal BL = 8															
A0	A1	A2	Sequential								Interleave							
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
1	0	0	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
1	1	0	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
0	0	1	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
0	1	1	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

**Write operation:** OPCODE (A9, A8) of the mode register is referred when a write command is executed as well as BL (Burst Length) and BT (Burst Type). CL ( $\overline{\text{CAS}}$  Latency) is ignored and CL is fixed to 0 for write operation, that is, write data input starts on the same cycle when the write command is issued.

**Burst write:** Before executing a burst write operation, OPCODE (A9, A8) should be set to (0, 0). Burst length (BL) determines the length of a sequential data by the burst write command, which can be set to 1, 2, 4, 8 or 256 (full-page). Starting address of a burst data is defined by column address (AY0 to AY7) and bank select address (A9) loaded through A0 to A9 in the cycle when the burst write command is issued.



**Single write:** Before executing a single write operation, OPCODE (A9, A8) should be set to (1, 0). In the single write operation, data are only written to the single column defined by the column address and the bank select address loaded at the write command set cycle regardless of the defined burst length. (The latency of data input is 0).

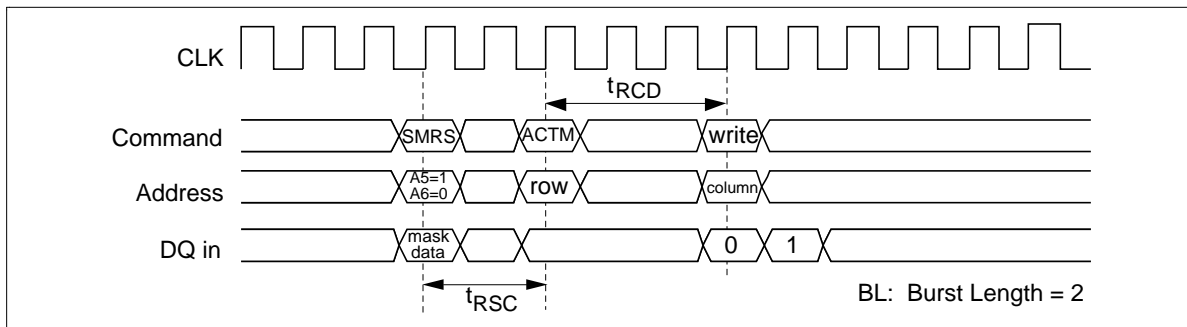


## HM5283206 Series

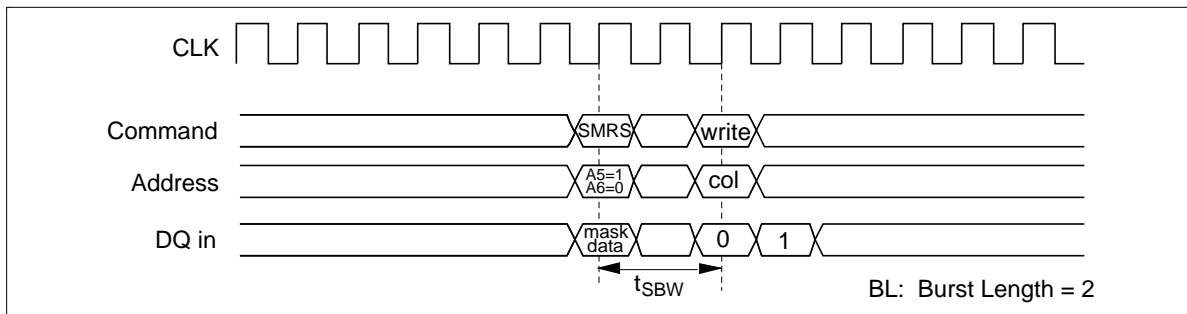
**Write per bit:** To use write per bit function,

1. Set mask data in advance, which define DQ paths to be masked, to the MASK register by SMRS command. An interval not less than  $t_{RSC}$  after a SMRS command to an ACTVM command is necessary.
2. Use ACTVM command to activate the bank for which write per bit operation is performed. An interval not less than  $t_{RCD}$  after an ACTVM command to a write or a block write command, is necessary.
3. Execute a write or a block write command. In this write operation, DQ paths defined by mask register are masked to preserve the previous data. (See the example below)

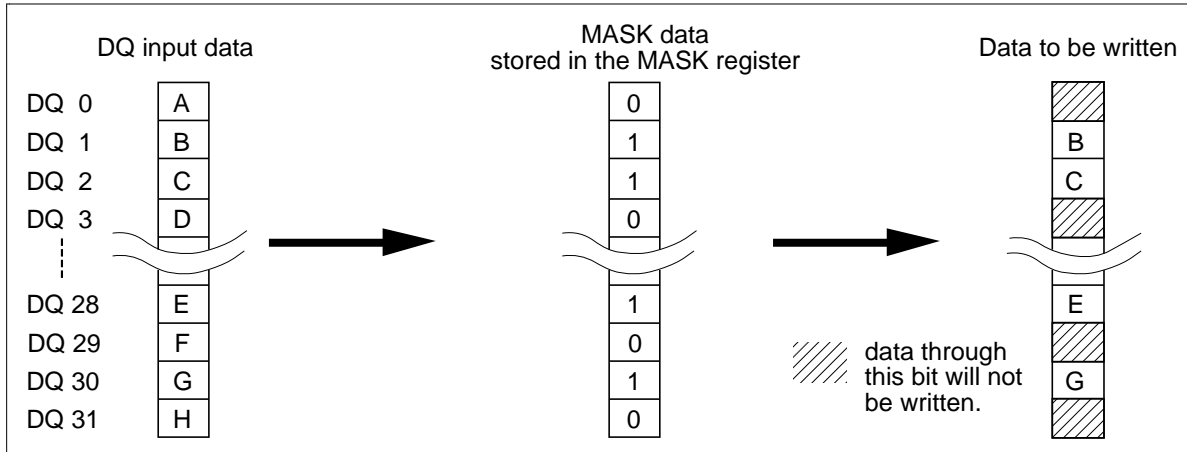
### Special Mode Register Set (Load Mask) in Idle State and Write Per Bit



### Special Mode Register Set (Load Mask) in Active State and Write Per Bit

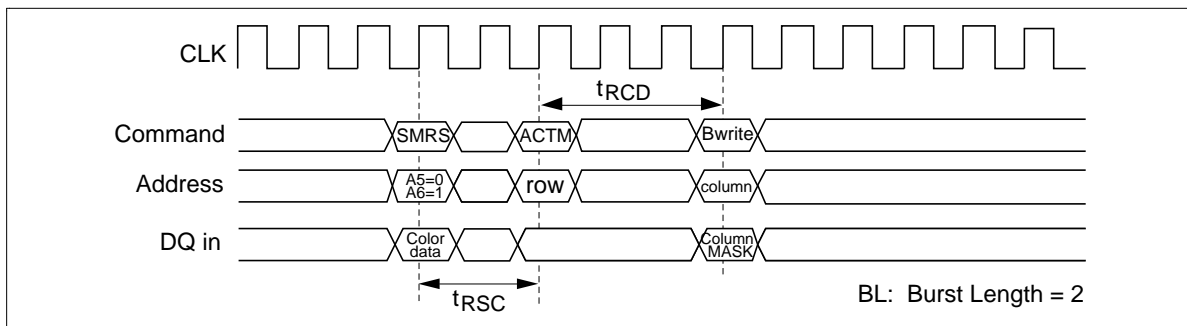


### Write Per Bit Example



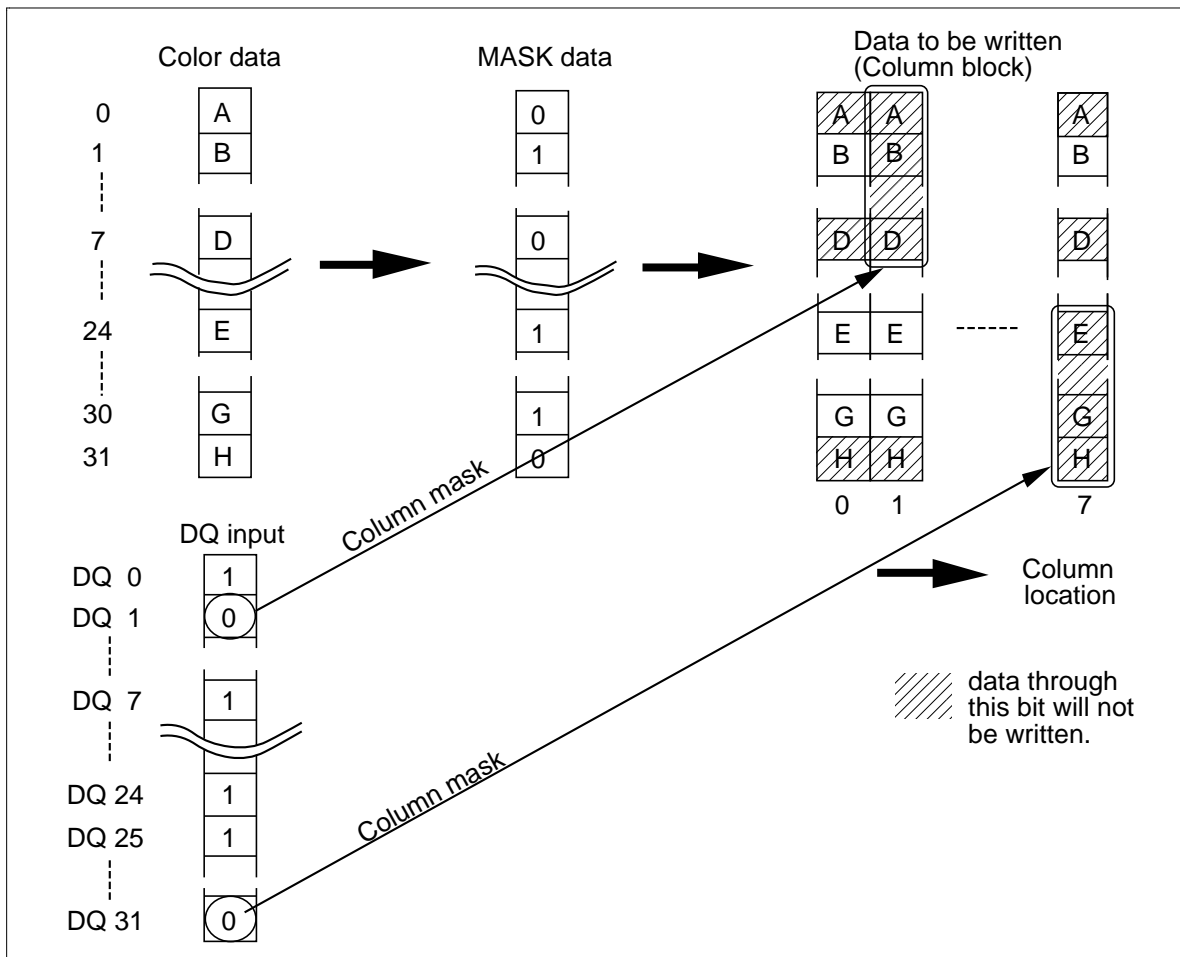
**Block write:** Before executing a block write command, a color data (32 bit) should be set in advance, which is allowed to be written in 8 columns at one write cycle, to the color register by SMRS command. An interval not less than  $t_{RSC}$  after a SMRS command to an ACTVM command is necessary. If a SMRS command is executed in active state to set the color register, an interval not less than  $t_{SBW}$  is required before executing a block write command after the SMRS command. If a block write command is applied to the bank which is activated by ACTVM command, write per bit function is also available. DQ inputs at the cycle, when a block write command is executed, are referred to mask the specific columns. See the example below.

### Special Mode Register Set (Load Mask) in Idle State and Block Write



## HM5283206 Series

### Block Write Example with Write Per Bit

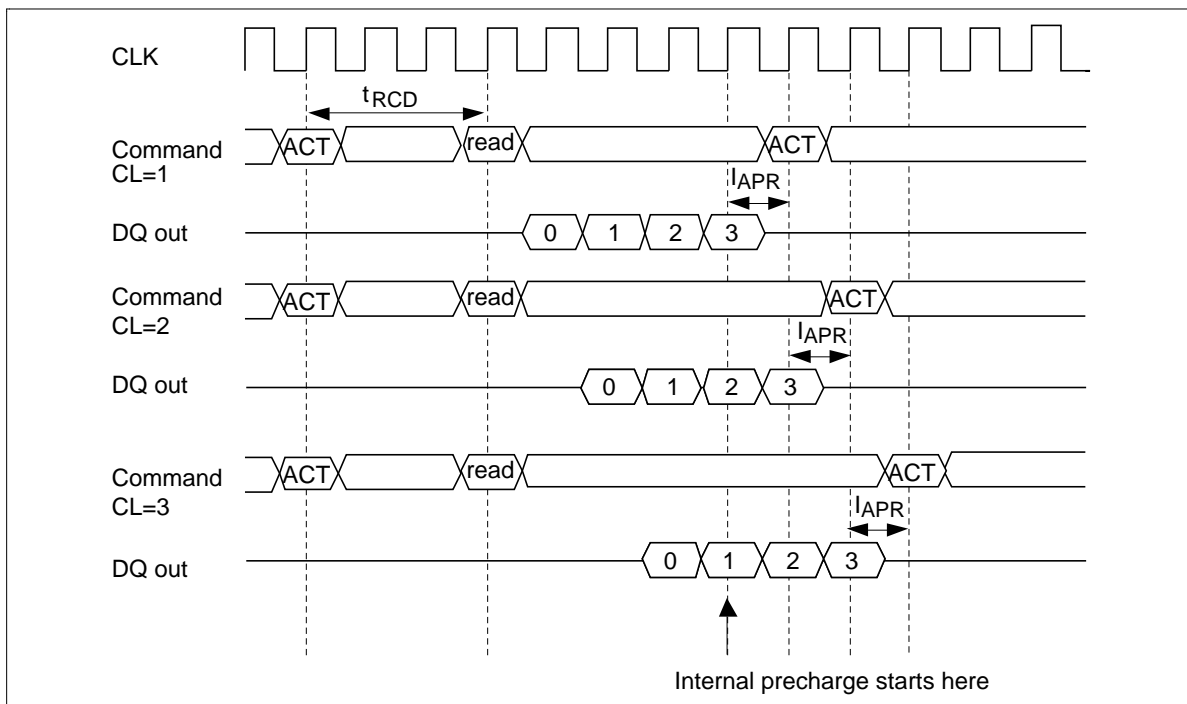


### Auto Precharge

**Read with auto precharge:** In this operation, since precharge is automatically performed after completing a read operation, so no precharge commands are necessary after each read operation. The command next to this command must be a bank active (ACTV, ACTVM) command. In addition, an interval defined by  $t_{APR}$  is required prior to the next command.

Note: In executing read with auto precharge command, every command to another bank is ignored until internal precharge completed.

CAS latency		Precharge start cycle
3	2	cycle before the last data out
2	1	cycle before the last data out
1	0	cycle before the last data out

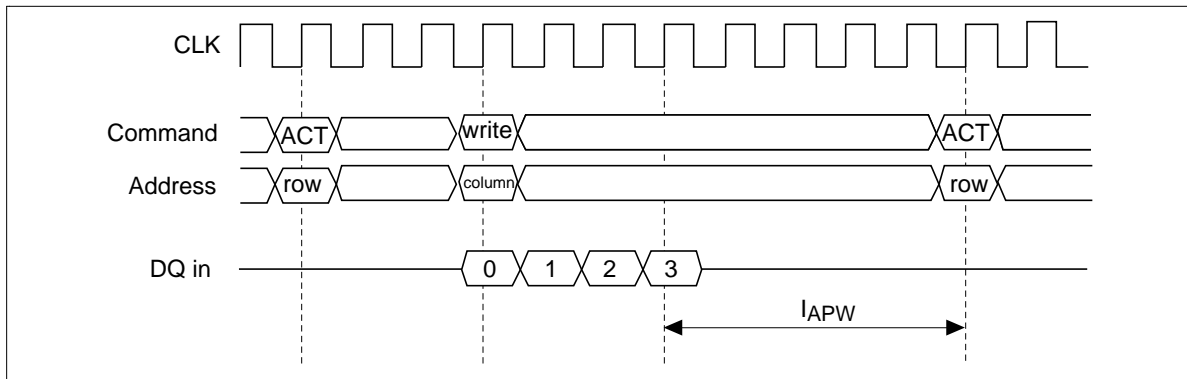


## HM5283206 Series

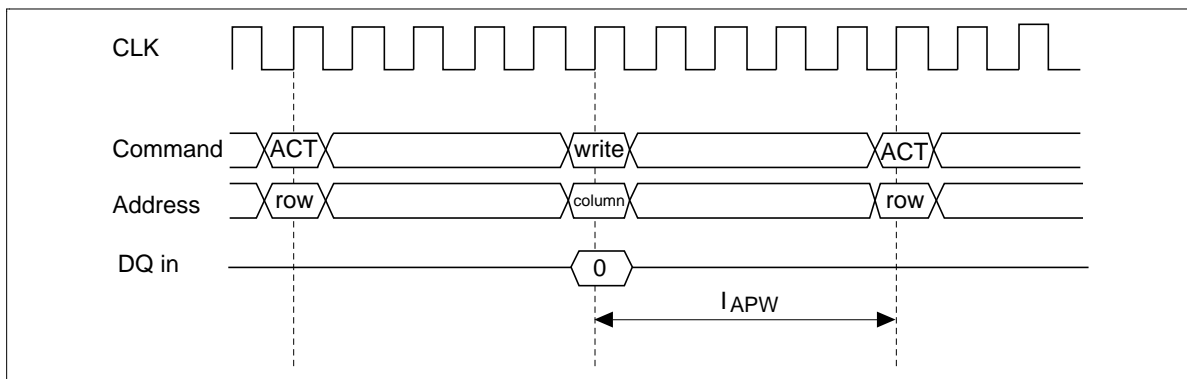
**Write with auto precharge:** In this operation, since precharge is automatically performed after completion of a burst write or a single write operation, so no precharge commands are necessary after the write operation. The command next to this command must be a bank active command (ACTV, ACTVM). In addition, an interval of  $t_{APW}$  is required between the last valid data and the following command.

Note: In executing write with auto precharge command, every command to another bank is ignored until internal precharge completed.

### Burst Write (Burst Length = 4)

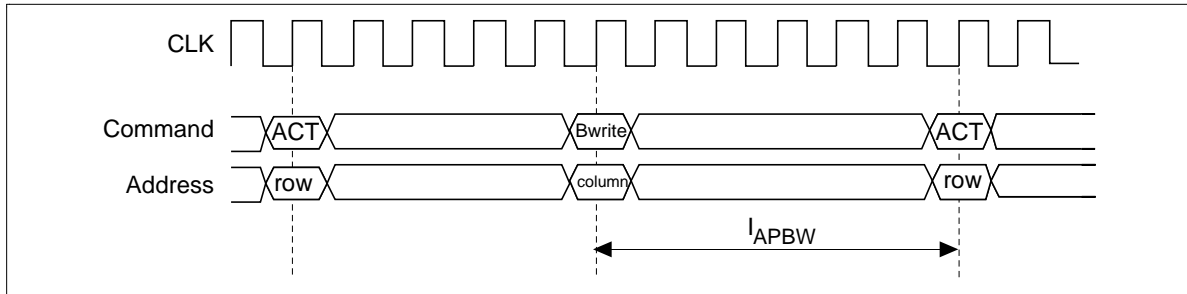


### Single Write



**Block write with auto-precharge:** In this operation, since precharge is automatically performed after completion of a block write operation, so no need to execute precharge command. The following command must be a bank active command (ACTV, ACTVM). In addition, an interval of  $I_{APBW}$  is required between the last valid data input and the following command.

#### Block Write with Auto Precharge



#### Full Page Burst Stop

**Burst stop command during burst read:** Burst stop command is used to stop data output during a full-page burst read. This command sets the output buffer to High-Z and stops the full-page burst read. The timing, from command input to the last data, depends on  $\overline{CAS}$  latency. BST command is legitimate only in case full page burst mode, and is illegal in case burst length 1, 2, 4 or 8.

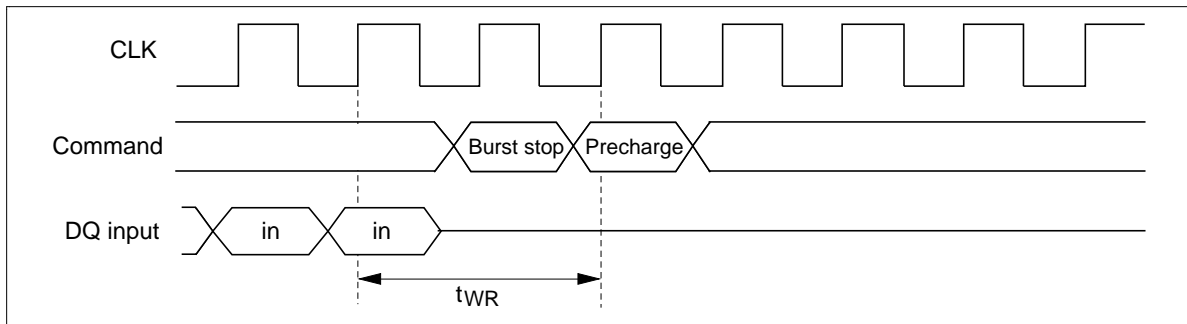
$\overline{CAS}$ latency	BST to valid data	BST to high impedance
1	0	1
2	1	2
3	2	3

**CAS Latency = 1, Burst Length = Full Page**



**Burst stop command at burst write:** For full page burst write cycle, when a burst stop command is issued, the write data at that cycle and the following write data input are ignored. The BST command is legitimate only in case full page burst mode, and is illegal for burst length 1, 2, 4 or 8.

**Burst Length = Full Page**

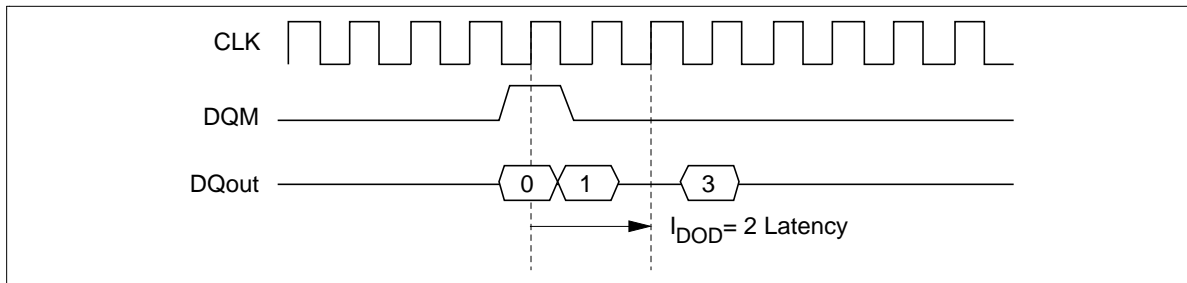


## HM5283206 Series

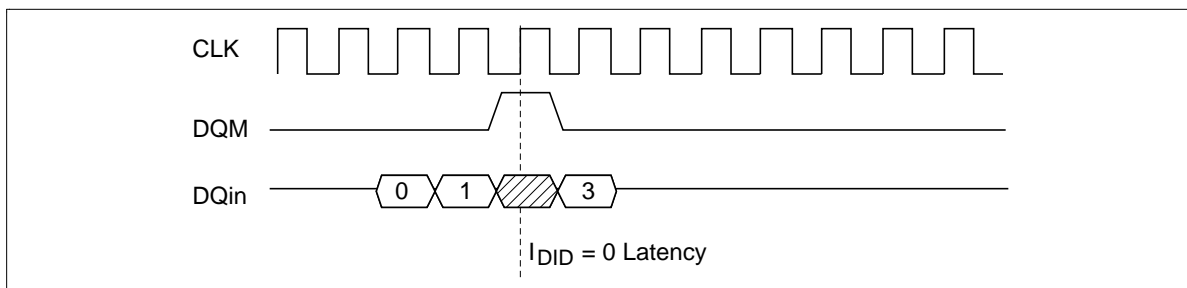
### DQM Control

The DQM  $i$  ( $i=0, 1, 2, 3$ ) controls the  $i$ th byte of DQ data. DQM control operation for read and for write are different in terms of latency.

**Reading:** When data are read, output buffer can be controlled by DQM $i$ . By setting DQM $i$  to LOW, the corresponding DQ output buffers become active. By setting DQM $i$  to HIGH, the corresponding DQ output buffers are made floated so that the  $i$ th byte of data are not driven out. The latency of DQM operation for read operation is 2.



**Writing:** Input data can be controlled by DQM $i$ . While DQM $i$  is LOW, data is driven into the HM5283206. By setting DQM $i$  to HIGH, corresponding  $i$ th byte of DQ input data are kept from being written to the HM5283206 and the previous data are protected. The latency of DQM control operation is 0.



## **Refresh**

**Auto Refresh:** All the banks must be precharged before executing an auto-refresh command. Auto refresh command increments the internal counter every time when it is executed. This command also determines the row to be refreshed. Therefore external address specification is not necessary. Refresh cycle is 1024 cycles/16 ms. (1024 cycles are required to refresh all the row addresses.) All output buffers become High-Z after auto-refresh start. No precharge commands are necessary after this operation.

**Self Refresh:** When issuing a self refresh command, by changing the level on CKE pin from HIGH to LOW simultaneously, a self refresh operation starts and is kept while CKE is LOW. During the self-refresh operation, all data schedule to be refreshed internally. This operation managed by an internal refresh timer. After exiting from the self refresh, since the last row refreshed cannot be determined, auto-refresh commands should immediately be performed for all addresses. Change the level on the CKE pin from LOW to HIGH to exit from Self refresh mode.

## **Others**

**Power Down Mode:** Power down mode is a state in which all input buffers except the CKE input buffer are made inactive and clock signal is masked to cut power dissipation. To enter into power down mode, CKE should be set to low. Power down mode is kept as long as CKE is low. Change the level on the CKE pin from LOW to HIGH to exit from Power down mode. In this mode, internal refresh is not performed.

**Clock Suspend:** The HM5283206 enters into clock suspend mode from active mode by setting CKE to low. There are several types of clock suspend mode depends on the state when CKE level is changed from HIGH to LOW.

**ACTIVE clock suspend:** If CKE-transition (1 to 0) happens during a bank active state, the bank active status is kept. Any input signals are ignored during this mode.

**READ and READ A suspend:** If CKE transition (1 to 0) happens during a read operation, the read operation is kept or DQ output data is driven out until completion. Any input signals are ignored during this mode.

**WRITE (BLOCK WRITE) and WRITE A (BLOCK WRITE A) suspend:** If CKE-transition (1 to 0) happens during a write operation, though any input signals include DQ input data ignored, the write operation is kept until completion. Any input signals are ignored during this mode.

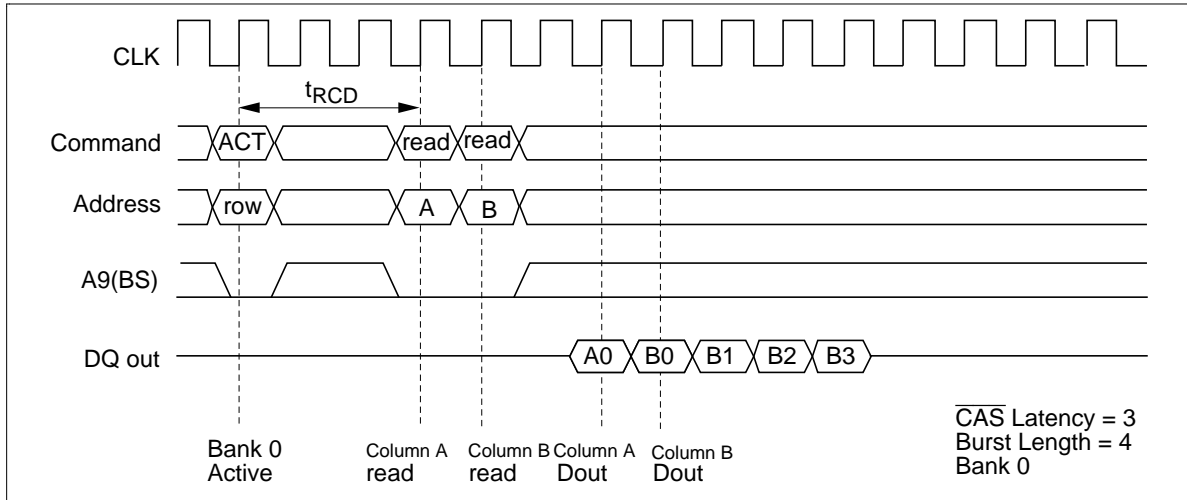
Change the level on the CKE pin from LOW to HIGH to exit from Clock suspend mode.

## HM5283206 Series

### Command Intervals

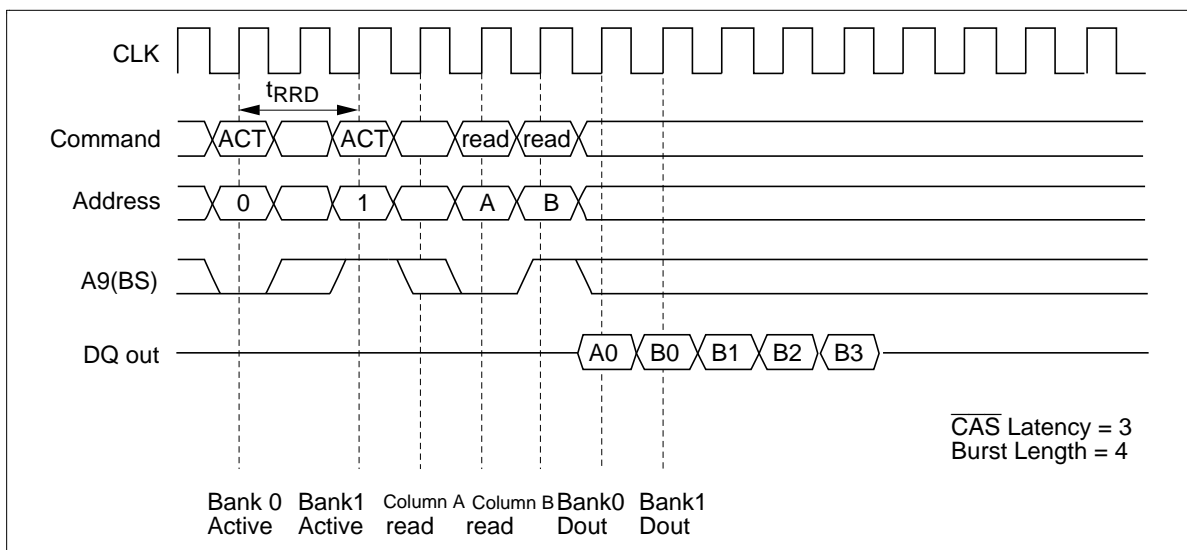
#### Read Command to Read Command Interval:

1. Operation for a column in the same row: Read command can be issued every cycle. Note that the latest read command has the priority to the preceding read command, that is, any read command can interrupt the preceding burst read operation to get valid data aimed by this interruption.



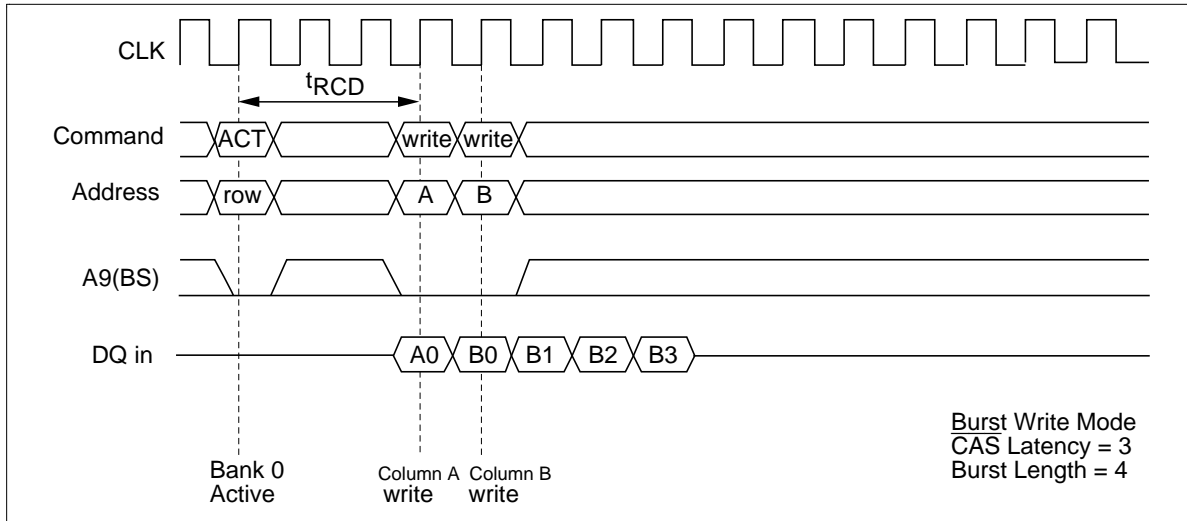
2. Operation for a column in other row of the same bank: It is necessary to execute a precharge command and a bank-active command before executing the new read command.

3. Operation for another bank: For another bank in active state, the new read command can be executed in the next cycle after the preceding read command is issued. If another bank is in idle state, a bank active command should be executed before executing the new read command.

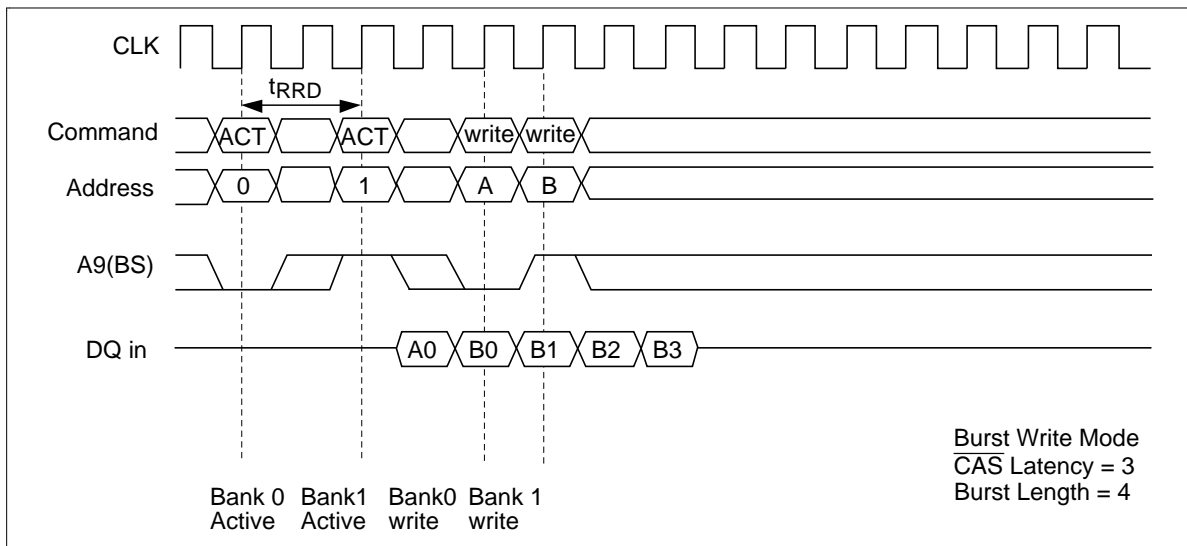


**Write Command to Write Command Interval:**

1. Operation for a column in the same row : Write command can be issued every cycle. Note that the latest write command has the priority to the preceding write command, that is, any write command can interrupt the preceding burst write operation to get valid data



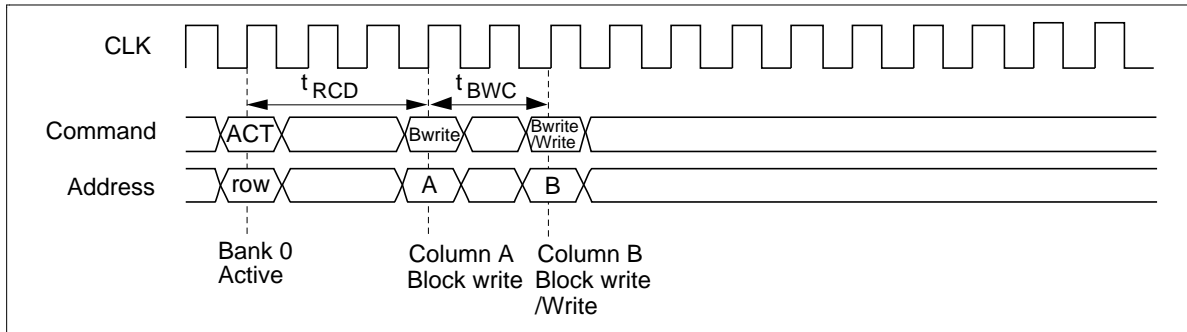
2. Operation for a column in other row of the same bank: It is necessary to execute a precharge command and a bank active command before executing the following write command.
3. Operation for another bank: For another bank in active state, the following burst write command can be executed in the next cycle after the preceding write command is issued. If another bank is in the idle state, bank active command should be executed.



## HM5283206 Series

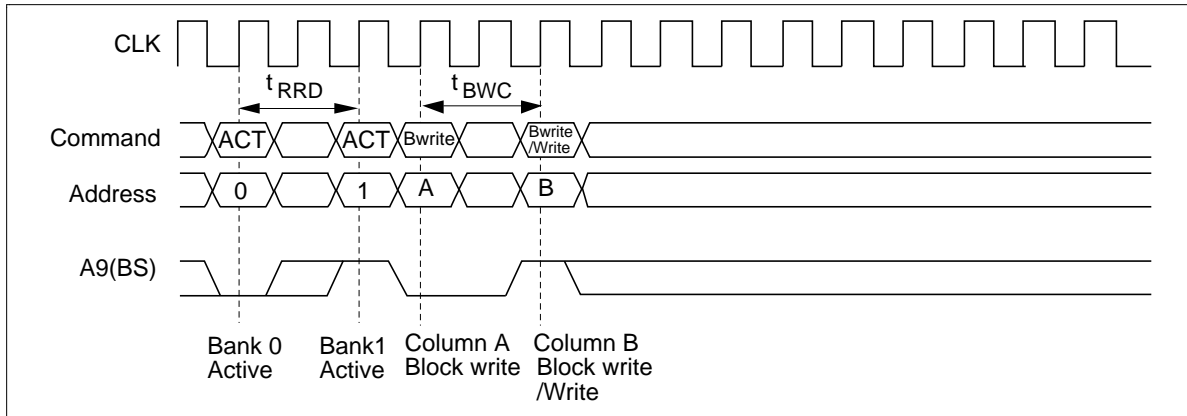
### Block Write Command to Write or Block Write Command Interval:

1. Operation for a column in the same row: It is necessary to take no less than  $t_{BWC}$  interval between a block write and another block write or the following write. If  $t_{CK}$  is less than  $t_{BWC}$ , NOP command should be issued for the cycle between a block write command and the following write or another block write command.



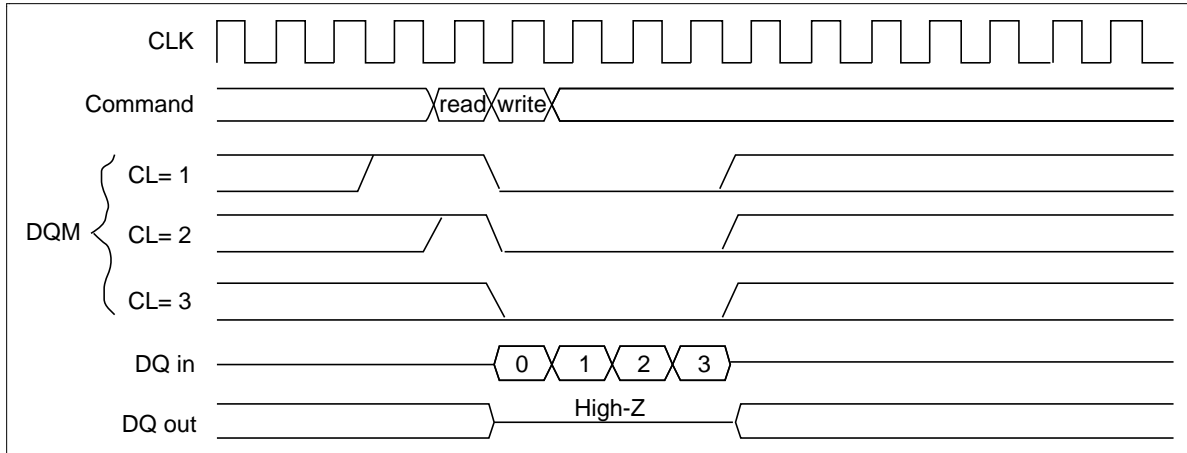
2. Operation for a column in other row of the same bank: It is necessary to execute a precharge command and a bank active command before the following write or another block write operation.

3. Operation for another bank: To execute the following write command or another block write command for another bank in active state,  $t_{BWC}$  interval to the next command is necessary. If another bank is in the idle state, bank active command should be executed. If  $t_{CK}$  is less than  $t_{BWC}$ , NOP command should be issued for the cycle between block write command and the following write or another block write command.



**Read Command to Write or Block Write Command Interval:**

1. Operation for a column in the same row: The write or the block write command following the preceding read command can be performed after an interval of no less than 1 cycle. To set DQ output High-Z when data are driven in, DQM must be used depending on  $\overline{\text{CAS}}$  latency as the timing shown below. Note that the latest write or block write command has the priority to the preceding read command, that is, any write or block write command can interrupt the preceding burst read operation to get valid data.



2. Operation for a column in other row of the same bank: It is necessary to execute a precharge command and a bank active command before executing the next write or another block write command.

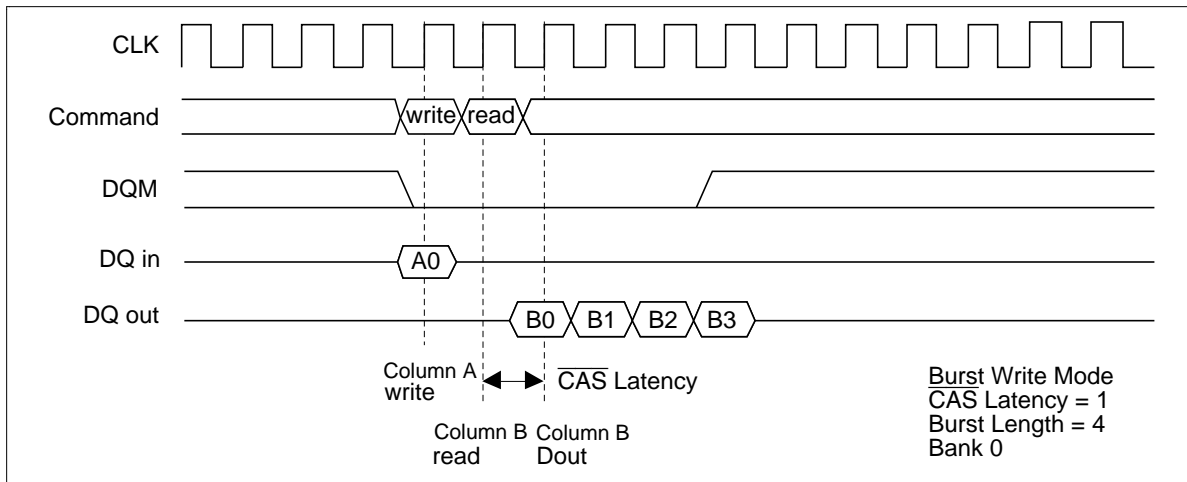
3. Operation for another bank: For another bank in active state, the following write or block write command can be executed from the next cycle after the preceding write command is issued. If another bank is in idle state, bank active command should be executed, prior to execute the following write or block write command.

## HM5283206 Series

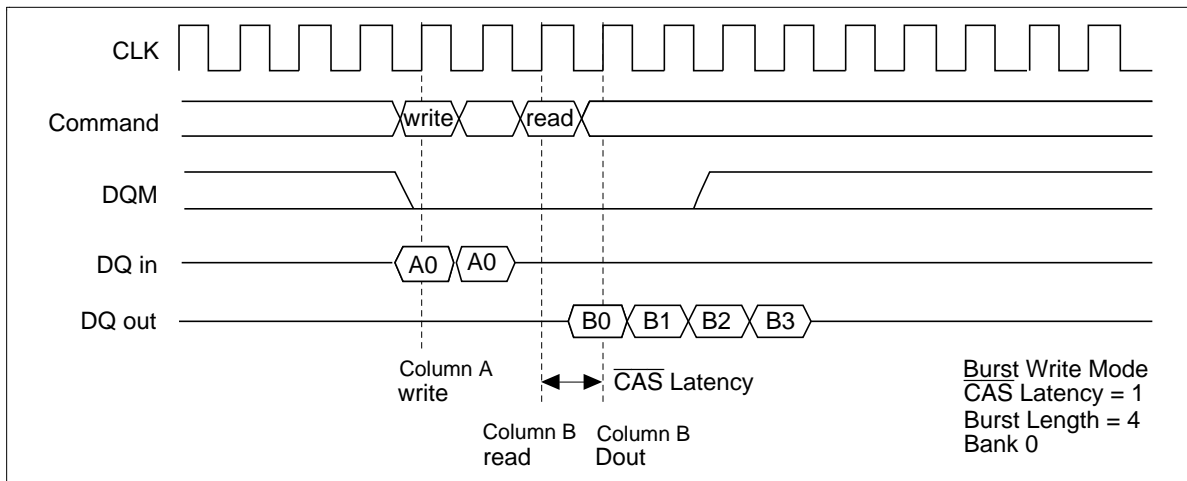
### Write Command to Read Command Interval:

1. Operation for a column in the same row: The read command following the preceding write command can be performed after an interval of no less than 1 cycle. Note that the latest read command has the priority to the preceding writing command, that is, any read command can interrupt the preceding write operation to get valid data.

#### WRITE to READ Command Interval (1)



#### WRITE to READ Command Interval (2)



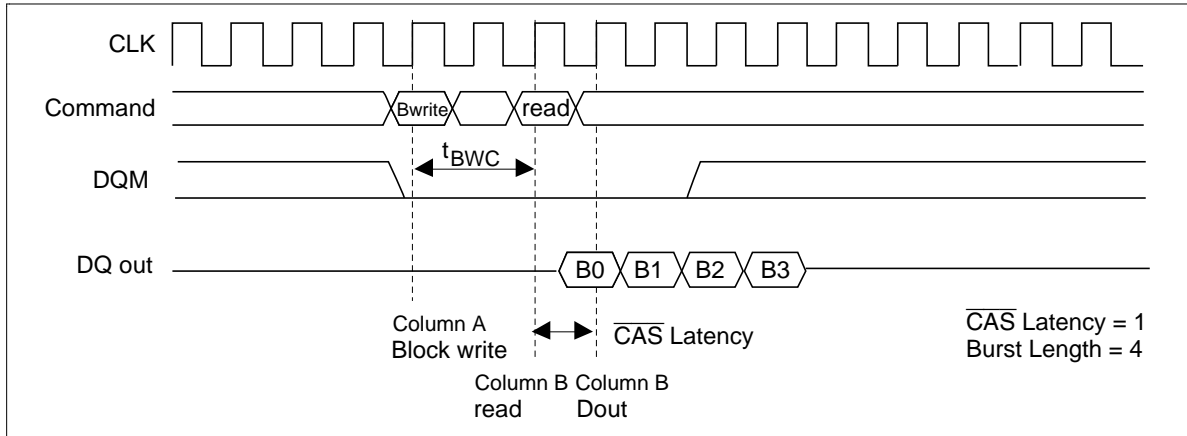
2. Operation for a column in other row of the same bank: To execute the following read command, it is necessary to execute a precharge command and a bank active command.

3. Operation for another bank: For another bank in active state, the following read command can be executed from the next cycle after the preceding write command is issued. If another bank is in idle state, a bank active command should be executed prior to execute the following read command.

**Block Write Command to Read Command Interval:**

1. Operation for a column in the same row : Within the same row, it is necessary to take no less than  $t_{BWC}$  between a block write and the following read command. If  $t_{CK}$  is less than  $t_{BWC}$ , NOP command should be issued for the cycle between a block write command and the following read command.

**Block Write Command to Read Command Interval**



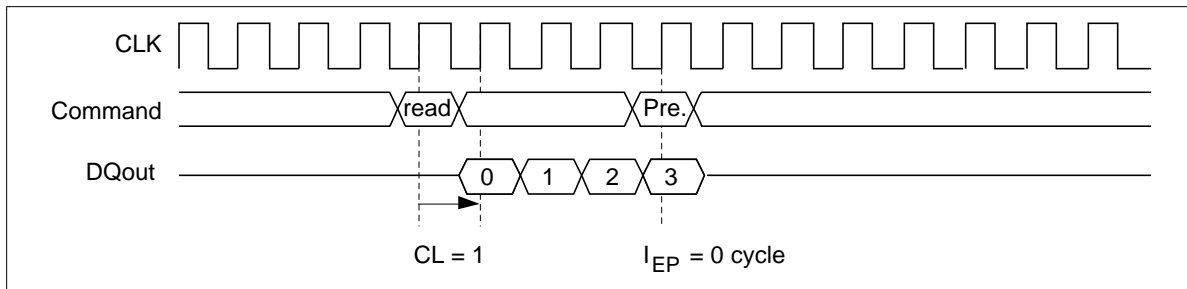
2. Operation for a column in other row of the same bank: It is necessary to execute a precharge command and a bank active command before the following write or another block write operation.
3. Operation for another bank: To execute a read command for another bank in active state,  $t_{BWC}$  interval to the next command is necessary. If another bank is in idle state, bank active command should be executed. If  $t_{CK}$  is less than  $t_{BWC}$ , NOP command should be issued for the cycle between a block write command and the following read command.

## HM5283206 Series

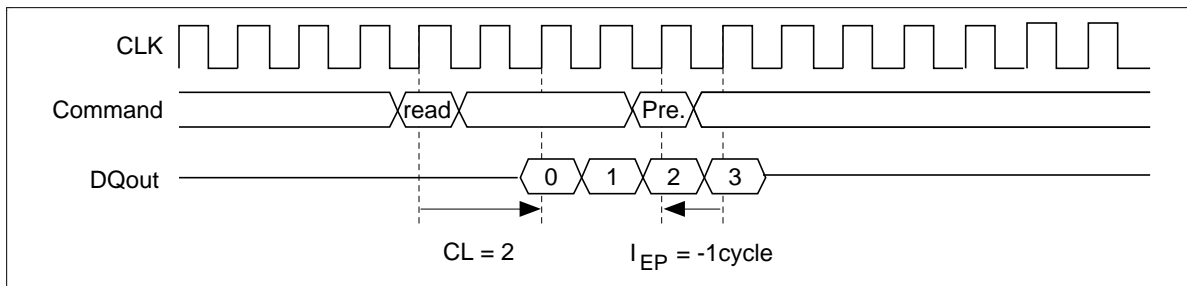
**Read Command to Precharge Command:** The minimum interval between read command and precharge command is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by  $t_{HZP}$ , there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by  $t_{EP}$  must be assured as an interval from the final data output to precharge command execution.

### READ to PRECHARGE Command Interval (Same Bank): Output All Data.

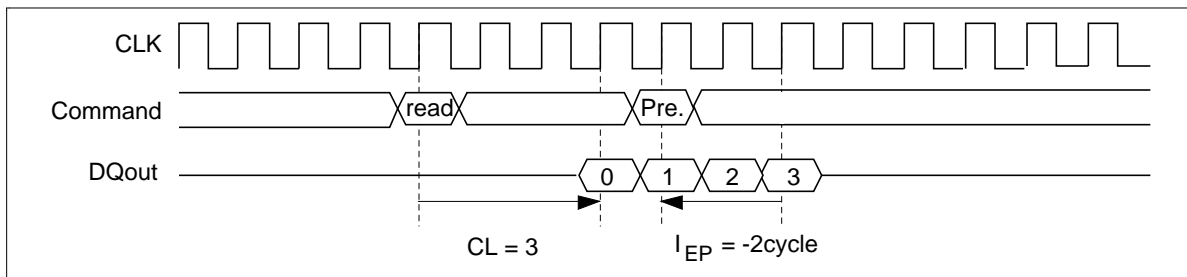
$\overline{\text{CAS}}$  Latency = 1, Burst Length = 4



$\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

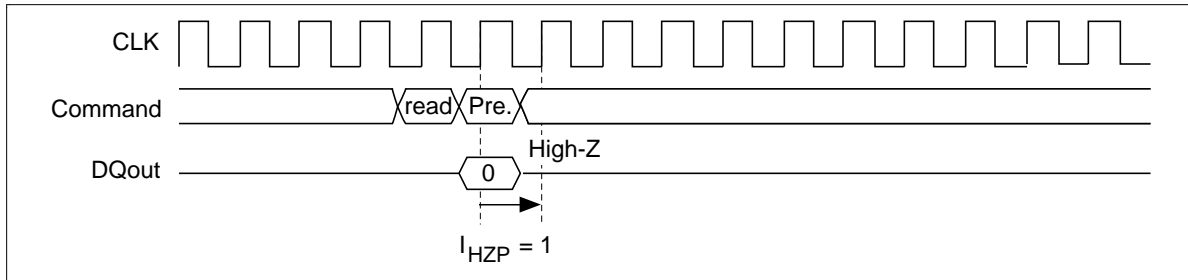


$\overline{\text{CAS}}$  Latency = 3, Burst Length = 4

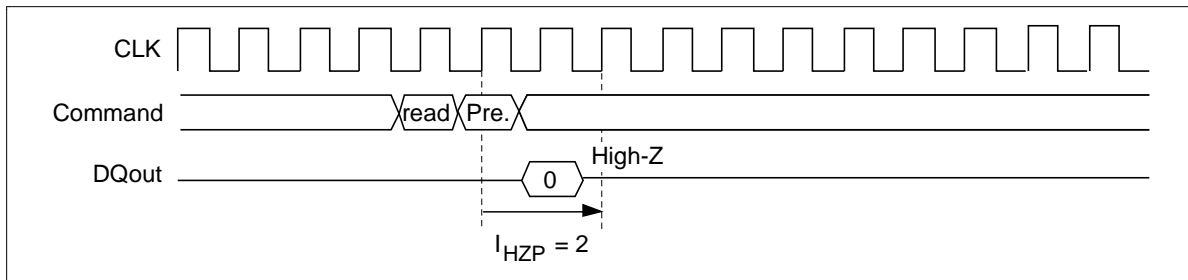


**READ to PRECHARGE Command Interval (Same Bank): Stop Output Data.**

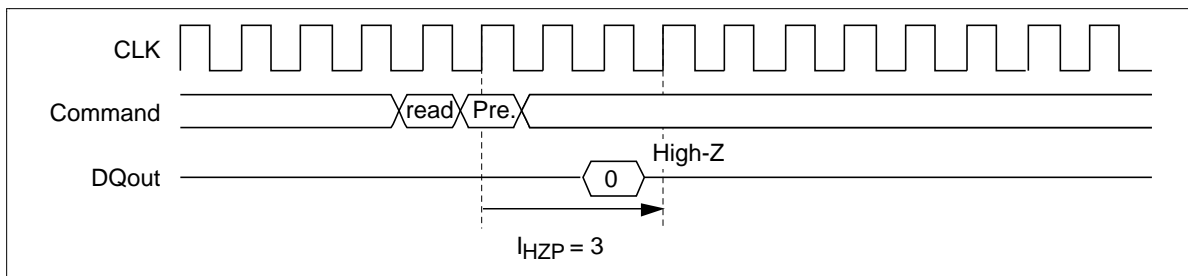
**CAS Latency = 1, Burst Length = 4**



**CAS Latency = 2, Burst Length = 4**



**CAS Latency = 3, Burst Length = 4**

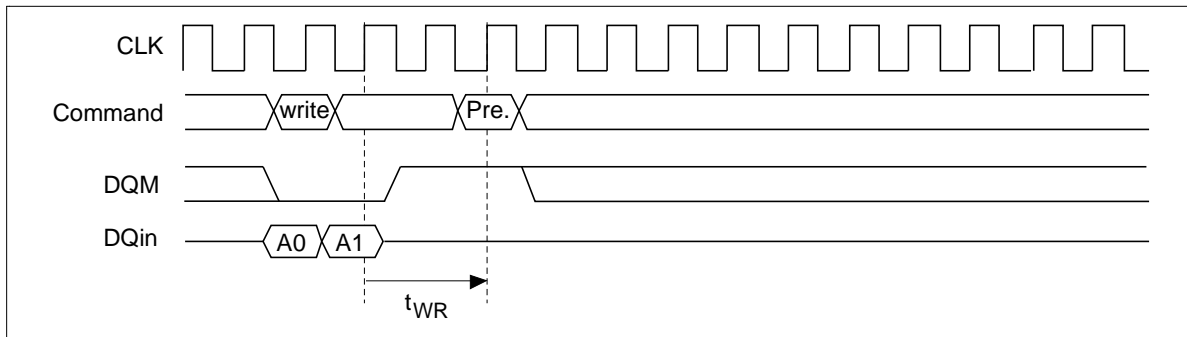


## HM5283206 Series

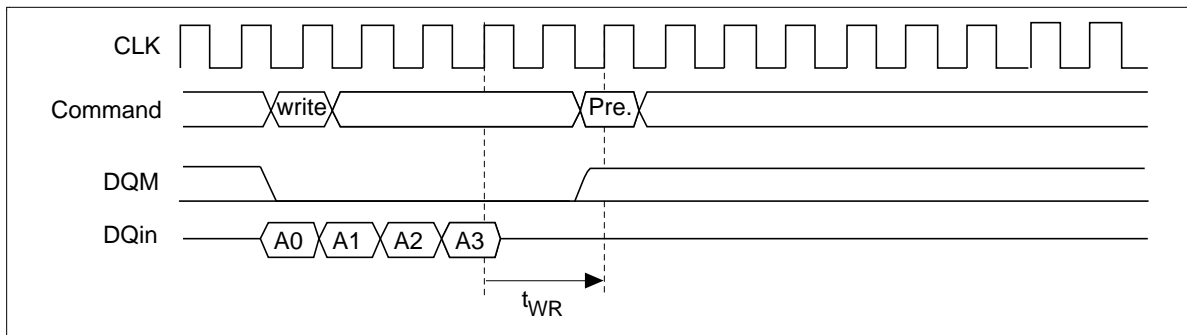
**Write Command to Precharge Command:** The minimum interval between a write command and the following precharge command is 1 cycle. However, if the burst write operation is not finished, input must be masked by means of DQM for the cycle defined by  $t_{WR}$ , for assurance.

### WRITE to Precharge Command Interval (Same Bank)

#### Burst Length = 4 (To Stop Write Operation)

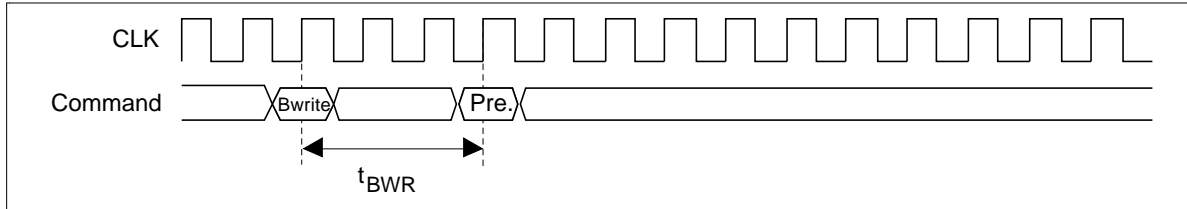


#### Burst Length = 4 (To Write All Data)



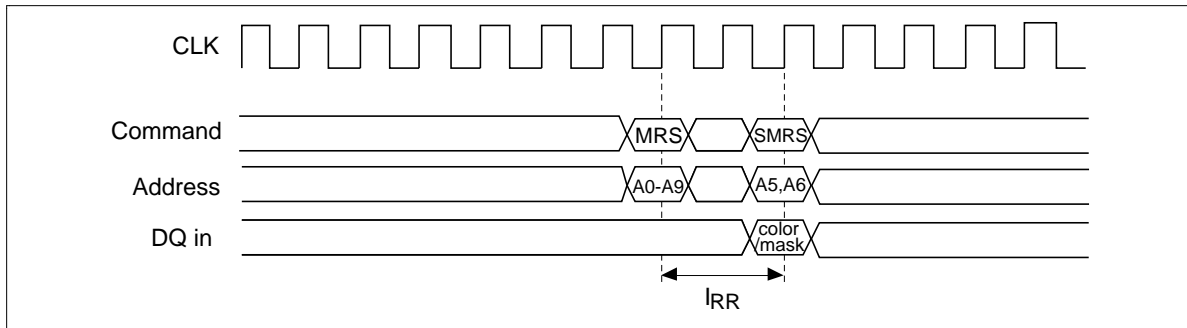
**Block Write Command to Precharge Command Interval:** The minimum interval between block write command and the following precharge command is  $t_{BWR}$ .

**Block Write to Precharge Command Interval (Same Bank)**



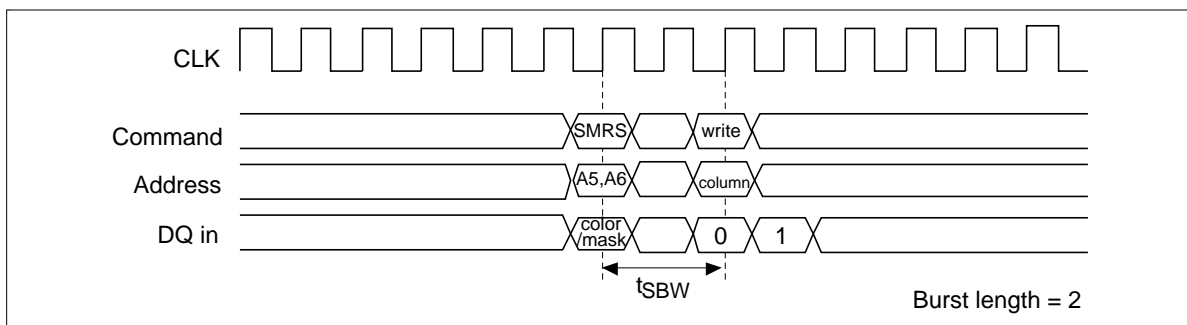
**Register set to register set interval:** The minimum interval between two successive register set commands (mode/special mode) is  $t_{RR}$ .

**Mode register set to special mode register interval**



**Special Mode Register Set to Block Write/Write Interval:** The minimum interval between a special mode register set and a block write/write is  $t_{SBW}$ .

**Special Mode Register Set to Burst Write Interval**



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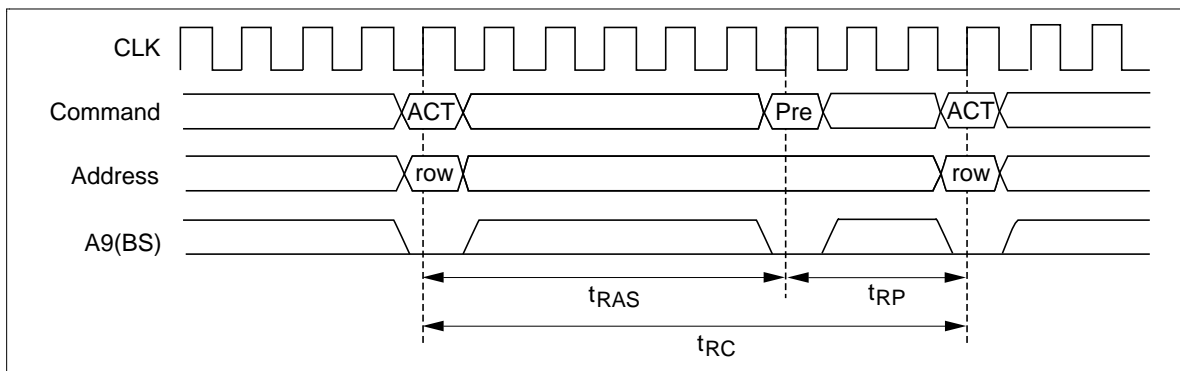
## HM5283206 Series

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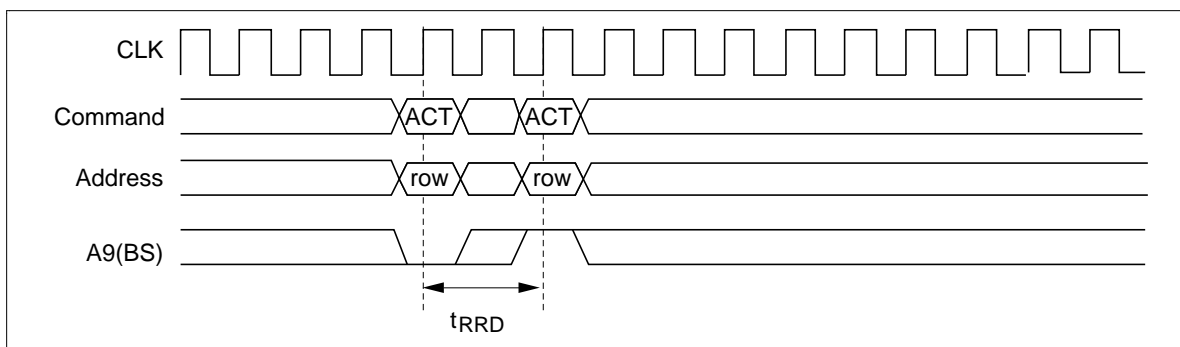
### Bank Active Command Interval:

1. Operation for the same bank: The interval between two bank-active commands must be no less than  $t_{RC}$ .
2. Operation for another bank: The interval between two bank-active commands must be no less than  $t_{RRD}$ .

### Bank Active to Bank Active for the Same Bank



### Bank Active to Bank Active for Another Bank



**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to $V_{SS}$	$V_T$	−1.0 to +4.6	V	1
Supply voltage relative to $V_{SS}$	$V_{DD}$	−1.0 to +4.6	V	
Short circuit output current	$I_{out}$	50	mA	
Power dissipation	$P_T$	1.0	W	
Operating temperature	$T_{opr}$	0 to +70	°C	
Storage temperature	$T_{stg}$	−55 to +125	°C	

Note: 1.  $V_{IH}(\text{max}) = 5.75 \text{ V}$  for pulse width  $\leq 5 \text{ ns}$

**Recommended DC Operating Conditions ( $T_a = 0 \text{ to } +70^\circ\text{C}$ )**

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	$V_{DD}, V_{DDQ}$	3.0	3.6	V	1
	$V_{SS}, V_{SSQ}$	0	0	V	
Input high voltage	$V_{IH}$	2.0	4.6	V	1, 2
Input low voltage	$V_{IL}$	−0.3	0.8	V	1, 3

Notes: 1. All voltage referred to  $V_{SS}$   
 2.  $V_{IH}(\text{max}) = 5.5 \text{ V}$  for pulse width  $\leq 5 \text{ ns}$   
 3.  $V_{IL}(\text{min}) = -1.0 \text{ V}$  for pulse width  $\leq 5 \text{ ns}$

## HM5283206 Series

**DC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{DD}$ ,  $V_{DD}Q = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}$ ,  $V_{SS}Q = 0\text{ V}$ )

		HM5283206								
		-8		-10		-12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Note
Operating current	$I_{CC1}$	—	210	—	180	—	150	mA	Burst length = 1 $t_{RC} = \text{min}$ , $CL = 3$ $t_{CK} = \text{min}$	1
Standby current (Bank Disable)	$I_{CC2}$	—	5	—	5	—	5	mA	$CKE = V_{IL}$ , $t_{CK} = \text{min}$	
		—	3	—	3	—	3	mA	$CKE = V_{IL}$ $CLK = V_{IL}$ or $V_{IH}$ Fixed	
		—	95	—	75	—	60	mA	$CKE = V_{IH}$ , $t_{CK} = \text{min}$ NOP command	
Active standby current (Bank active)	$I_{CC3}$	—	15	—	10	—	10	mA	$CKE = V_{IL}$ , $t_{CK} = \text{min}$ , DQ = High-Z	1
		—	100	—	80	—	65	mA	$CKE = V_{IH}$ , $t_{CK} = \text{min}$ , NOP command DQ = High-Z	
Burst operating current (CL = 1)	$I_{CC4}$	—	220	—	170	—	140	mA	$t_{CK} = \text{min}$ , $BL = 4$ , 2 bank operation	1
(CL = 2)	$I_{CC4}$	—	280	—	240	—	200	mA		
(CL = 3)	$I_{CC4}$	—	330	—	280	—	240	mA		
Refresh current	$I_{CC5}$	—	190	—	150	—	120	mA	$t_{RC} = \text{min}$ , $CL = 3$ $t_{CK} = \text{min}$	
Self refresh current	$I_{CC6}$	—	4	—	4	—	4	mA	$V_{IH} \geq V_{DD} - 0.2$ $V_{IL} \leq 0.2\text{ V}$	
Block write operating current	$I_{CC7}$	—	200	—	160	—	130	mA	$t_{CK} = \text{min}$ , $CL = 3$ 1 bank operation, $t_{RC} = 150\text{ ns}$	
Input leakage current	$I_{LI}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0 \leq V_{in} \leq V_{DD}$	
Output leakage current	$I_{LO}$	-10	10	-10	10	-10	10	$\mu\text{A}$	$0 \leq V_{out} \leq V_{DD}$ DQ = disable	
Output high voltage	$V_{OH}$	2.4	—	2.4	—	2.4	—	V	$I_{OH} = -2\text{ mA}$	
Output low voltage	$V_{OL}$	—	0.4	—	0.4	—	0.4	V	$I_{OL} = 2\text{ mA}$	

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}(\text{max})$  is specified on condition that all output pins are floated.

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{DD}$ ,  $V_{DD}Q = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{I1}$	—	5	pF	1
Input capacitance (Signals)	$C_{I2}$	—	5	pF	1
Output capacitance (DQ)	$C_O$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $DQM = V_{IH}$  to disable Dout.

## HM5283206 Series

**AC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{DD}$ ,  $V_{DD}Q = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}$ ,  $V_{SS}Q = 0\text{ V}$ )

		HM5283206							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock cycle time (CL = 1)	t <sub>CK</sub>	24	—	30	—	36	—	ns	1
(CL = 2)	t <sub>CK</sub>	12	—	15	—	18	—	ns	
(CL = 3)	t <sub>CK</sub>	8	—	10	—	12	—	ns	
CLK high pulse width	t <sub>CH</sub>	3	—	3	—	4	—	ns	1
CLK low pulse width	t <sub>CL</sub>	3	—	3	—	4	—	ns	1
Access time from CLK (CL = 1)	t <sub>AC</sub>	—	23	—	28	—	32	ns	1, 2
(CL = 2)	t <sub>AC</sub>	—	11	—	13	—	15	ns	
(CL = 3)	t <sub>AC</sub>	—	7	—	8	—	10	ns	
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	23	—	28	—	32	ns	1, 2
Data-out hold time	t <sub>OH</sub>	3	—	3	—	3	—	ns	1
CLK to data-out low impedance	t <sub>LZ</sub>	0	—	0	—	0	—	ns	1
CLK to data-out high impedance (CL = 1)	t <sub>HZ</sub>	—	11	—	13	—	15	ns	1, 3
(CL = 2,3)	t <sub>HZ</sub>	—	6	—	7	—	9	ns	
Data-in setup time	t <sub>DS</sub>	2.5	—	3	—	3.5	—	ns	1
Data-in hold time	t <sub>DH</sub>	1	—	1	—	1.5	—	ns	1
Address setup time	t <sub>AS</sub>	2.5	—	3	—	3.5	—	ns	1
Address hold time	t <sub>AH</sub>	1	—	1	—	1.5	—	ns	1
CKE setup time	t <sub>CKS</sub>	2.5	—	3	—	3.5	—	ns	1, 4
CKE hold time	t <sub>CKH</sub>	1	—	1	—	1.5	—	ns	1, 4
Command ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , DQM, DSF) setup time	t <sub>CMS</sub>	2.5	—	3	—	3.5	—	ns	1
Command ( $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , DQM, DSF) hold time	t <sub>CMH</sub>	1	—	1	—	1.5	—	ns	1
Refresh/active to refresh/active command period	t <sub>RC</sub>	72	—	90	—	108	—	ns	1
Active to precharge on full page mode	t <sub>RASC</sub>	—	120000	—	120000	—	120000	ns	1
Active to precharge command period	t <sub>RAS</sub>	48	120000	60	120000	72	120000	ns	1
Active command to column command	t <sub>RCD</sub>	24	—	30	—	36	—	ns	1

## HM5283206 Series

**AC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{DD}$ ,  $V_{DD}Q = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS}$ ,  $V_{SS}Q = 0\text{ V}$ )  
(cont)

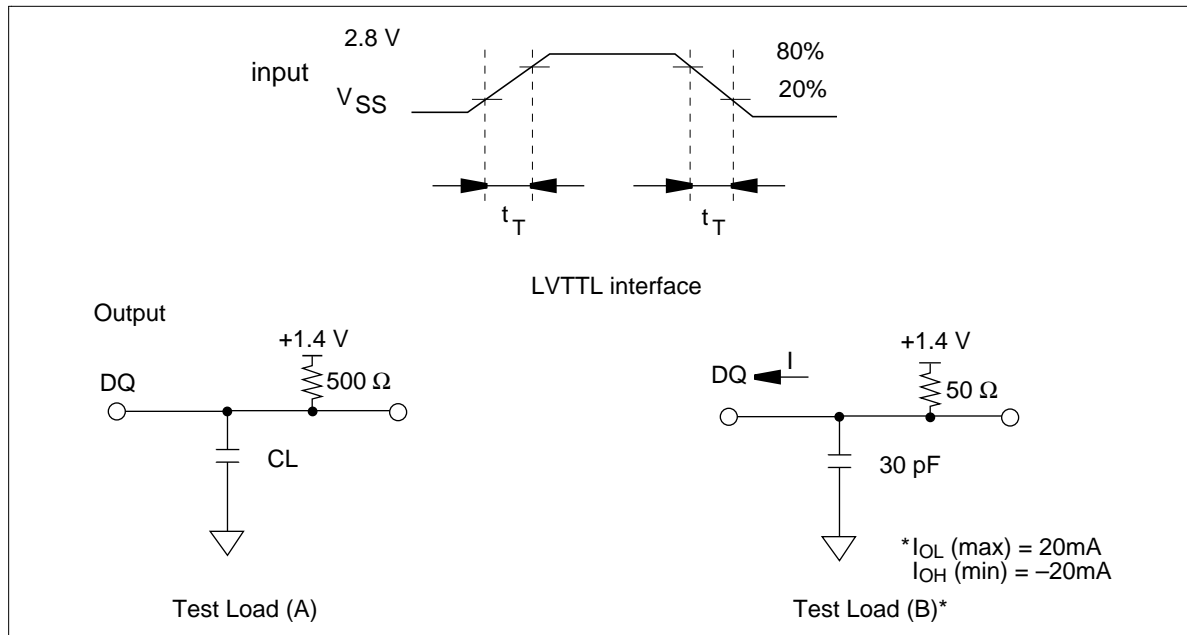
		HM5283206							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Precharge to active command period	t <sub>RP</sub>	24	—	30	—	36	—	ns	1
The last data-in to precharge lead time (CL = 1)	t <sub>WR</sub>	12	—	15	—	18	—	ns	1
(CL = 2)	t <sub>WR</sub>	12	—	15	—	18	—	ns	
(CL = 3)	t <sub>WR</sub>	16	—	20	—	24	—	ns	
Block write to precharge lead time (CL = 1)	t <sub>BWR</sub>	24	—	30	—	34	—	ns	1
(CL = 2)	t <sub>BWR</sub>	24	—	30	—	34	—	ns	
(CL = 3)	t <sub>BWR</sub>	24	—	30	—	36	—	ns	
Active (a) to active (b) command period	t <sub>RRD</sub>	16	—	20	—	24	—	ns	1
Register set to active command	t <sub>RSC</sub>	16	—	20	—	24	—	ns	1
Block write cycle time	t <sub>BWC</sub>	16	—	20	—	24	—	ns	1
Special mode register set to column command	t <sub>SBW</sub>	16	—	20	—	24	—	ns	1
Transition time (rise to fall)	t <sub>T</sub>	1	5	1	5	1	5	ns	
Refresh period	t <sub>REF</sub>	—	16	—	16	—	16	ms	

- Notes: 1. AC measurement assumes  $t_T = 1\text{ ns}$ . Reference level for timing of input signals is 1.4 V.  
Test load (A) is used with CL = 30 pF in general except for the measurement of access time (note2) and  $t_{HZ}$  (note3).
2. Access time is measured at 1.4 V. Test load (B) is used with current source.
3.  $t_{HZ}$  (max) defines the time at which the outputs achieves  $\pm 200\text{ mV}$ . Test load (A) is used with CL = 5 pF and with current source.
4. When Active Suspend Exit, Power Down Exit or Self Refresh Exit is executed.  
CKE should be kept "H" more than 1 cycle from these Exit cycles.

## HM5283206 Series

### Test Conditions

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures



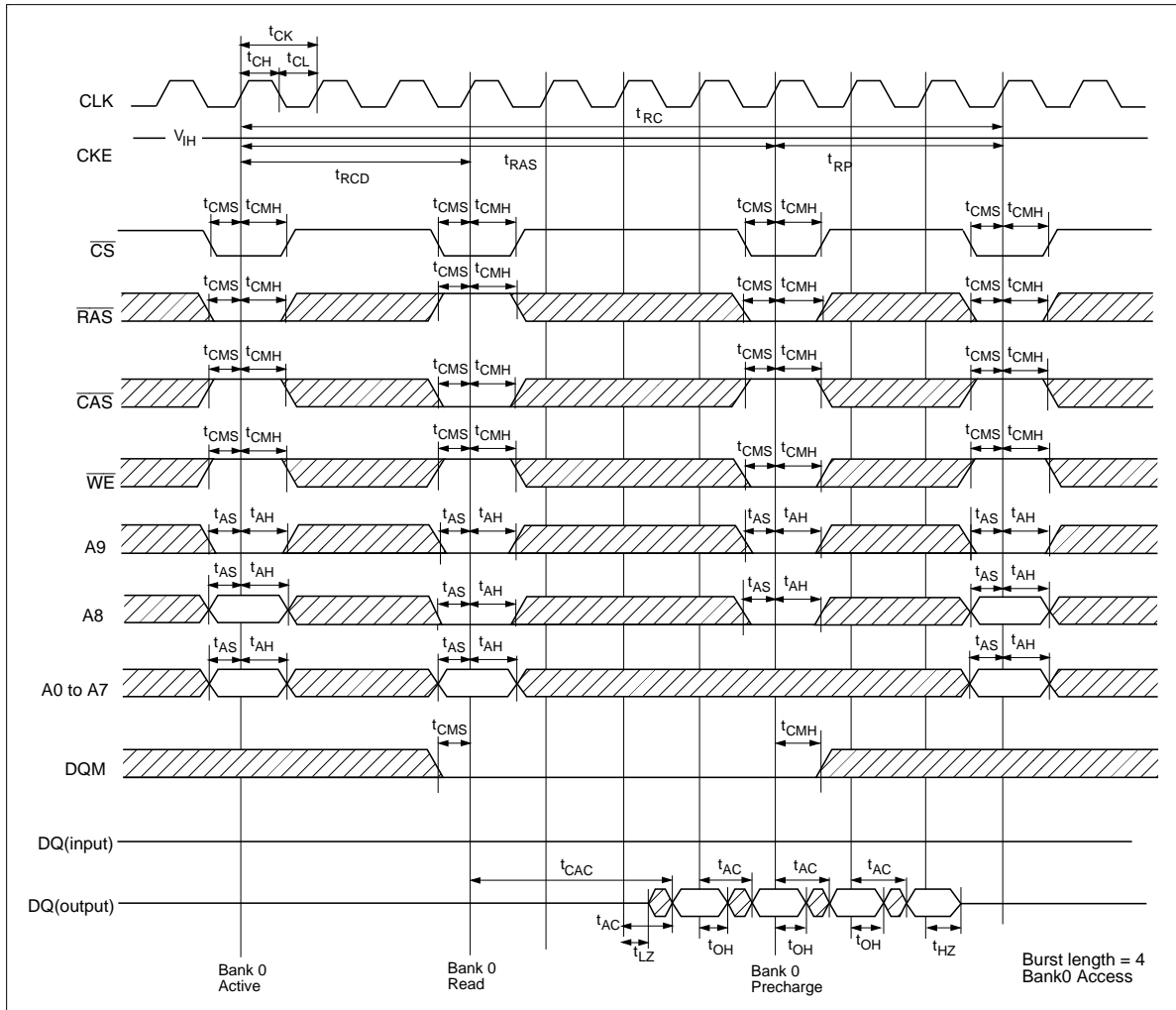
**Relationship Between Frequency and Minimum Latency**

		HM5283206									
Parameter		-8			-10			-12			
CL		3	2	1	3	2	1	3	2	1	
t <sub>CK</sub> (ns)	Symbol	8	12	24	10	15	30	12	18	36	Notes
Last data in to active command (Auto precharge, same bank)	I <sub>APW</sub>	5	3	2	5	3	2	5	3	2	
Block write to active command (Auto precharge, same bank)	I <sub>APBW</sub>	6	4	2	6	4	2	6	4	2	
Precharge command to high impedance	I <sub>HZP</sub>	3	2	1	3	2	1	3	2	1	
Last data out to active command (Auto precharge, same bank)	I <sub>APR</sub>	1	1	1	1	1	1	1	1	1	
Last data out to precharge	I <sub>EP</sub>	−2	−1	0	−2	−1	0	−2	−1	0	
Column command to column command	I <sub>CCD</sub>	1	1	1	1	1	1	1	1	1	
Write command to data in latency	I <sub>WCD</sub>	0	0	0	0	0	0	0	0	0	
DQM to data in	I <sub>DID</sub>	0	0	0	0	0	0	0	0	0	
DQM to data out	I <sub>DOD</sub>	2	2	2	2	2	2	2	2	2	
CKE to CLK disable	I <sub>CLE</sub>	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	I <sub>BSR</sub>	2	1	0	2	1	0	2	1	0	
Burst stop to output high impedance	I <sub>BSH</sub>	3	2	1	3	2	1	3	2	1	
Burst stop to write data ignore	I <sub>BSW</sub>	0	0	0	0	0	0	0	0	0	
MRS to data in latency	I <sub>MSD</sub>	0	0	0	0	0	0	0	0	0	
SMRS to data in latency	I <sub>SSD</sub>	0	0	0	0	0	0	0	0	0	
Register set to register set	I <sub>RR</sub>	2	2	1	2	2	1	2	2	1	

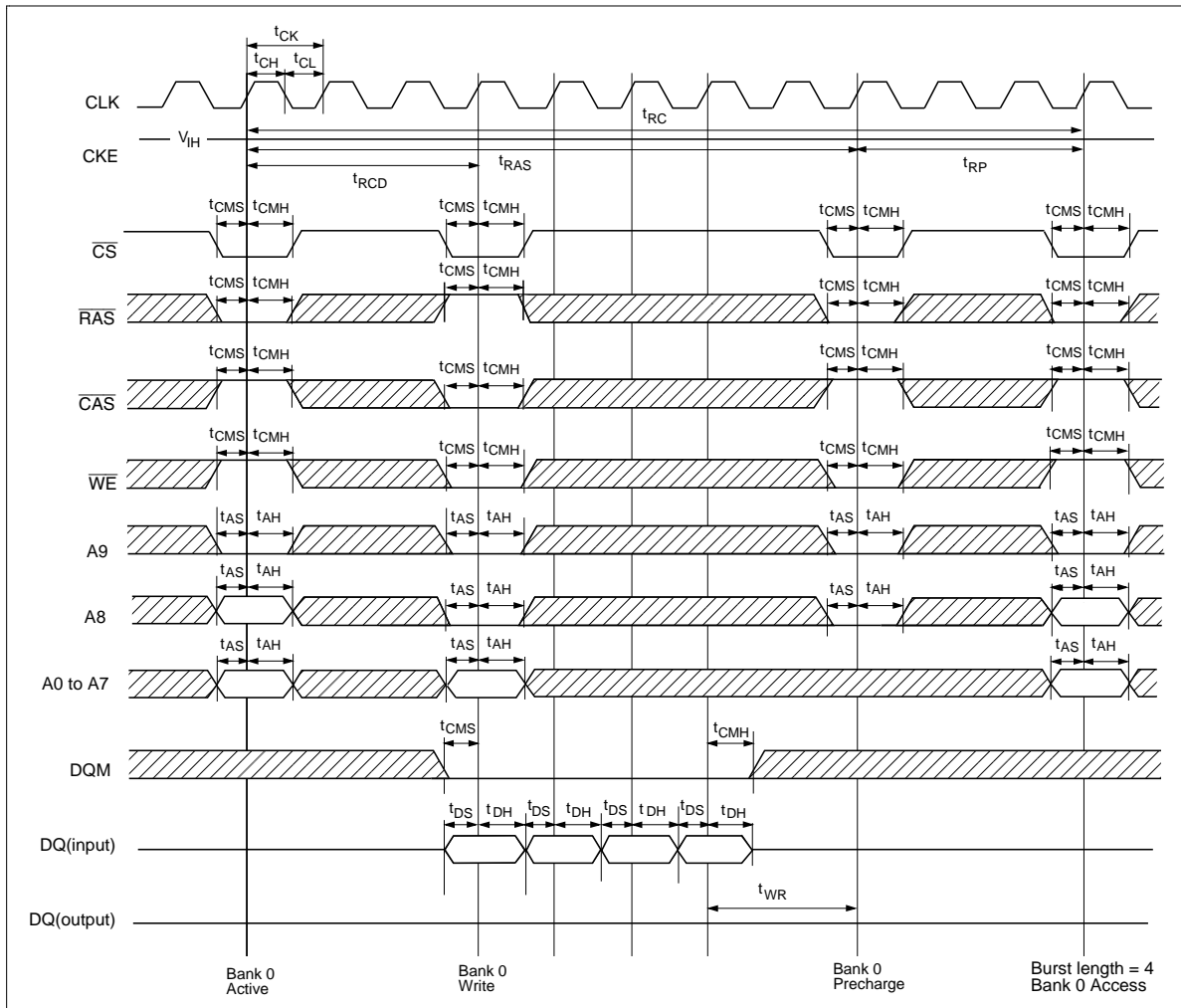
# HM5283206 Series

## Timing Waveforms

### Read Cycle

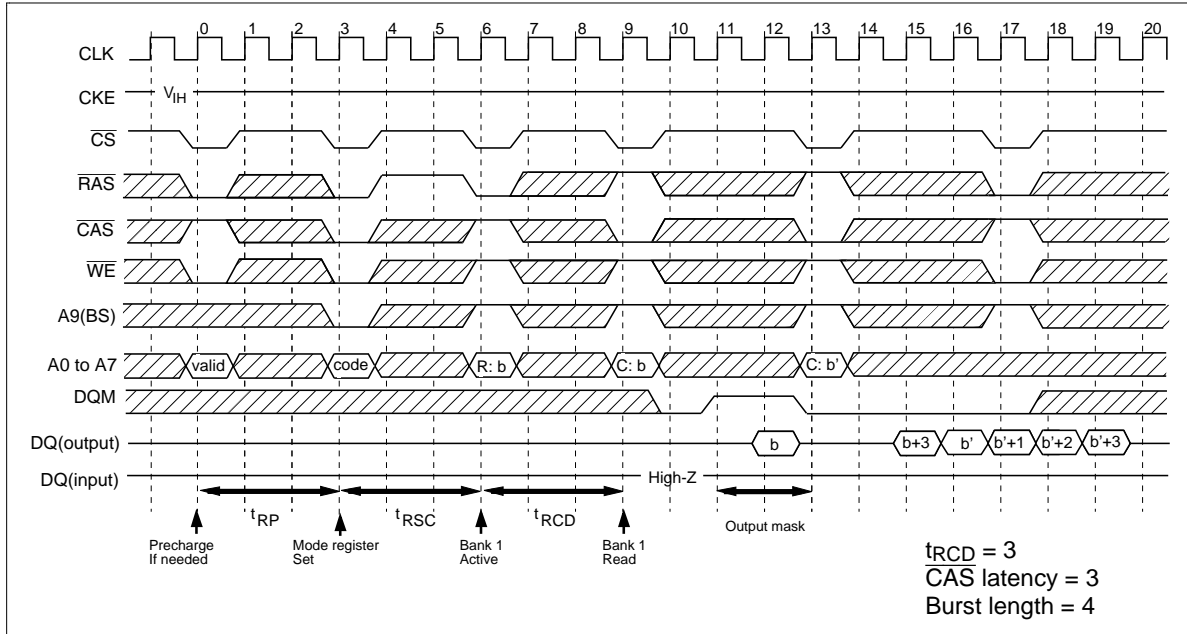


# Write Cycle

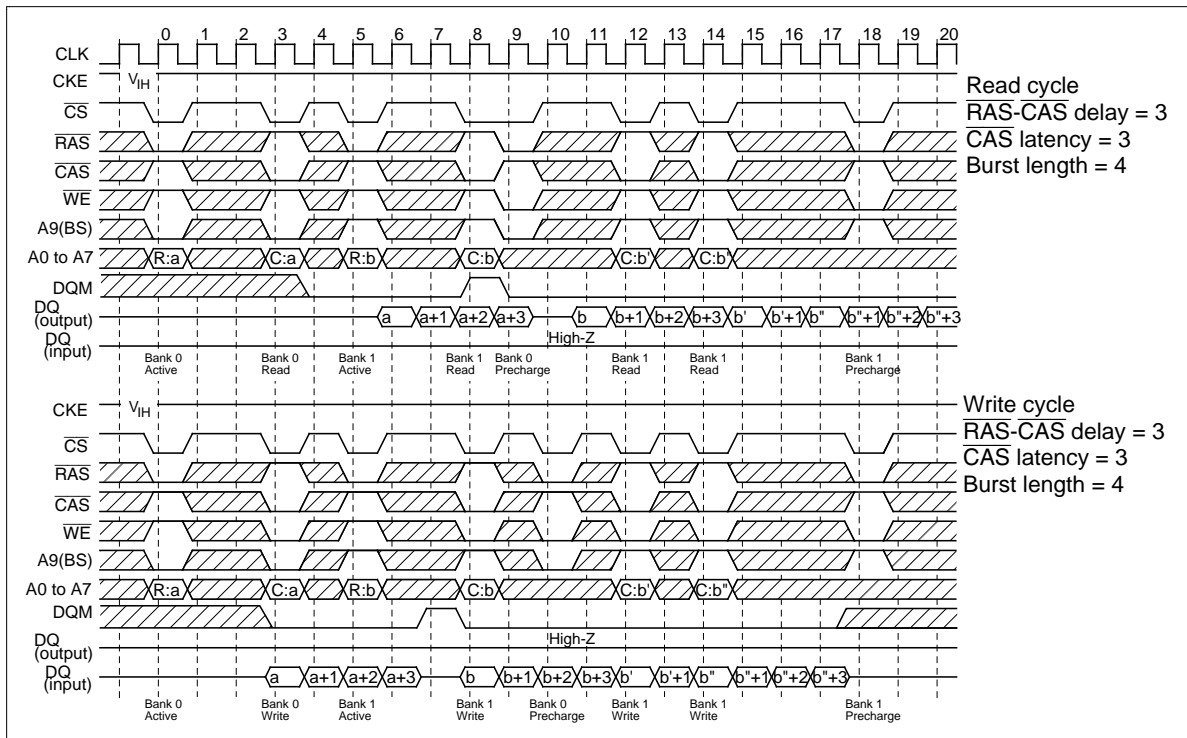


## HM5283206 Series

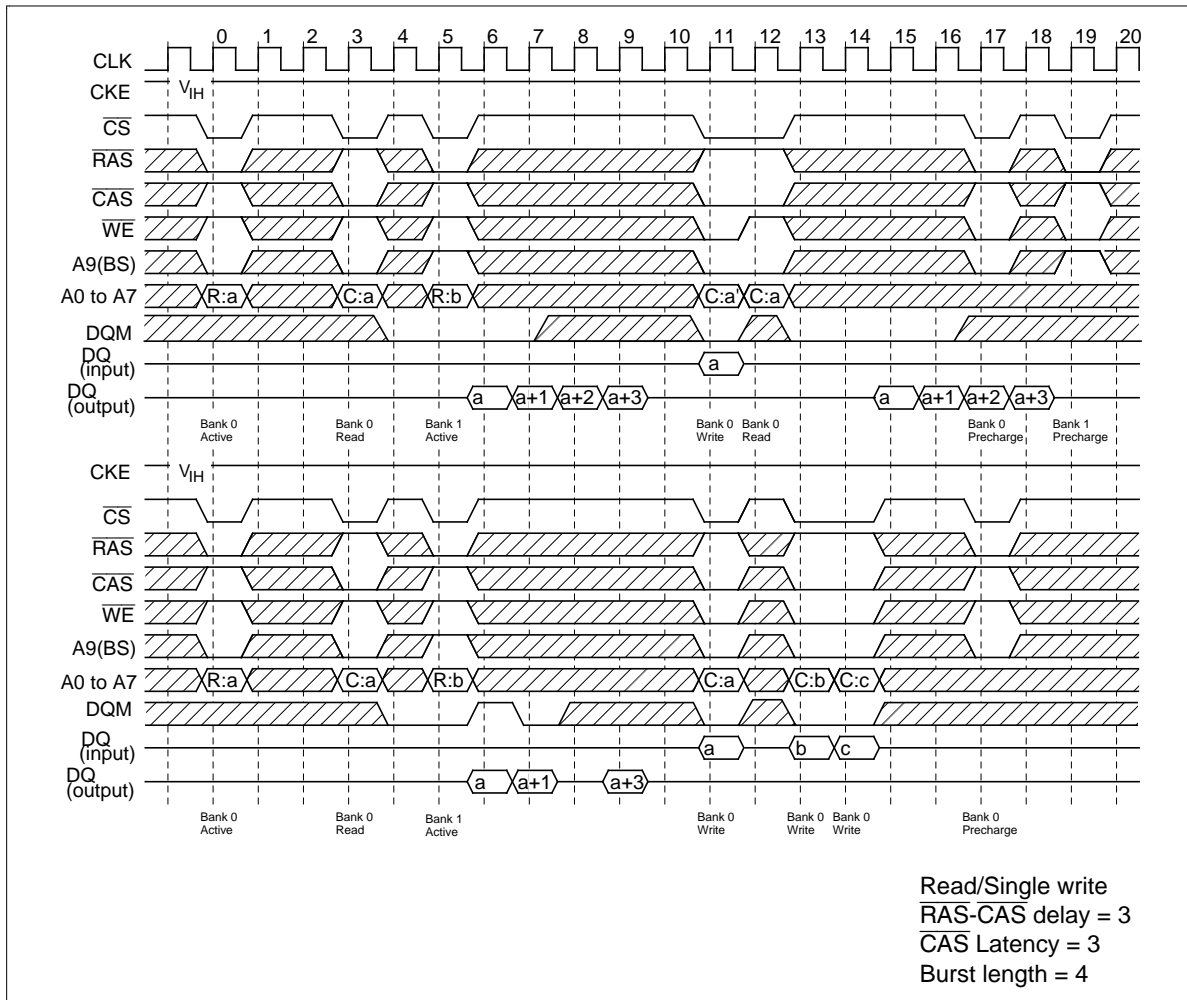
### Mode Register Set Cycle



### Read Cycle/Write Cycle

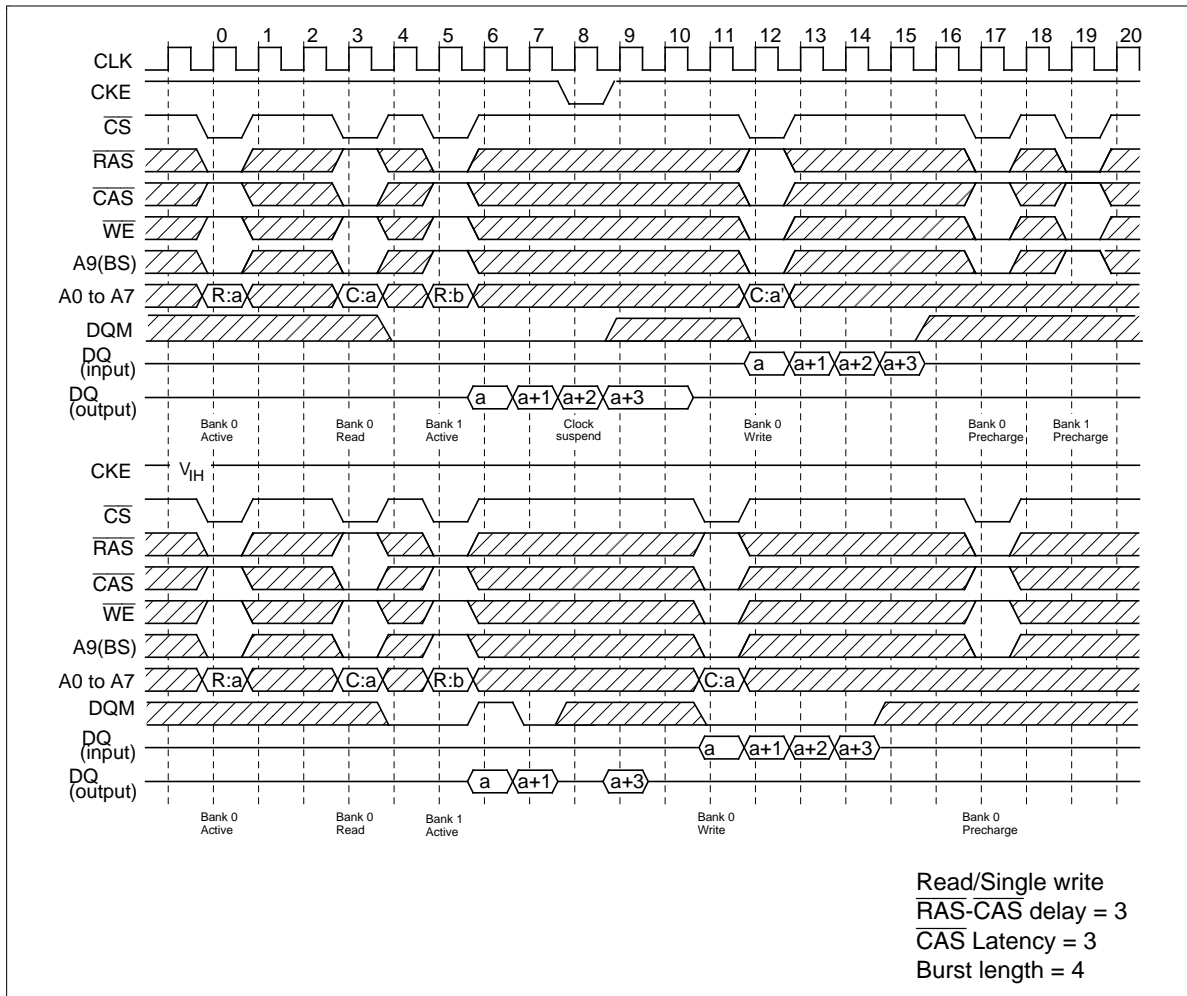


Read/Single Write Cycle

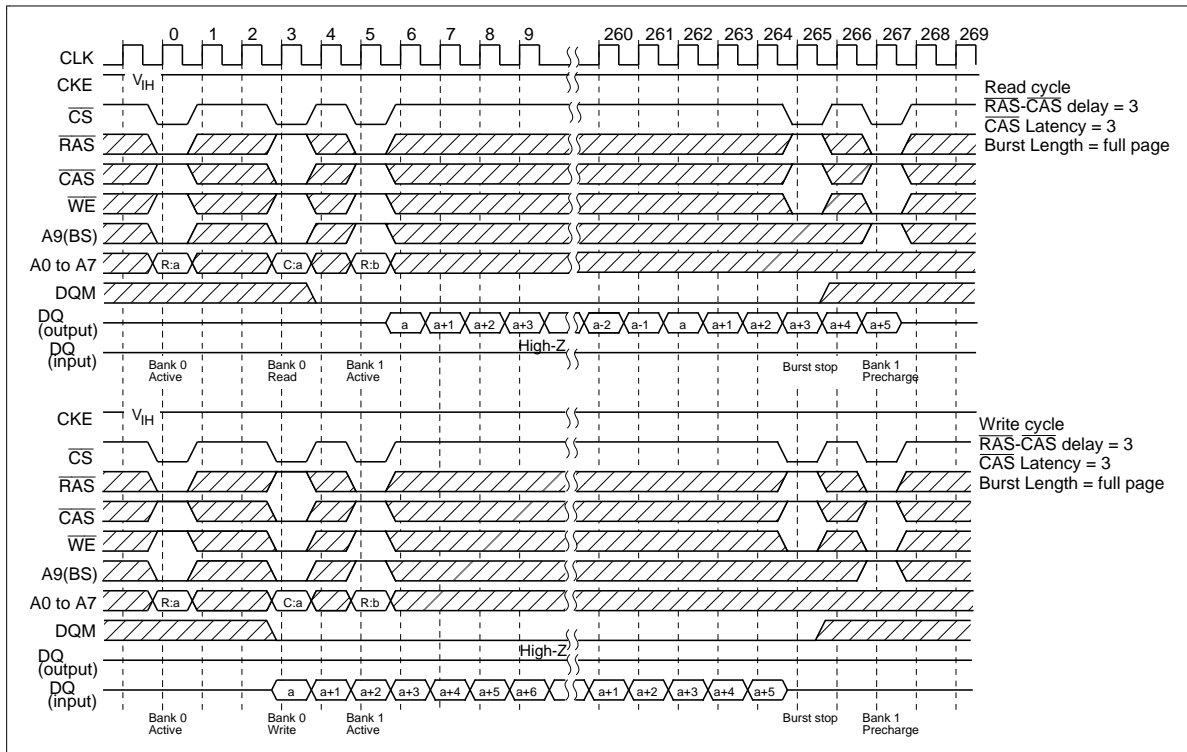


## HM5283206 Series

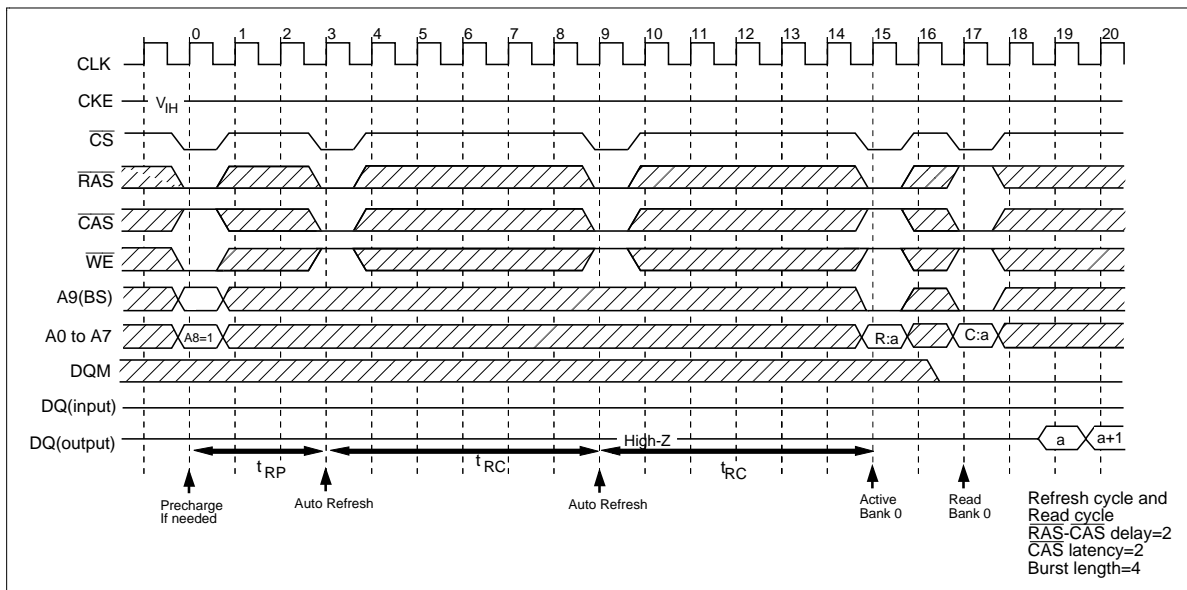
### Read/Burst Write Cycle



### Full Page Read/Write Cycle

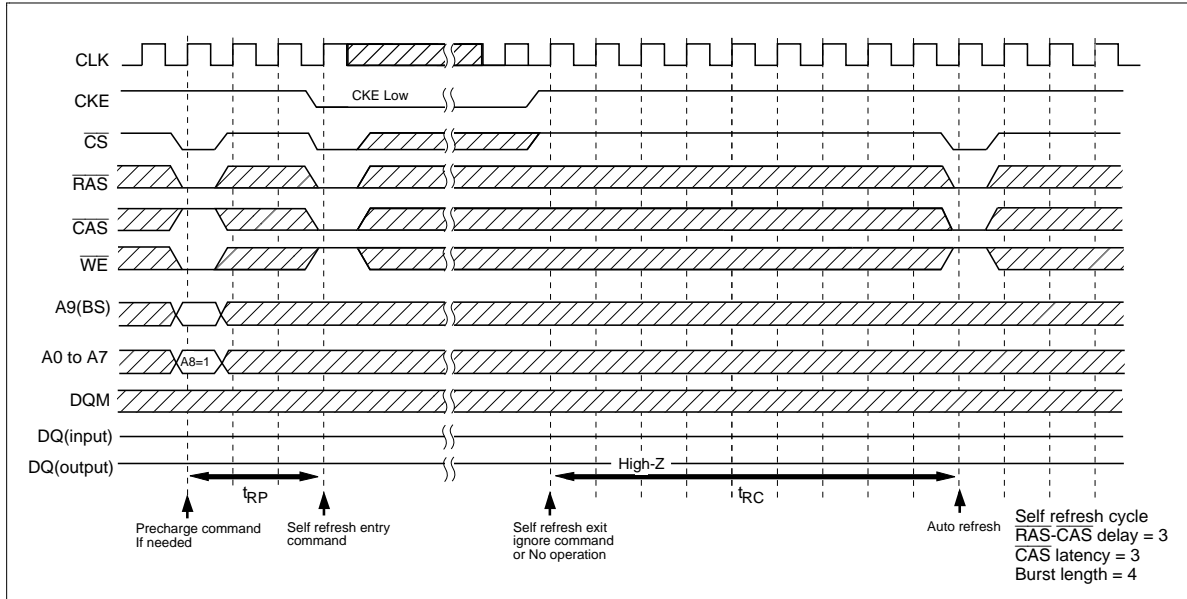


### Auto Refresh Cycle

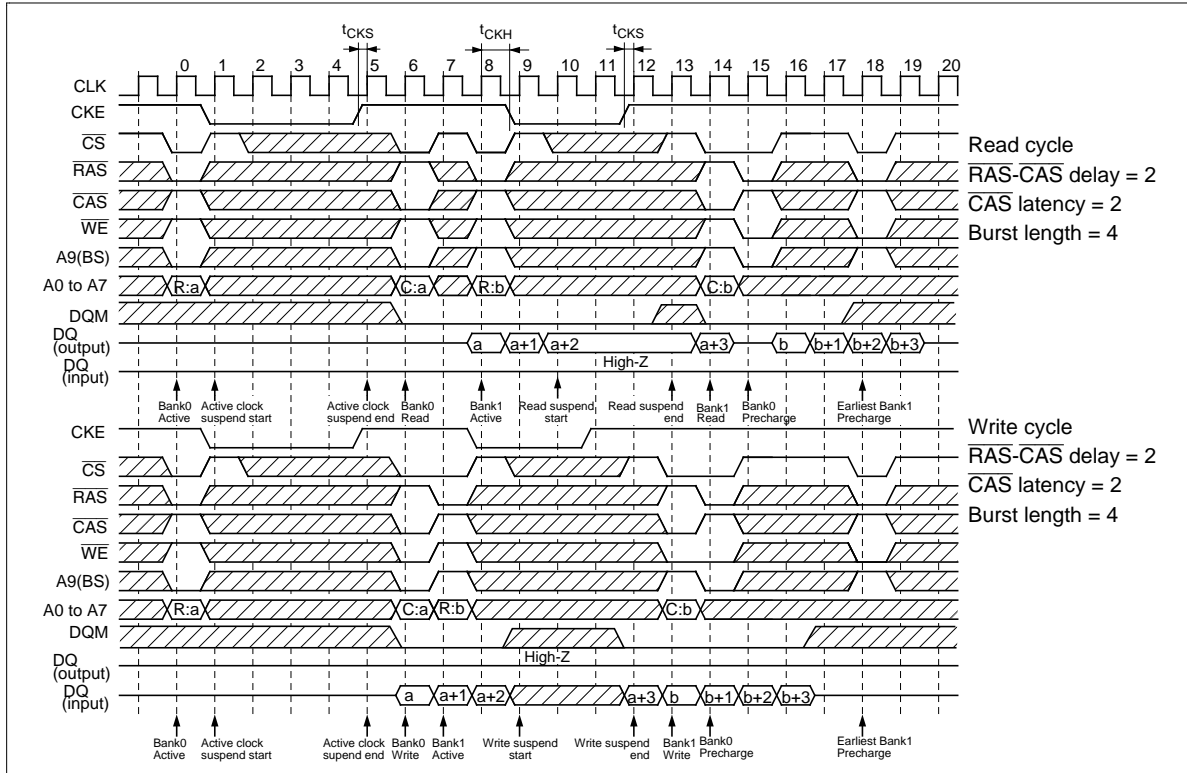


## HM5283206 Series

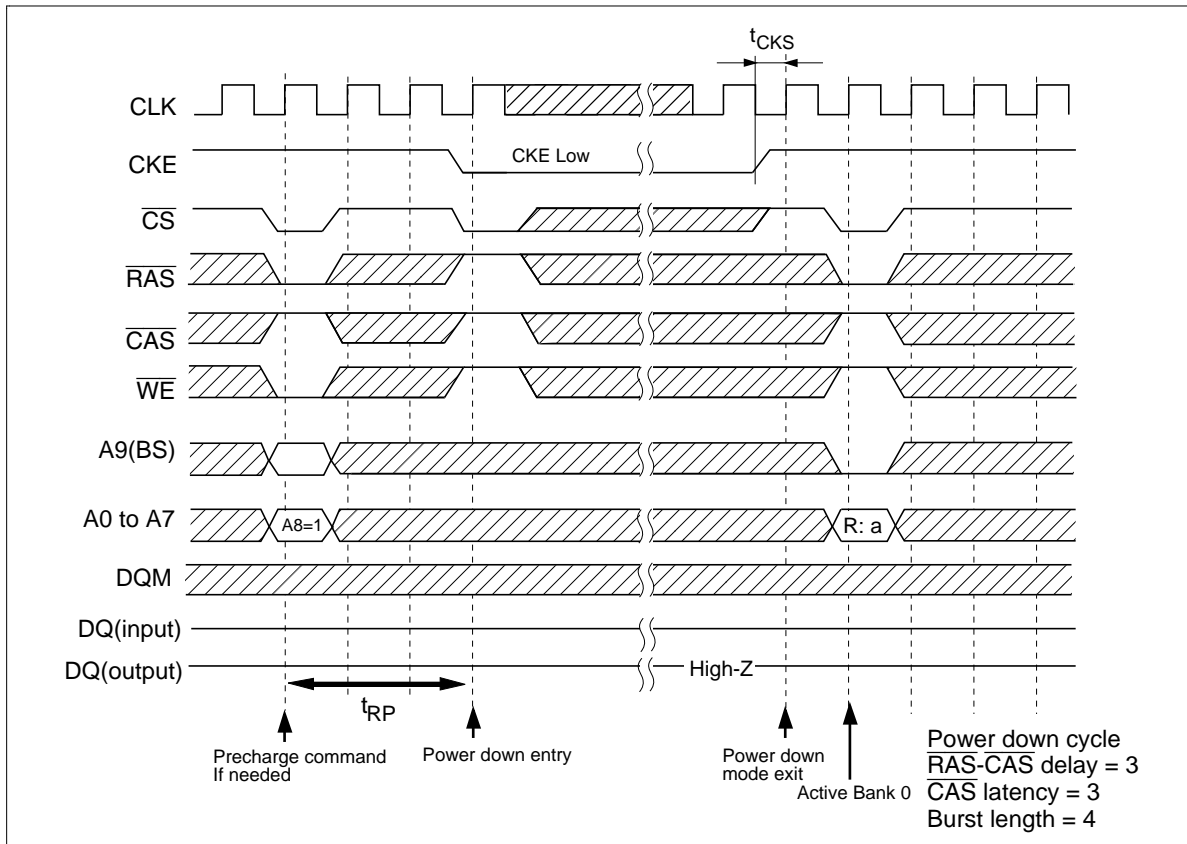
### Self Refresh Cycle



### Clock Suspend Mode

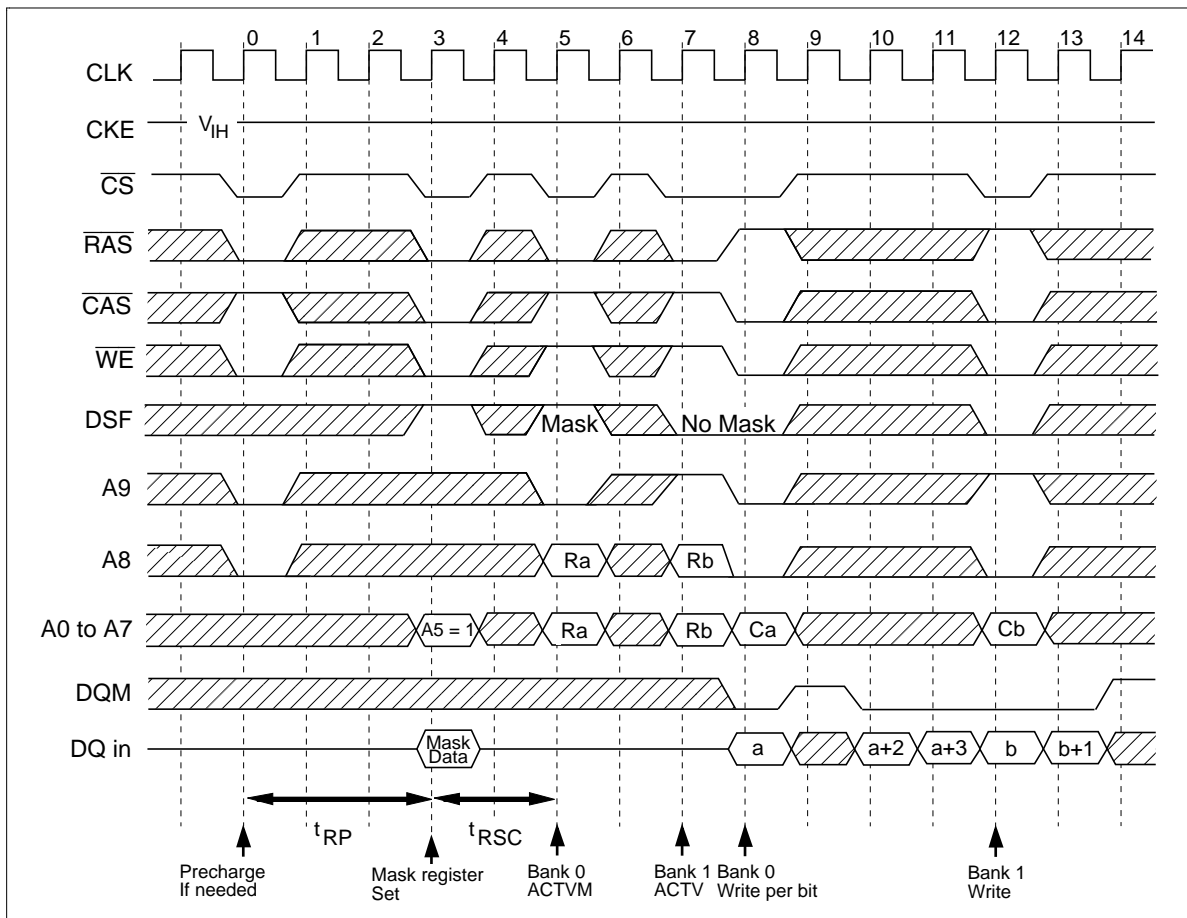


### Power Down Mode

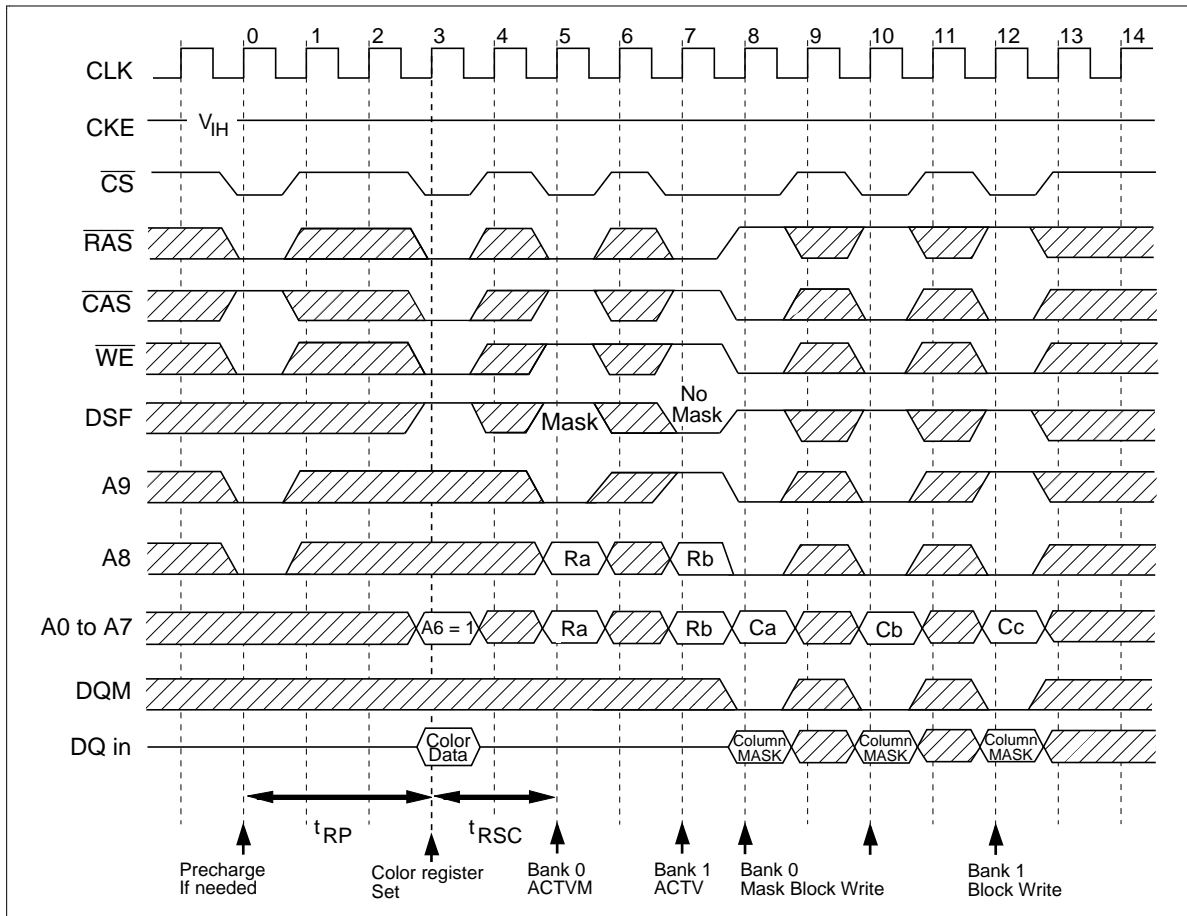


## HM5283206 Series

### Mask Register Set Cycle

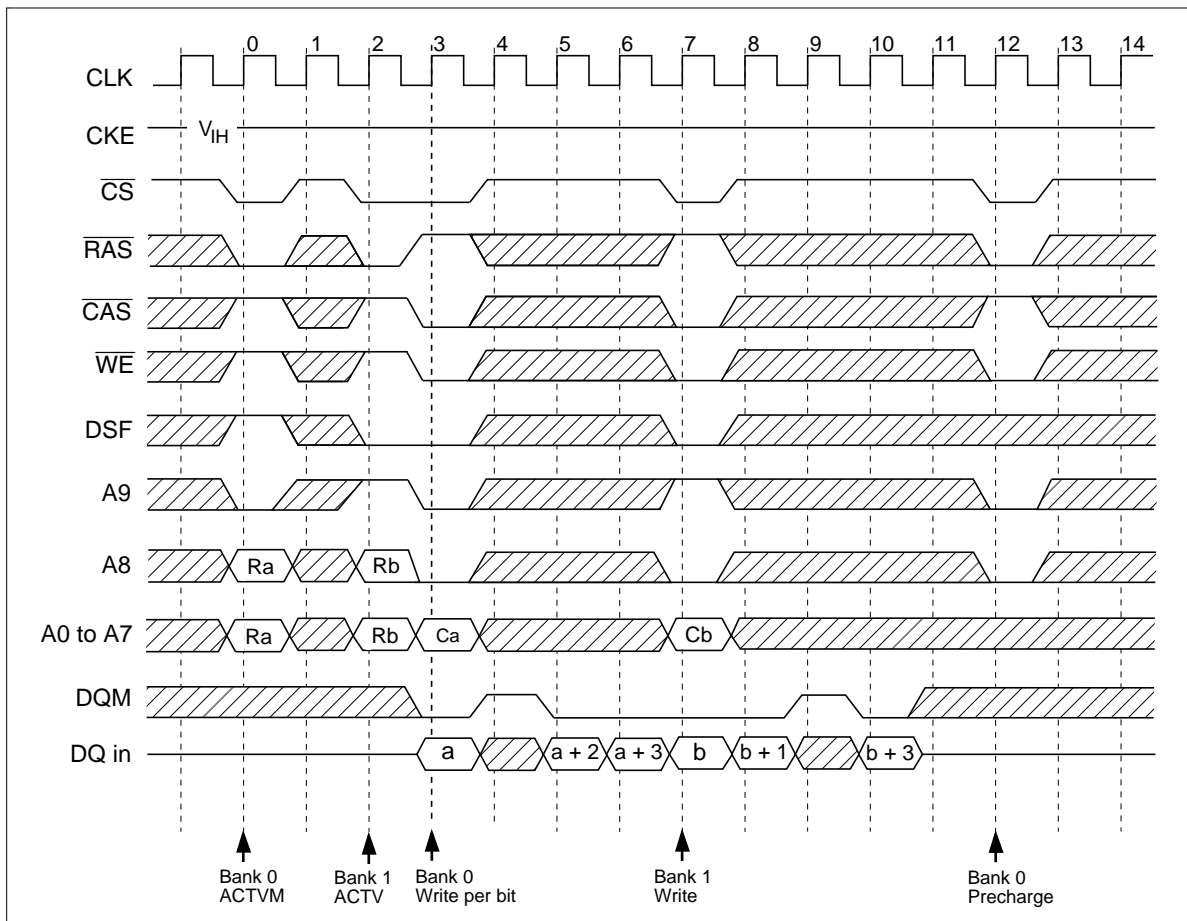


Color Register Set Cycle

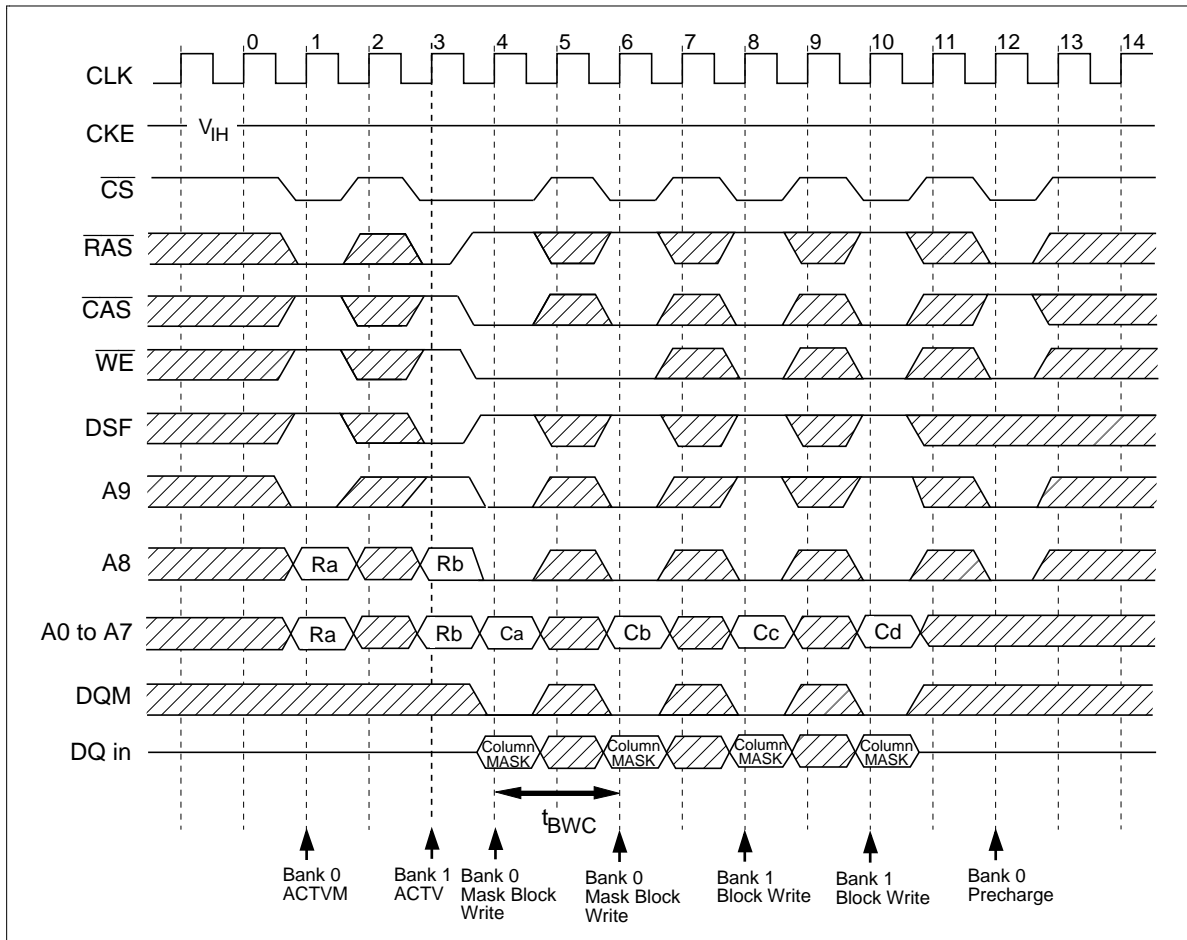


## HM5283206 Series

### Write Cycle (with I/O Mask)



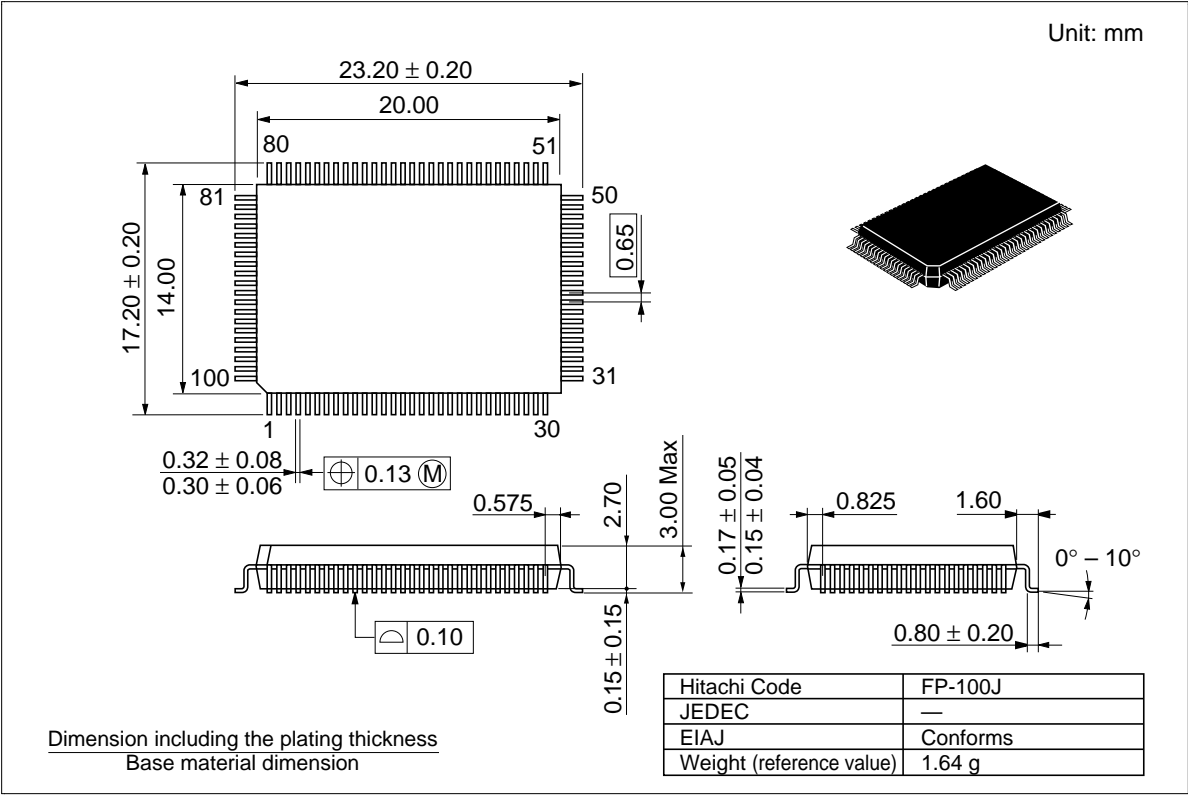
Block Write Cycle



HM5283206 Series

Package Dimensions

HM5283206FP Series (FP-100J)



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## HM5283206 Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 20, 1994	Initial issue	Y. Saiki	T. Kizaki
0.1	Nov. 11, 1994	Commands Operation Change of column block and DQ input at the block write cycle and column mask location Operation of HM5283206 Series Change of column block and the order of burst operation Addition of description for read command to write or block write command interval (3) Change of figure for bank active command interval AC Characteristics $t_{OH}$ min: 2/2/2 ns to 3/3/3 ns $t_{HZ}$ (CL = 1) max: 10/12/14 ns to 13/15/17 ns $t_{CKS}$ min: 3/2/2 ns to 3/3/3 ns $t_{CKH}$ min: 1/2/2 ns to 1/1/1 ns $t_{RC}$ min: 90/100/125 ns to 90/108/135 ns $t_{RAS}$ min: 60/70/80 ns to 60/72/90 ns Change of Timing Waveforms: Read Cycle/Write Cycle, Color Register Set Cycle and Block Write Cycle	Y. Saiki	T. Kizaki
0.2	Nov. 20, 1995	Deletion of HM5283206TT Series Change of Simplified State Diagram Commands Operation Change of description for Commands Operation Change of figure for Column address and write command BL = 2 Change of description for Graphic Commands Change of Command Truth Table and CKE Truth Table Change of Function Truth Table: Change of notes 5 Addition of notes 6 Operation of HM5283206 Series Addition of note for read with auto precharge, write with auto precharge and power down mode Change of figure for write per bit, block write, read command to read command interval, write command to write command interval and write command to precharge command AC Characteristics Change of figure for Test load (B) DC Characteristics $I_{CC1}$ max: TBD to 180/150/120 mA $I_{CC2}$ max: TBD to 5/5/5 mA $I_{CC2}$ max: TBD to 3/3/3 mA $I_{CC2}$ max: TBD to 75/60/50 mA $I_{CC3}$ max: TBD to 10/10/10 mA $I_{CC3}$ max: TBD to 80/65/55 mA $I_{CC4}$ (CL = 1) max: TBD to 170/140/110 mA $I_{CC4}$ (CL = 2) max: TBD to 240/200/160 mA $I_{CC4}$ (CL = 3) max: TBD to 280/240/190 mA $I_{CC5}$ max: TBD to 150/120/100 mA	Y. Saiki	T. Kizaki

## HM5283206 Series

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.2	Nov. 20, 1995	DC Characteristics I <sub>CC6</sub> max: 2/2/2 mA to 4/4/4 mA Addition of I <sub>CC7</sub> max: 160/130/110 mA	Y. Saiki	T. Kizaki
0.2	Nov. 20, 1995	AC Characteristics t <sub>HZ</sub> min: 2/2/2 ns to —/—/— ns t <sub>DS</sub> , t <sub>AS</sub> , t <sub>CKS</sub> , t <sub>CMS</sub> min: 3/3/3 ns to 3/3.5/4 ns t <sub>DH</sub> , t <sub>AH</sub> , t <sub>CKH</sub> , t <sub>CMH</sub> min: 1/1/1 ns to 1/1.5/2 ns Addition of t <sub>RASC</sub> max: 80000/80000/80000 ns Change of notes 4 Change of Timing Waveforms Read cycle, auto refresh cycle, self refresh cycle, clock suspend mode and power down mode	Y. Saiki	T. Kizaki
0.3	Feb. 15, 1996	AC Characteristics t <sub>RAS</sub> max: 10000/10000/10000 ns 120000/120000/120000 ns t <sub>RASC</sub> max: 80000/80000/80000 ns 120000/120000/120000 ns Change of notes 4	Y. Saiki	T. Kizaki
1.0	May. 30, 1996	Commands Operation Change of CKE Truth Table	Y. Saiki	T. Kizaki
2.0	Jul. 30, 1997	Addition of HM5283206-8 Series Deletion of HM5283206-15 Series Change of CKE Truth Table AC Characteristics t <sub>AC</sub> (CL = 1) max: 22 ns to 23 ns Change of package informations: Height (max) 3.10 to 3.00	M. Suzuki	T. Kizaki
3.0	Nov. 20, 1997	DC Characteristics I <sub>CC1</sub> max: TBD/180/150 mA to 210/180/150 mA I <sub>CC2</sub> max: TBD/5/5 mA to 5/5/5 mA I <sub>CC2</sub> max: TBD/3/3 mA to 3/3/3 mA I <sub>CC2</sub> max: TBD/75/60 mA to 95/75/60 mA I <sub>CC3</sub> max: TBD/10/10 mA to 15/10/10 mA I <sub>CC3</sub> max: TBD/80/65 mA to 100/80/65 mA I <sub>CC4</sub> (CL = 1) max: TBD/170/140 mA to 220/170/140 mA I <sub>CC4</sub> (CL = 2) max: TBD/240/200 mA to 280/240/200 mA I <sub>CC4</sub> (CL = 3) max: TBD/280/240 mA to 330/280/240 mA I <sub>CC5</sub> max: TBD/150/120 mA to 190/150/120 mA I <sub>CC6</sub> max: TBD/4/4 mA to 4/4/4 mA I <sub>CC7</sub> max: TBD/160/130 mA to 200/160/130 mA	H. Suzuki	K. Hayakawa
4.0	Jan. 20, 1998	Correct error	H. Suzuki	K. Hayakawa

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## HM5283206 Series

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Rev.	Date	Contents of Modification	Drawn by	Approved by
5.0	May. 19, 1998	Correct errors Change of figures for Column address and write command (BL = 2), READ to PRECHARGE command interval: Output all data (CL = 2), Special mode register set (load mask) in idle state and block write Change of description for Precharge command and Graphic commands note Change of simplified State Diagram AC Characteristics $t_{BWR}$ (CL = 1), (CL = 2) min: 24/30/36 ns to 24/3034 ns	H. Suzuki	K. Hayakawa
6.0	Oct. 2, 1998	Correct errors Column address and block write command: A0 to A1 HIGH or LOW to A0 to A2 HIGH or LOW CKE Truth Table Change of DSF (self refresh): L to ×		

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