HM534252 Series

262,144-Word x 4-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM534252 is a 1-Mbit multiport video RAM equipped with a 256k-word x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function.

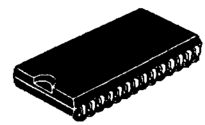
It also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

■ FEATURES

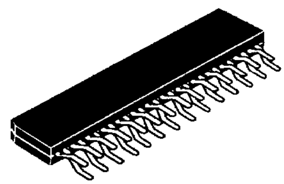
- Multiport Organization
  Asynchronous and Simultaneous Operation of RAM and SAM Capability
  RAM............................256k-word x 4-bit
  SAM............................512-word x 4-bit
- Access Time
  RAM ....100 ns/100 ns/120 ns/150 ns (max)
  SAM................30 ns/40 ns/40 ns/50 ns (max)
- Cycle Time
  RAM ....190 ns/190 ns/220 ns/260 ns (max)
  SAM................30 ns/40 ns/40 ns/60 ns (max)
- Low Power
  Active
  RAM ....385 mW (max)
  SAM ....358 mW (max)
  Standby ....40 mW (max)
- High-speed Page Mode Capability
- Logic Operation Mode Capability
- 2 Types of Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  $\overline{RAS}$ Only Refresh
  $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  Hidden Refresh
- TTL Compatible

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_3	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_3	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection



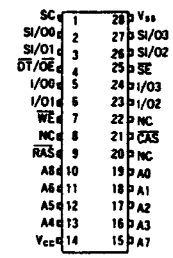
(CP-28D)



(ZP-28)

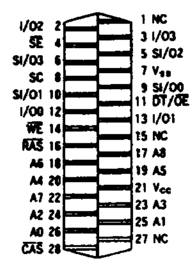
■ PIN OUT

HM534252JP Series



(Top View)

HM534252ZP Series

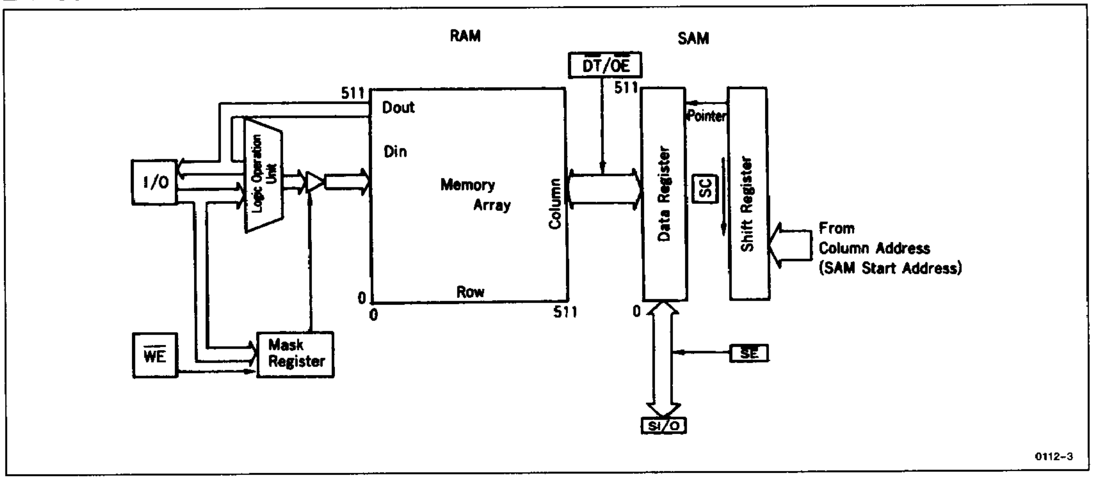


(Bottom View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM534252JP-10	100 ns	400 mil
HM534252JP-11	100 ns	28-pin
HM534252JP-12	120 ns	Plastic SOJ
HM534252JP-15	150 ns	(CP-28D)
HM534252ZP-10	100 ns	400 mil
HM534252ZP-11	100 ns	28-pin
HM534252ZP-12	120 ns	Plastic ZIP
HM534252ZP-15	150 ns	(ZP-28)

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation of the HM534252.

• Table 1. Operation Cycles of the HM534252

Input Level at the Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	H	X	CBR Refresh
L	X	L	X	Logic Operation Set/Reset

Note: X; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534252 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in a serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

■ OPERATION OF HM534252

• Operation of RAM Port

RAM Read Cycle ($\overline{\text{DT}}/\overline{\text{OE}}$ high, $\overline{\text{CAS}}$ high, at the falling edge of $\overline{\text{RAS}}$)

Row address is entered at the $\overline{\text{RAS}}$ falling edge and column address at the $\overline{\text{CAS}}$ falling edge to the device as in standard DRAM. Then when $\overline{\text{WE}}$ is high and $\overline{\text{DT}}/\overline{\text{OE}}$ is low while $\overline{\text{CAS}}$ is low, the selected address data outputs through I/O pin. At the falling edge of RAS, $\overline{\text{DT}}/\overline{\text{OE}}$ and $\overline{\text{CAS}}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{\text{RAS}}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{\text{DT}}/\overline{\text{OE}}$ high, $\overline{\text{CAS}}$ high at the falling edge of $\overline{\text{RAS}}$)

• Normal Mode Write Cycle ($\overline{\text{WE}}$ high at the falling edge of $\overline{\text{RAS}}$)

When $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are set low after $\overline{\text{RAS}}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{\text{WE}}$ should be high at the falling edge of $\overline{\text{RAS}}$ to distinguish normal mode from mask write mode.

If $\overline{\text{WE}}$ is set low before the $\overline{\text{CAS}}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{\text{CAS}}$ falling edge.

If $\overline{\text{WE}}$ is set low after the $\overline{\text{CAS}}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{\text{WE}}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{\text{OE}}$ in high.

If $\overline{\text{WE}}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{\text{CAS}}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{\text{OE}}$ high.

• Mask Write Mode ($\overline{\text{WE}}$ low at the falling edge of $\overline{\text{RAS}}$)

If $\overline{\text{WE}}$ is set low at the falling edge of $\overline{\text{RAS}}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{\text{RAS}}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{\text{RAS}}$ cycle, So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{\text{DT}}/\overline{\text{OE}}$ high, $\overline{\text{CAS}}$ high at the falling edge of $\overline{\text{RAS}}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore address access time (t_{AA}), $\overline{\text{RAS}}$ to column address delay time (t_{RAD}), and access time from $\overline{\text{CAS}}$ precharge (t_{ACP}) are added. In one $\overline{\text{RAS}}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 μs).

Transfer Operation

The HM534252 provides the transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{\text{DT}}/\overline{\text{OE}}$ low at the falling edge of $\overline{\text{RAS}}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
 (a) Read transfer cycle:RAM $\rightarrow$ SAM
 (b) Write transfer cycle:RAM $\leftarrow$ SAM

(3) Determine input or output of SAM I/O pin (SI/O)
 Read transfer cycle: SI/O output
 Pseudo transfer cycle,
 write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither CAS nor address need to be set because SAM start address can be latched internally.

Read Transfer Cycle ($\overline{\text{CAS}}$ high, $\overline{\text{DT}}/\overline{\text{OE}}$ low, WE high at the falling edge of $\overline{\text{RAS}}$)

This cycle becomes read transfer cycle by driving $\overline{\text{DT}}/\overline{\text{OE}}$ low and $\overline{\text{WE}}$ high at the falling edge of $\overline{\text{RAS}}$. The row address data (512 x 4-bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$. After the rising edge of $\overline{\text{DT}}/\overline{\text{OE}}$, the new address data outputs from SAM start address determined by column address.

This cycle can access SAM serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{\text{DT}}/\overline{\text{OE}}$ rising edge, and t_{SDH} (min) between the first SAM access and $\overline{\text{DT}}/\overline{\text{OE}}$ rising edge (see figure 1).

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{\text{RAS}}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{\text{CAS}}$ high, $\overline{\text{DT}}/\overline{\text{OE}}$ low, $\overline{\text{WE}}$ low, and $\overline{\text{SE}}$ high at the falling edge of $\overline{\text{RAS}}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{\text{CAS}}$ is high $\overline{\text{DT}}/\overline{\text{OE}}$ low, $\overline{\text{WE}}$ low, and $\overline{\text{SE}}$ high, at the falling edge of $\overline{\text{RAS}}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{\text{RAS}}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{\text{RAS}}$ becomes high. In this cycle, SAM access is inhibited during $\overline{\text{RAS}}$ low, therefore, SC should not be raised.

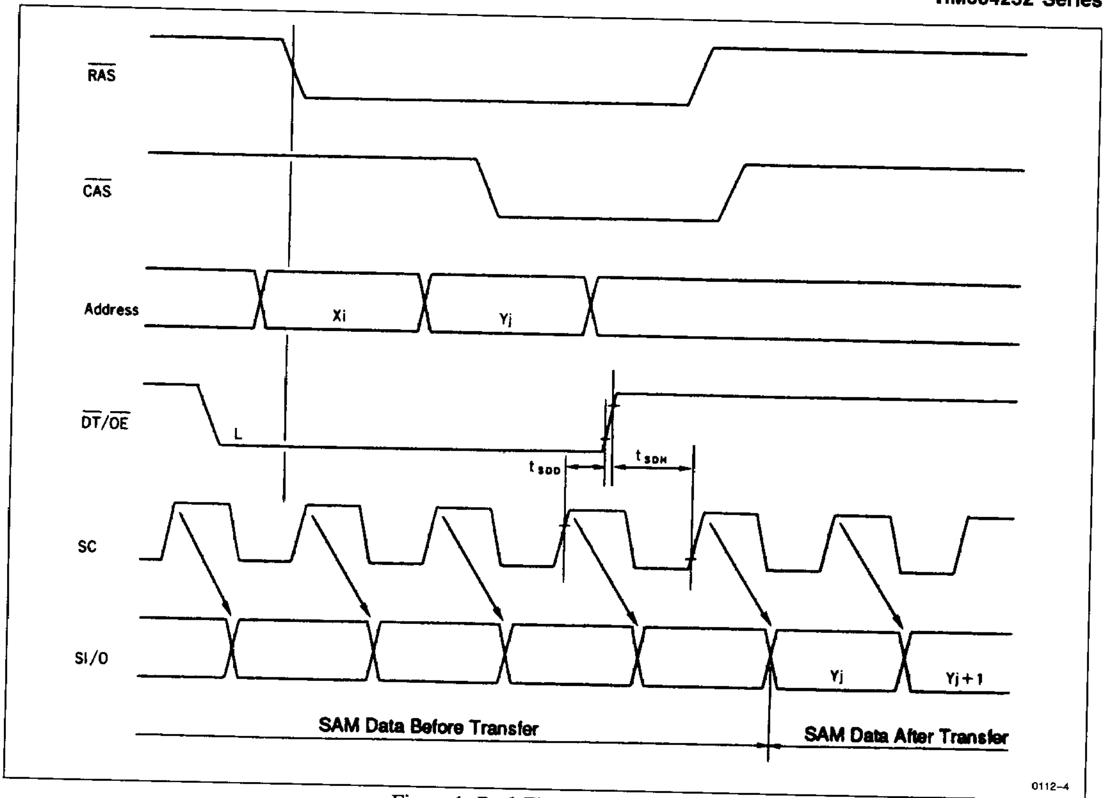


Figure 1. Real Time Read Transfer

Write Transfer Cycle ($\overline{\text{CAS}}$ high, $\overline{\text{DT}}/\overline{\text{OE}}$ low, $\overline{\text{WE}}$ low, and $\overline{\text{SE}}$ low at the falling edge of $\overline{\text{RAS}}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{\text{RAS}}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{\text{RAS}}$ becomes high. SAM access is inhibited during $\overline{\text{RAS}}$ low. In this period, SC should not be raised.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{\text{SE}}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{\text{SE}}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{\text{SE}}$ high can mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{\text{RAS}}$ only refresh cycle, (2) $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{\text{RAS}}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{\text{RAS}}$ Only Refresh Cycle: $\overline{\text{RAS}}$ only refresh cycle is performed by activating only $\overline{\text{RAS}}$ cycle with $\overline{\text{CAS}}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{\text{CAS}}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{\text{DT}}/\overline{\text{OE}}$ should be high at the falling edge of $\overline{\text{RAS}}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$. In this cycle, refresh address does not need to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{\text{RAS}}$ only refresh cycles because $\overline{\text{CAS}}$ circuits don't operate. To distinguish this cycle from logic operation set/reset cycle, $\overline{\text{WE}}$ should be high at the falling edge of $\overline{\text{RAS}}$.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating RAS when DT/OE and CAS keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode

The HM534252 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{\text{CAS}}$ and $\overline{\text{WE}}$ Low at the falling edge of $\overline{\text{RAS}}$)

In logic operation set/reset cycle, the following operations are performed at the same time; (1) Selection of logic operations and logic operation mode set/reset, (2) Mask data programming, (3) $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are low at the falling edge of $\overline{\text{RAS}}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{\text{RAS}}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{\text{RAS}}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0–A3 levels at the falling edge of $\overline{\text{RAS}}$. (A4–A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0, 1, 0, 1) resets the logic operation mode. When write cycle is performed after than, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{\text{RAS}}$ in logic operation set/reset cycle when mask data is not used.

(2) Mask data programming

High/low level of I/O at the falling edge of $\overline{\text{RAS}}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

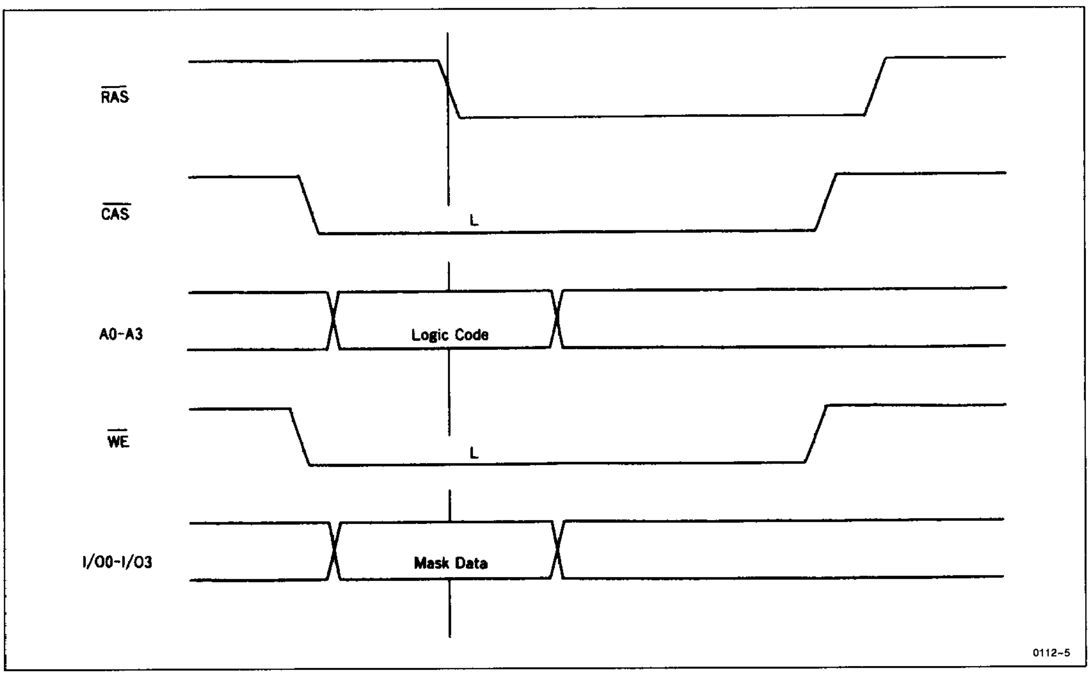


Figure 2. Logic Operation Set/Reset

• Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A3	A2	A1	A0			
0	0	0	0	Zero	0	Logic Operation Mode Set
0	0	0	1	AND1	Di • Mi	
0	0	1	0	AND2	$\overline{\text{Di}}$ • Mi	
0	0	1	1	—	Mi	
0	1	0	0	AND3	Di • $\overline{\text{Mi}}$	
0	1	0	1	THROUGH	Di	Logic Operation Mode Reset
0	1	1	0	EOR	$\overline{\text{Di}}$ • Mi + Di • $\overline{\text{Mi}}$	Logic Operation Mode Set
0	1	1	1	OR1	Di • Mi	
1	0	0	0	NOR	$\overline{\text{Di}}$ • $\overline{\text{Mi}}$	
1	0	0	1	ENOR	Di • Mi + $\overline{\text{Di}}$ • $\overline{\text{Mi}}$	
1	0	1	0	INV1	$\overline{\text{Di}}$	
1	0	1	1	OR2	$\overline{\text{Di}}$ + Mi	
1	1	0	0	INV2	$\overline{\text{Mi}}$	
1	1	0	1	OR3	Di + $\overline{\text{Mi}}$	
1	1	1	0	NAND	$\overline{\text{Di}}$ + $\overline{\text{Mi}}$	
1	1	1	1	One	1	

Notes: Di; External data-in
Mi; The data of the memory cell

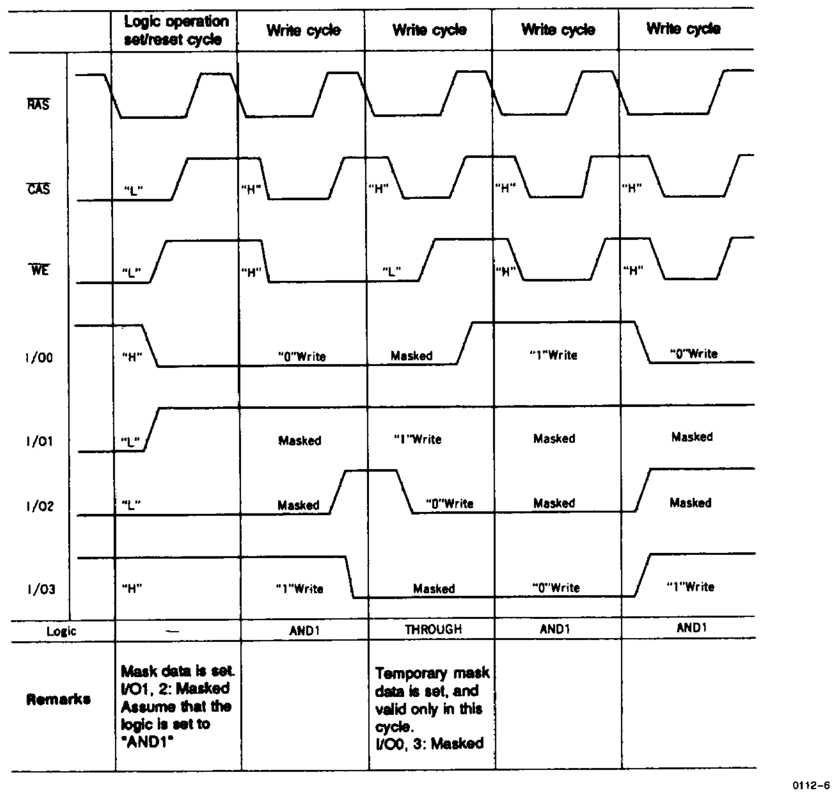


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is divided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed internally.

(1) Reading memory data in given address into internal bus.

(2) Performing operation between input data and memory data.

(3) Writing the result of (2) into address given by (1).

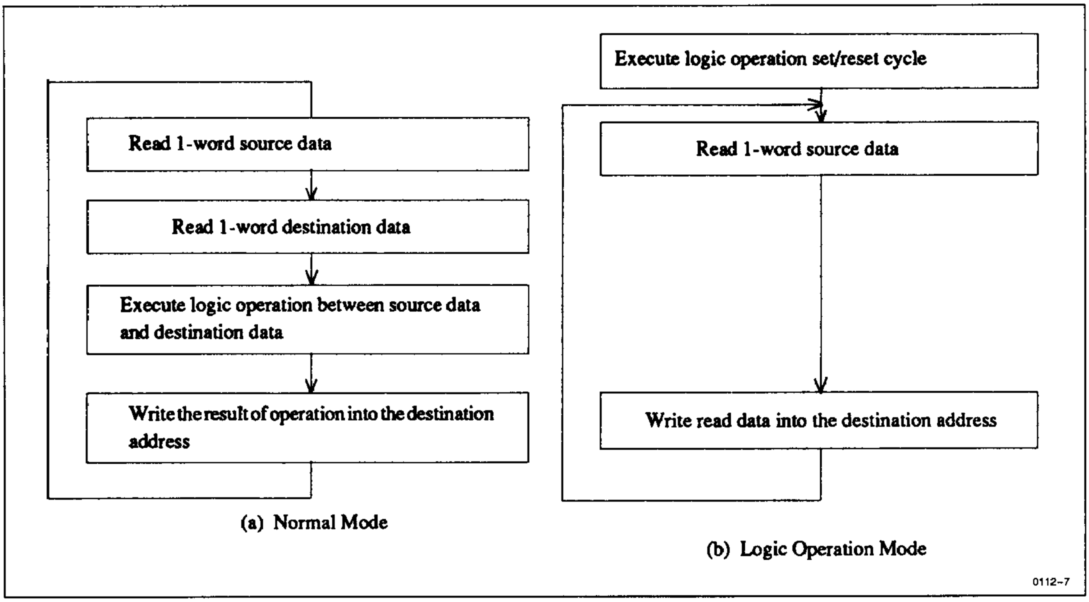


Figure 4. Sequence of Raster Operation

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• **Recommended DC Operating Conditions** (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1, 2
	I_{CC7}	—	120	—	120	—	100	—	85	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1
	I_{CC8}	—	65	—	55	—	55	—	40	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	2
	I_{CC9}	—	120	—	120	—	100	—	85	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode Current	I_{CC4}	—	80	—	80	—	70	—	60	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1, 3
	I_{CC10}	—	130	—	130	—	110	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	60	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	95	—	95	—	90	—	85	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	2
	I_{CC12}	—	135	—	135	—	125	—	115	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

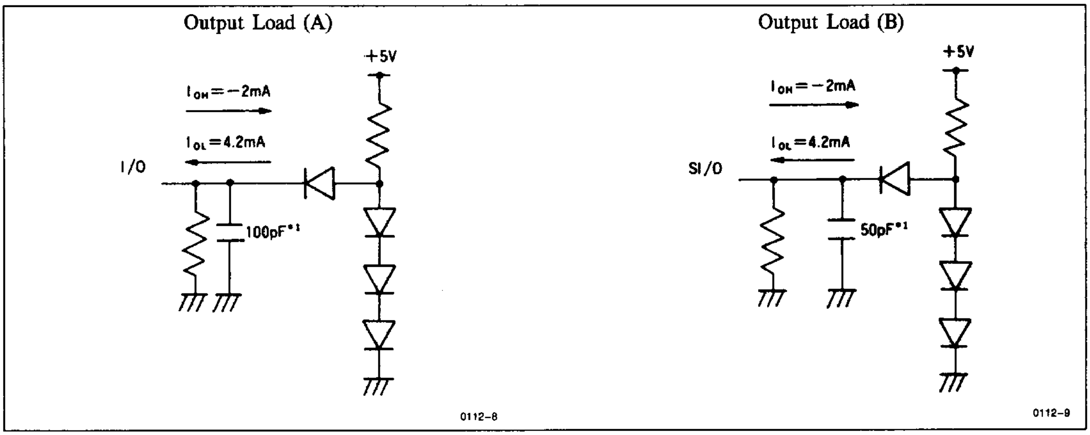
• Capacitance (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

- **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)(1, 11)

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V



Note: *1. Including scope & jig.

Common Parameter

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{\text{OE}}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{\text{CAS}}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{\text{OE}}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{\text{RAS}}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{\text{RAS}}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Modify Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
DT Hold Time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
DT Hold Time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to DT Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to DT Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
DT to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
DT Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
DT Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time from SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

Serial Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

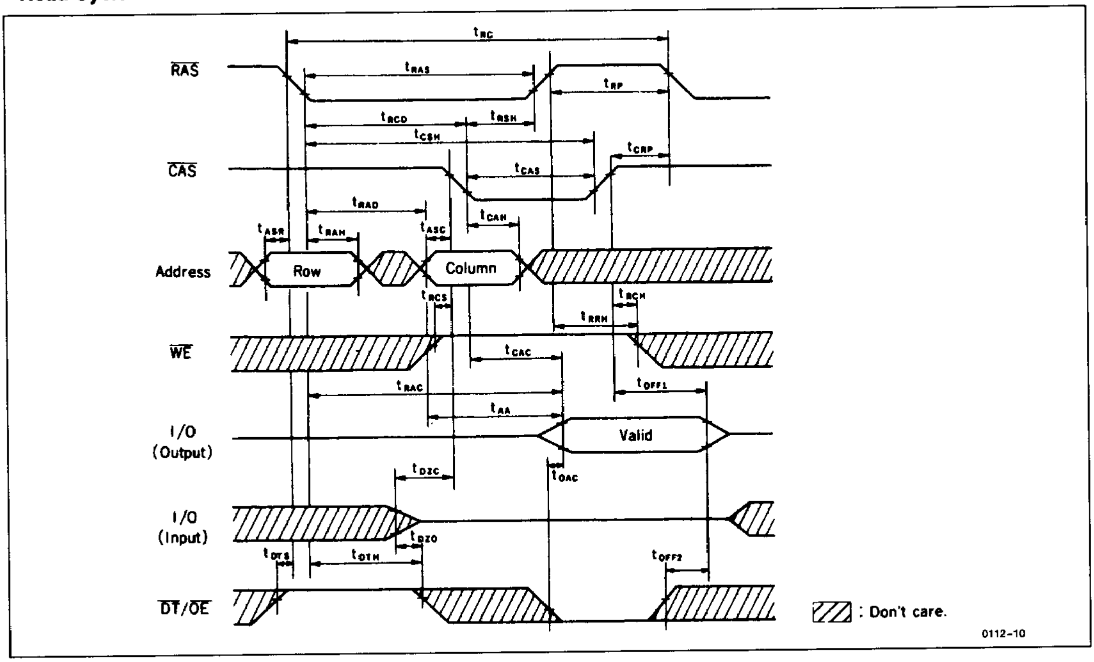
Logic Operation Mode

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width in Write Cycle	t_{RFS}	140	10000	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width in Write Cycle	t_{CFS}	60	10000	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ Hold Time in Write Cycle	t_{FCSH}	140	—	140	—	165	—	200	—	ns	
$\overline{RAS}$ Hold Time in Write Cycle	t_{FRSH}	60	—	60	—	70	—	80	—	ns	
Write Cycle Time	t_{FRC}	230	—	230	—	265	—	310	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	85	—	85	—	100	—	120	—	ns	

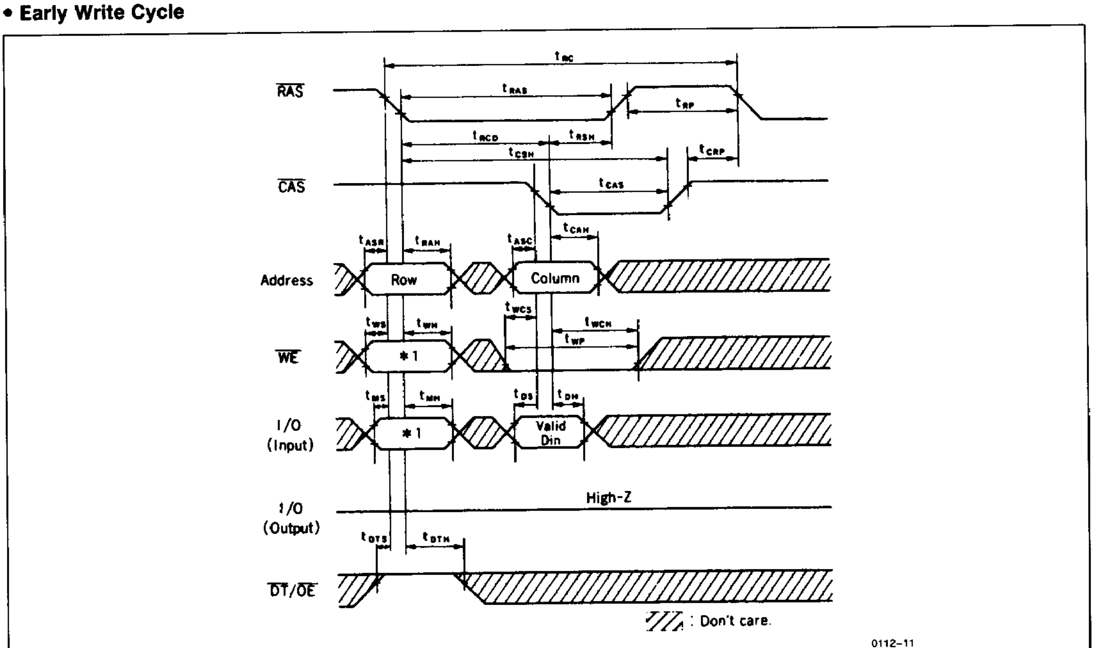
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds that value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} − 200 mV, V_{OL} + 200 mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{SCC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).

■ TIMING WAVEFORMS

• Read Cycle

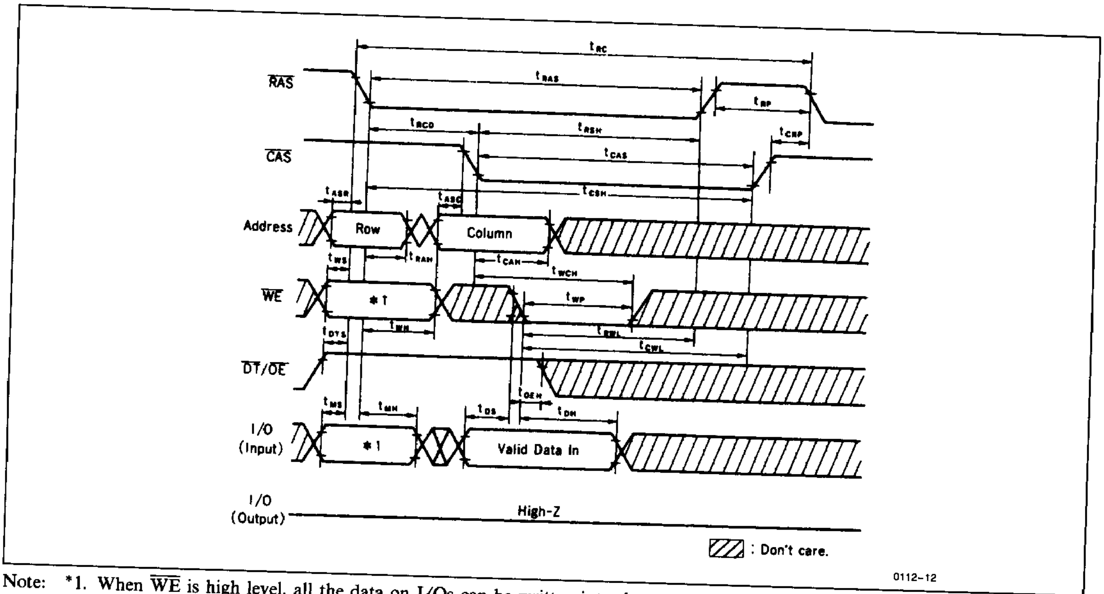


• Early Write Cycle



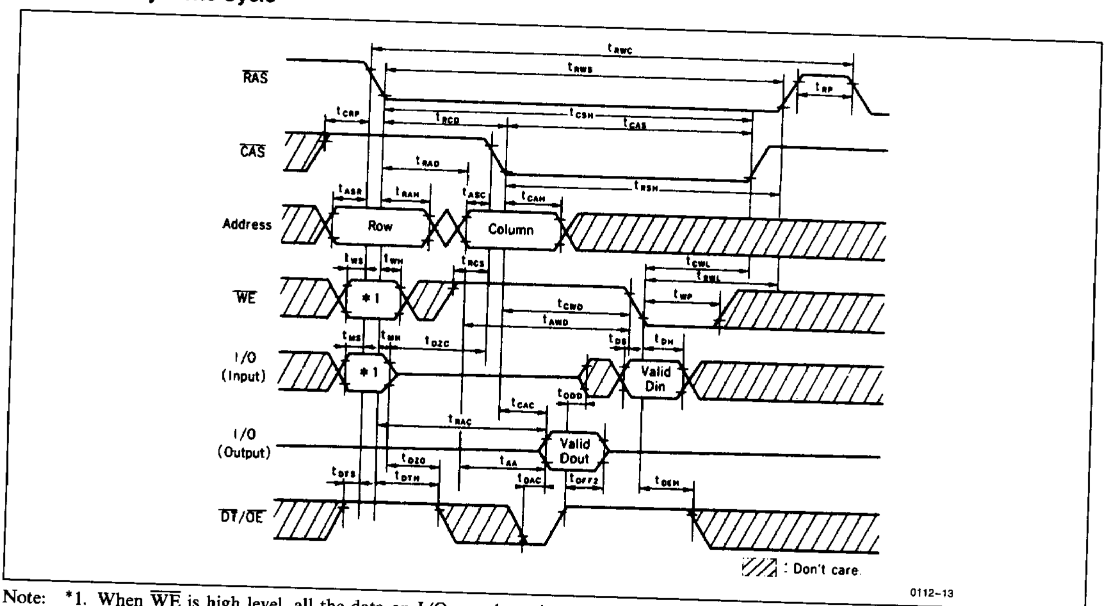
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



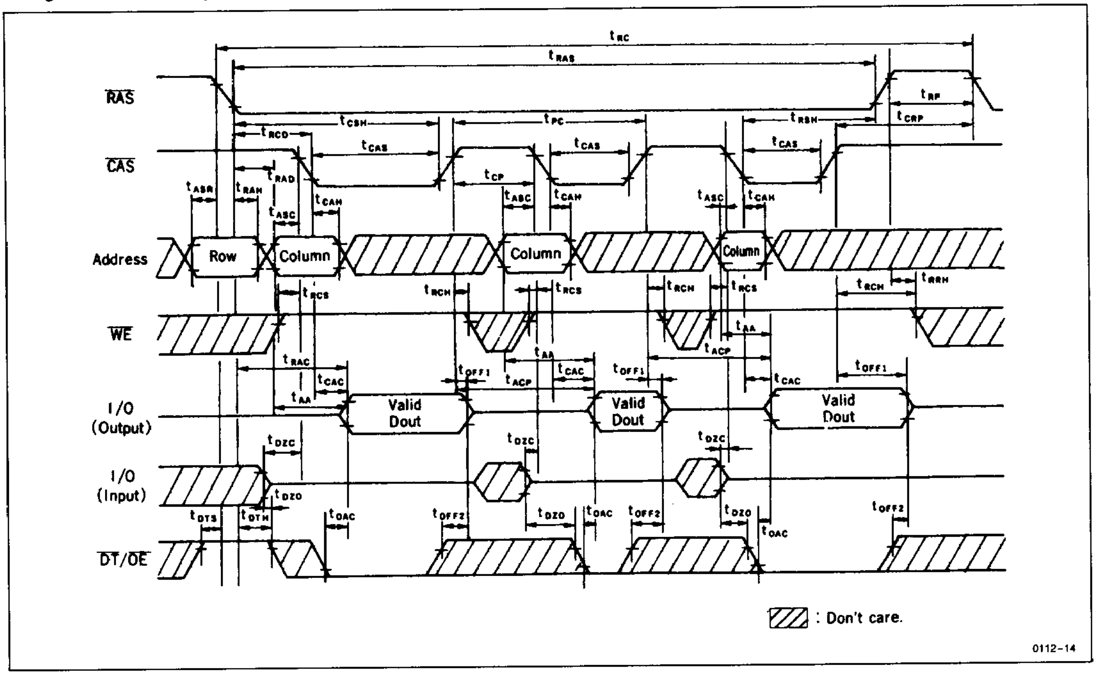
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

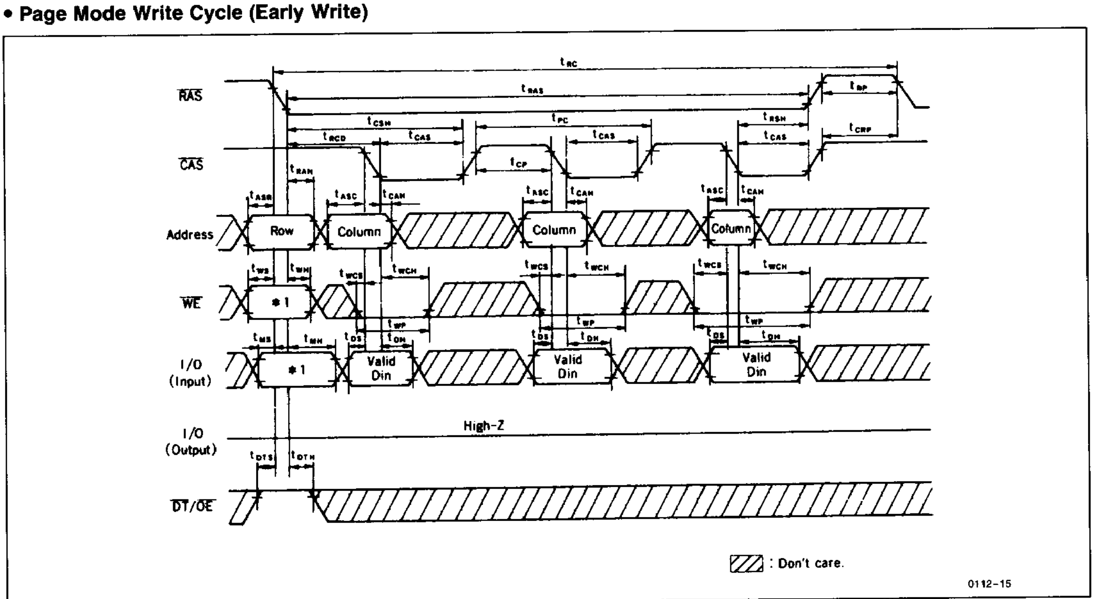


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

- **Page Mode Read Cycle**

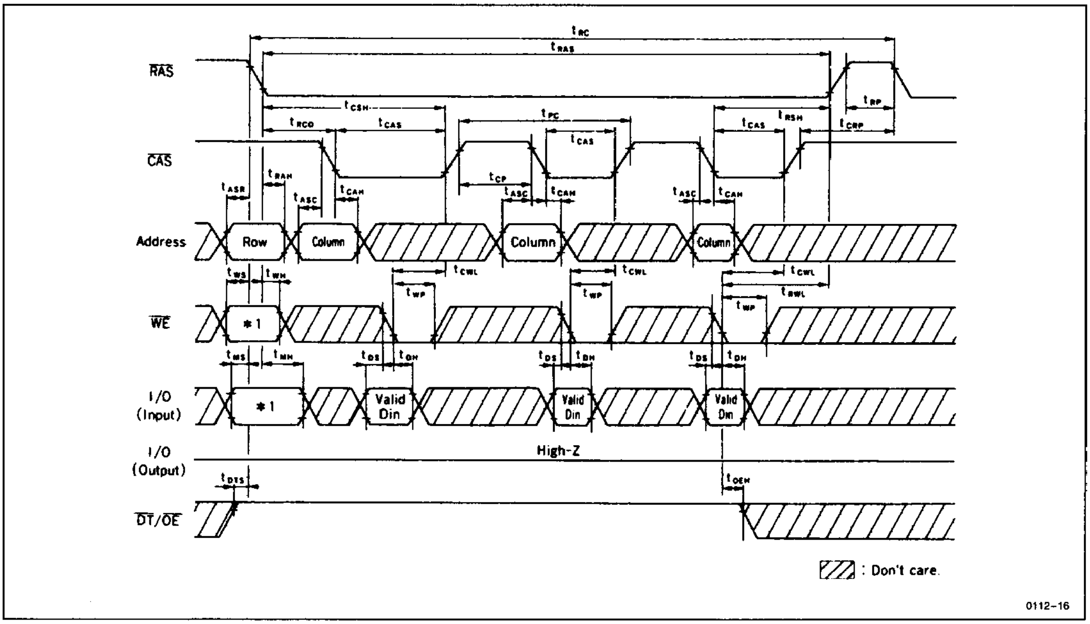


- **Page Mode Write Cycle (Early Write)**



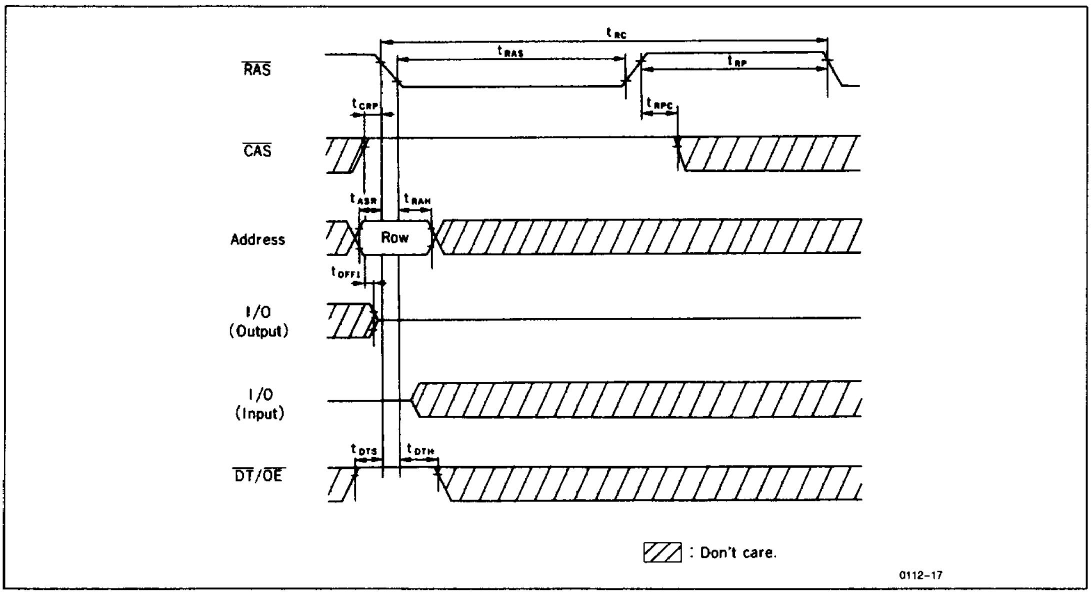
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Write Cycle (Delayed Write)

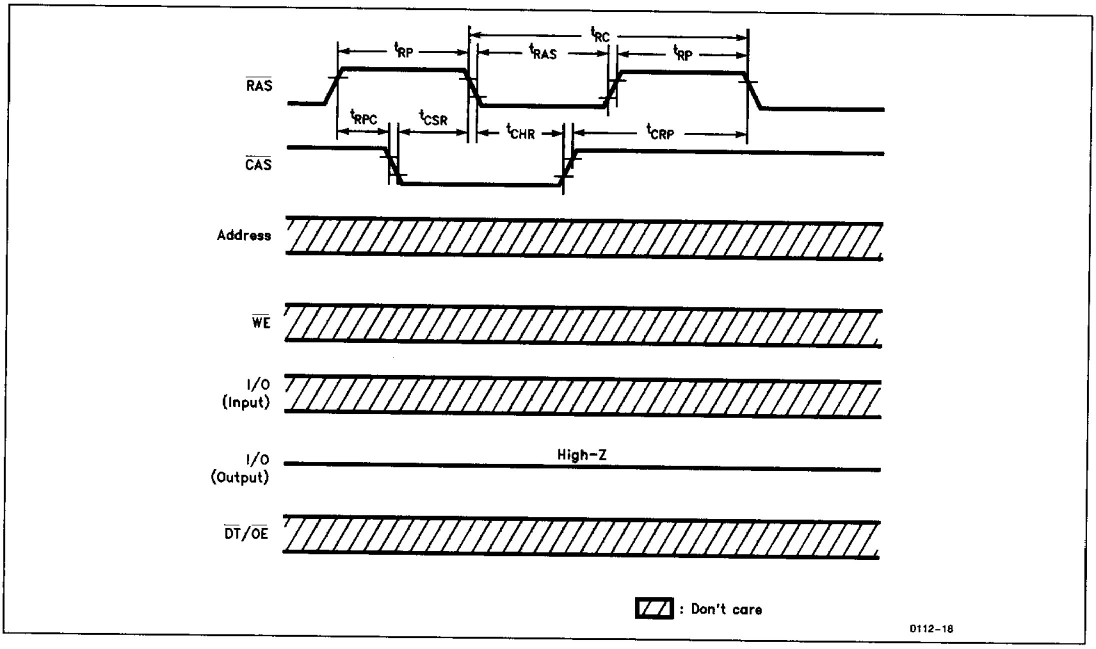


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

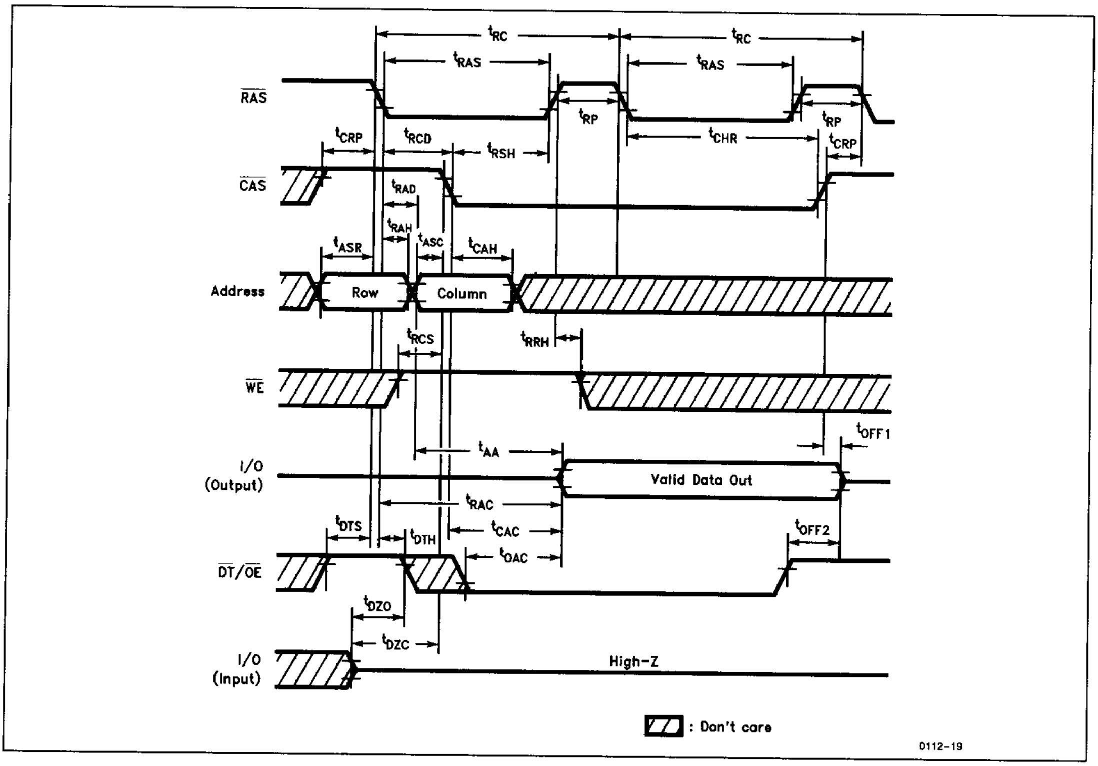
• $\overline{RAS}$ Only Refresh Cycle



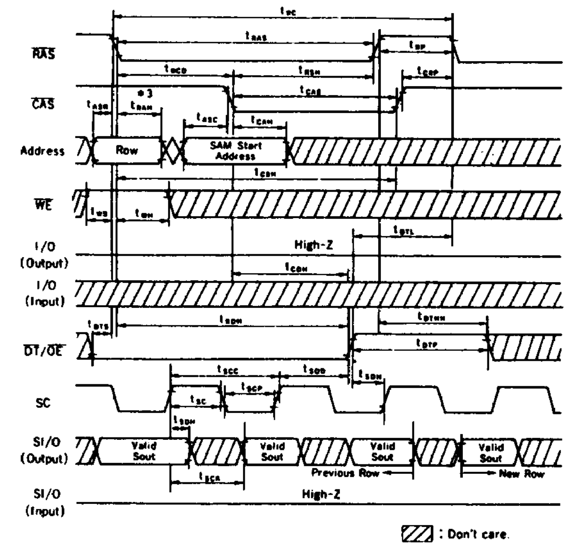
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

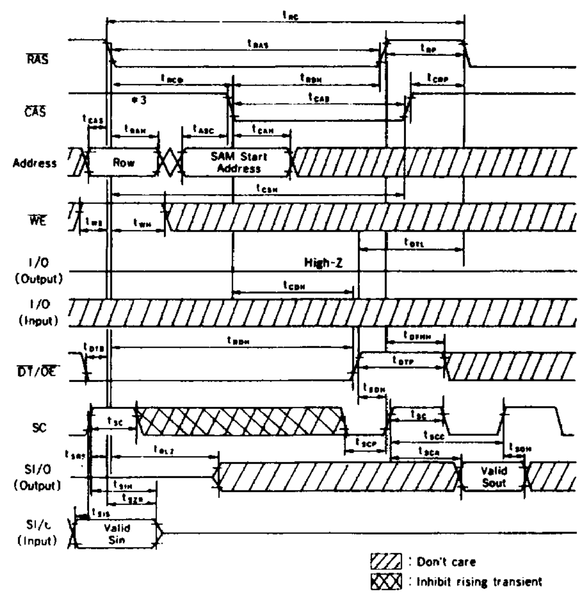


• Read Transfer Cycle (1)*1, *2



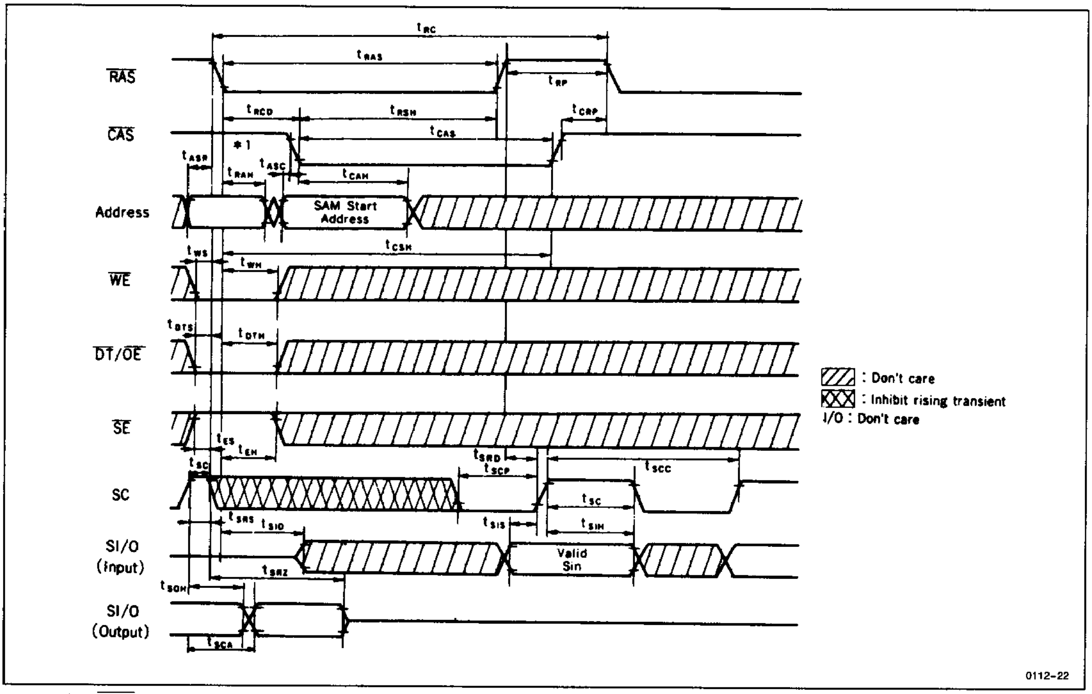
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Read Transfer Cycle (2)*1, *2



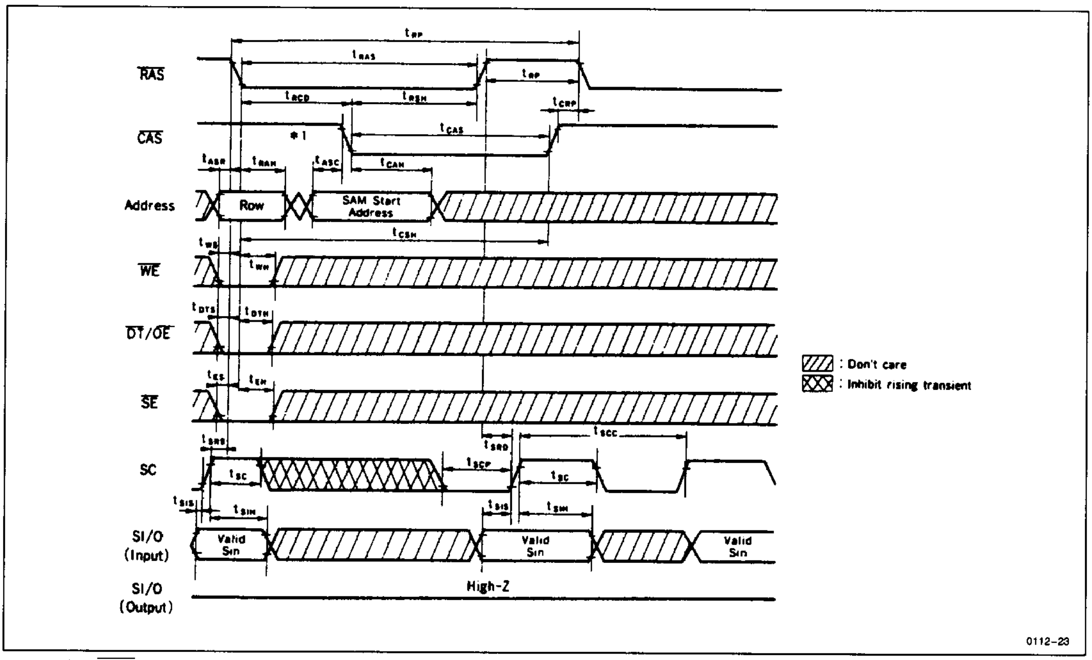
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Pseudo Transfer Cycle**



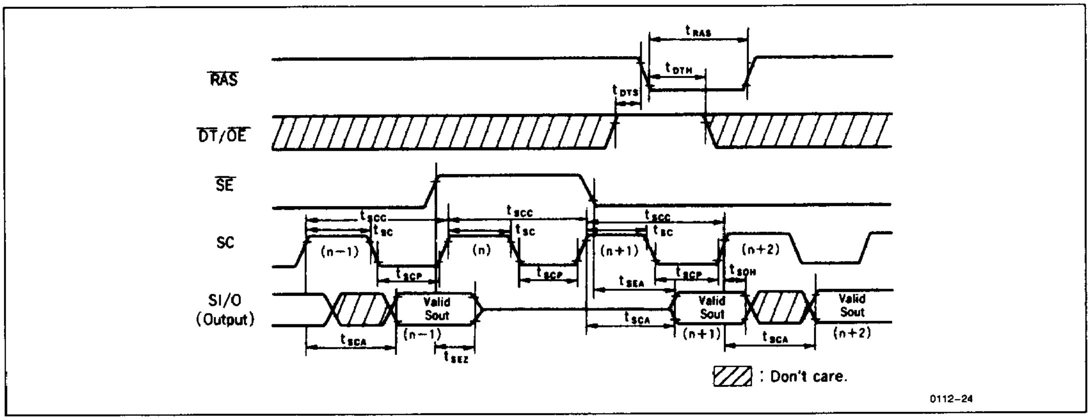
Note: *1. $\overline{\text{CAS}}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Write Transfer Cycle**

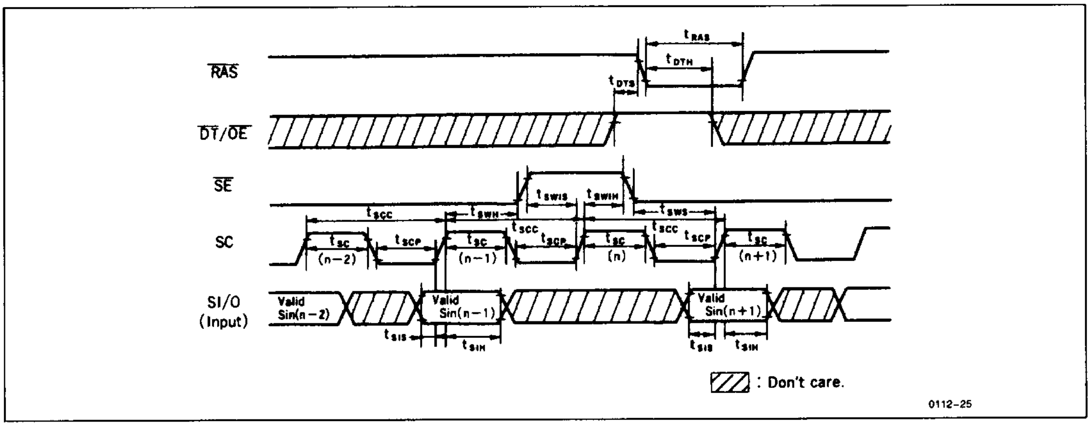


Note: *1. $\overline{\text{CAS}}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

- **Serial Read Cycle**

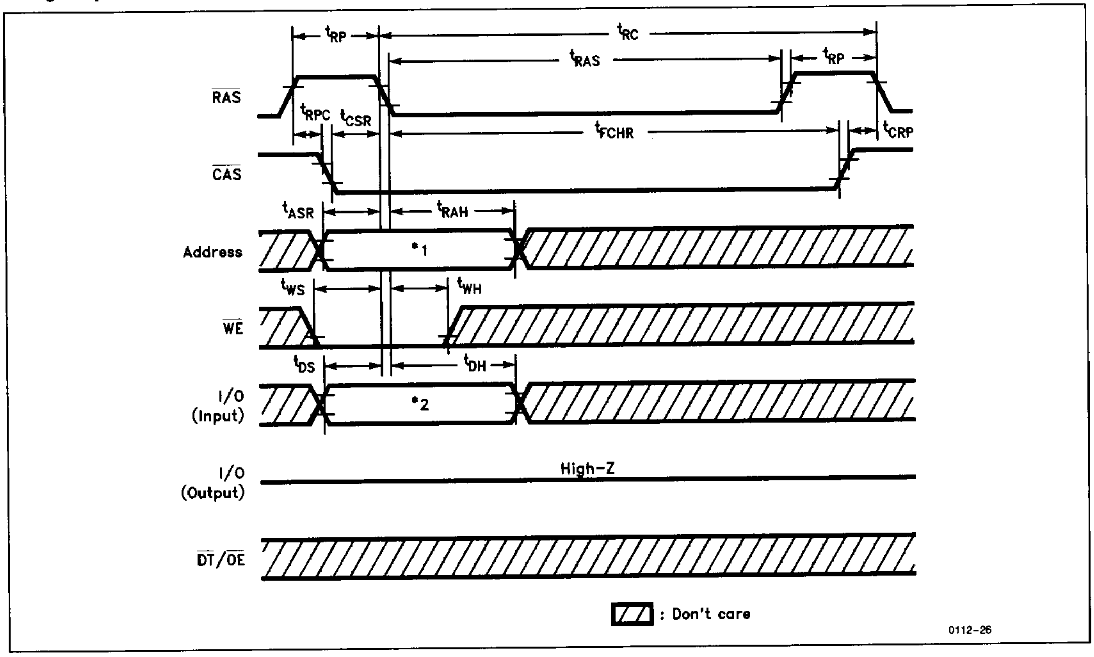


- **Serial Write Cycle**



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

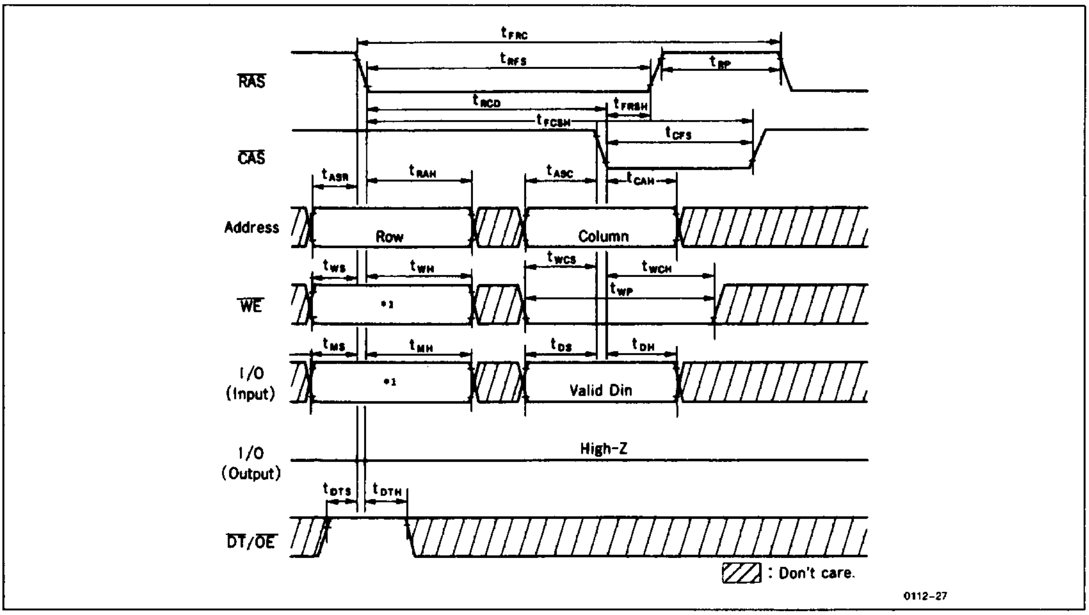
• **Logic Operation Set/Reset Cycle**



Notes: *1. Logic code A0–A3.
*2. Write mask data.

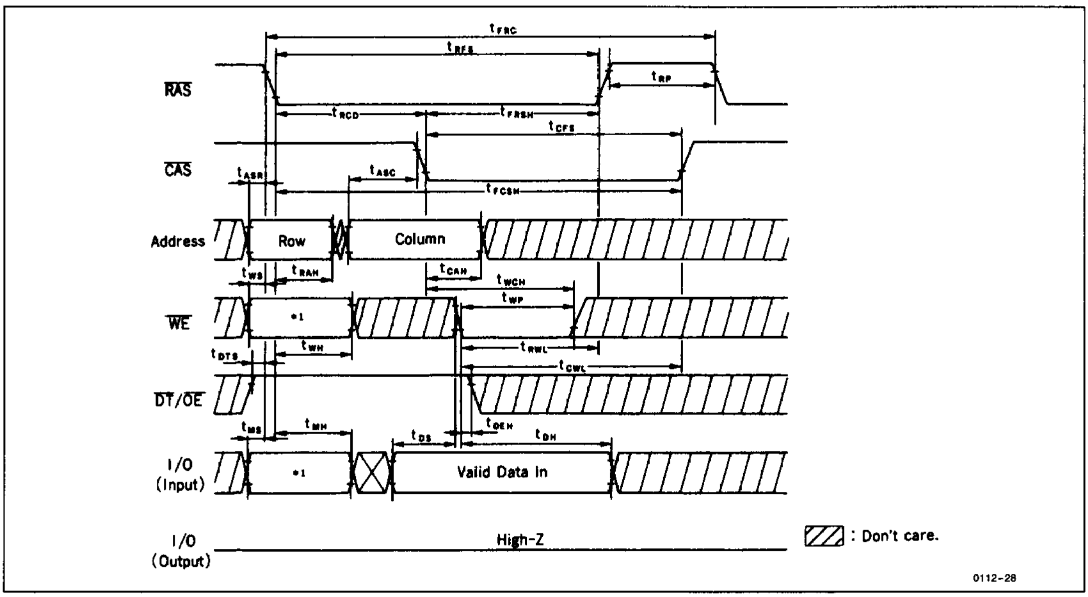
■ LOGIC OPERATION MODE TIMING WAVEFORMS

• Early Write Cycle



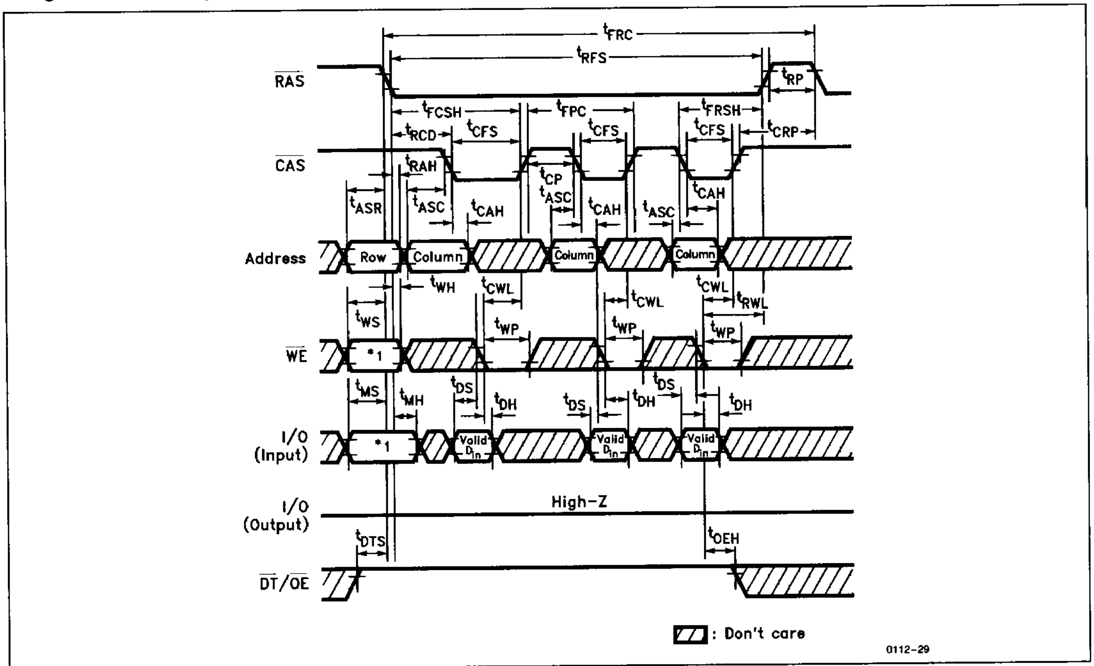
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Delayed Write Cycle



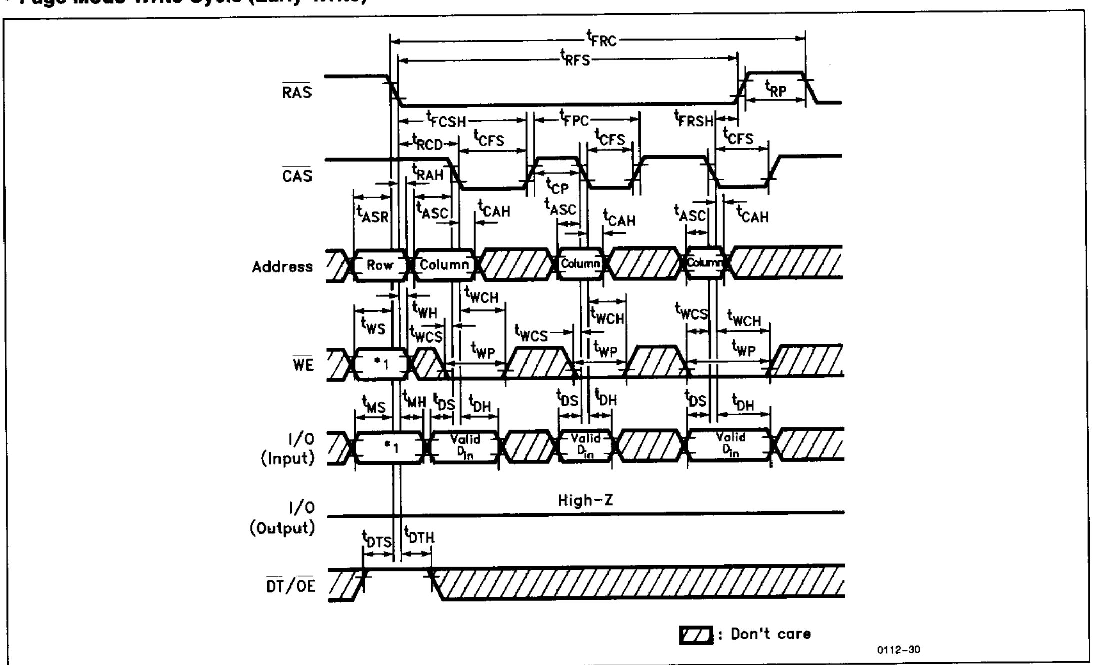
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

- **Page Mode Write Cycle (Delayed Write)**



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

- **Page Mode Write Cycle (Early Write)**



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

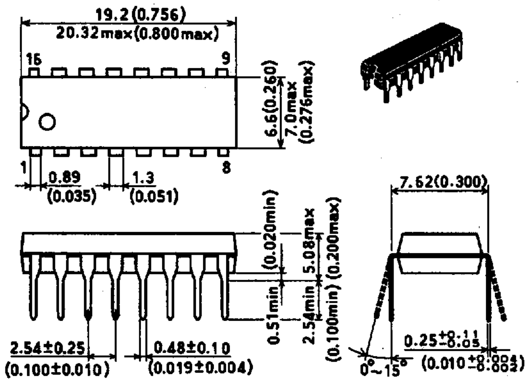
■ PACKAGE INFORMATION

T-90-20

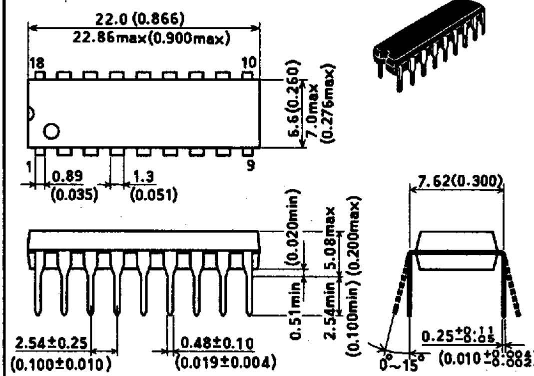
• **Dual-in-line Plastic**

Unit: mm (inch) Scale 3/2

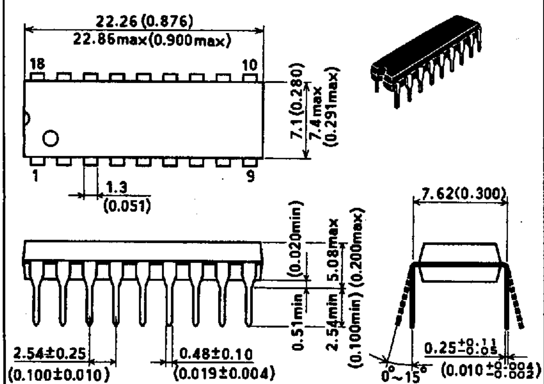
• **DP-16B**



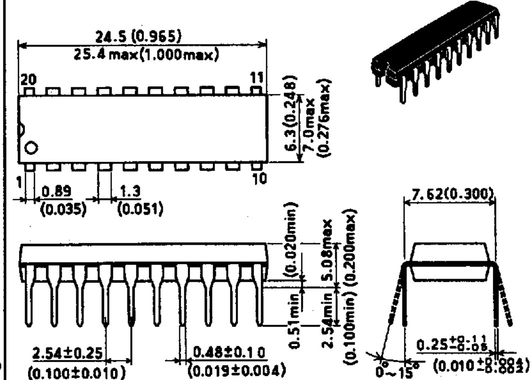
• **DP-18B**



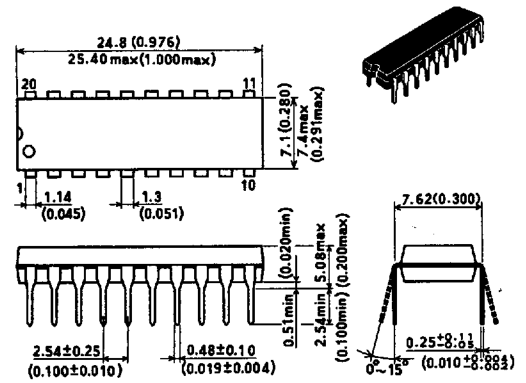
• **DP-18C**



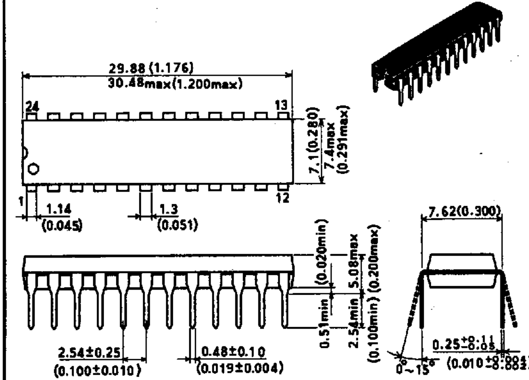
• **DP-20N**



• **DP-20NA**



• **DP-20NC**



• Dual-in-line Plastic

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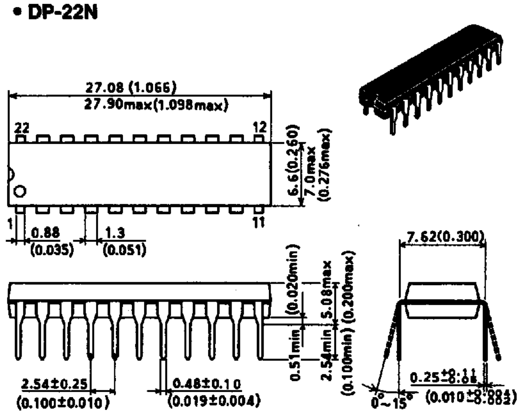
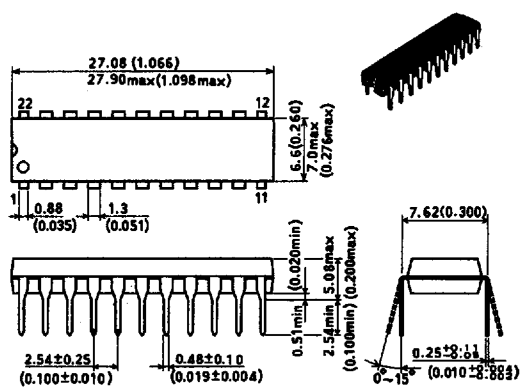
Unit: mm (inch) Scale 3/2

T-90-20

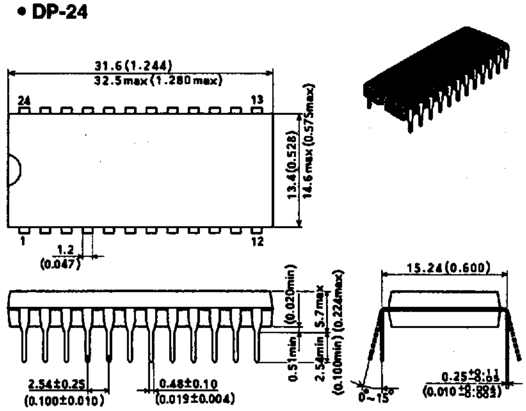
• DP-22N



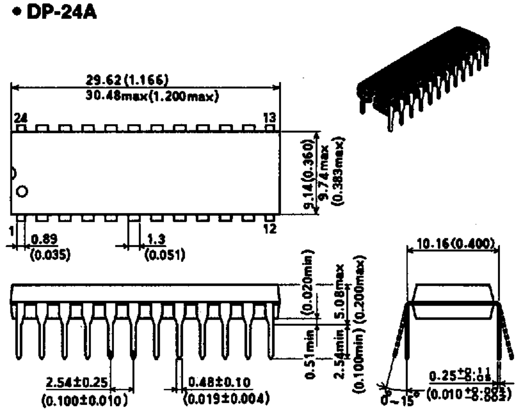
• DP-22NB



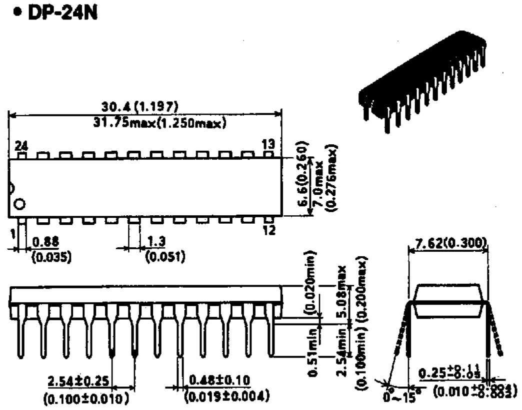
• DP-24



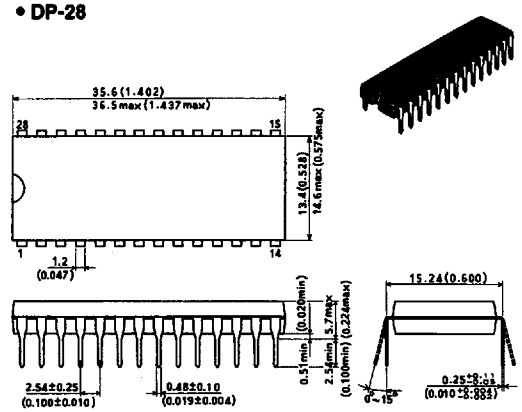
• DP-24A



• DP-24N



• DP-28



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• Dual-in-line Plastic

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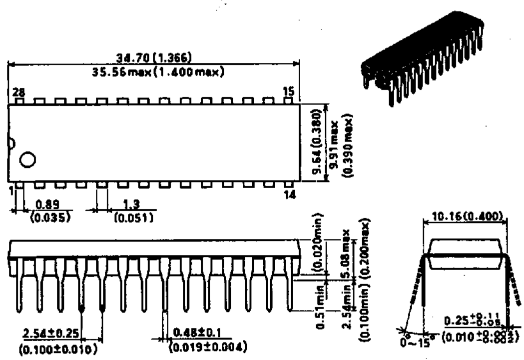
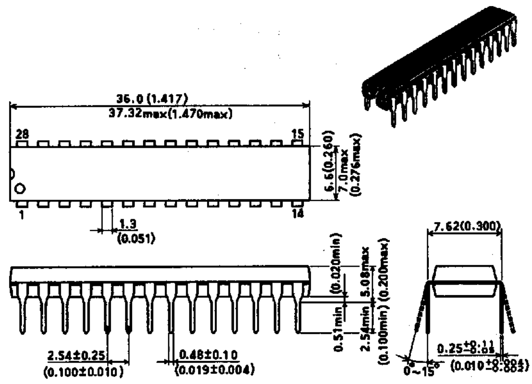
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

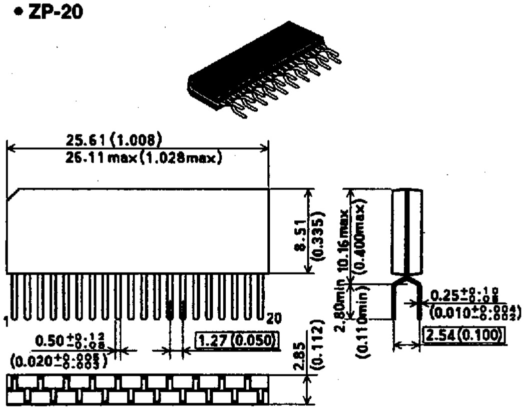


• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

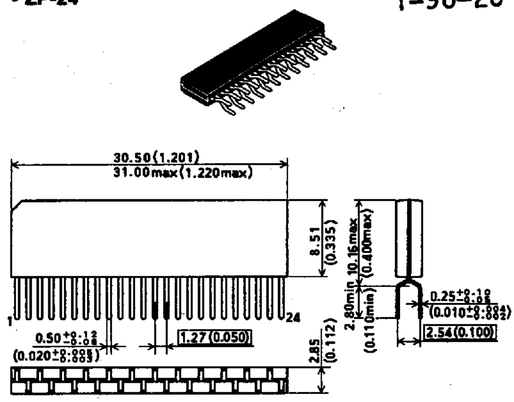
Unit: mm (inch) Scale 3/2

T-90-20

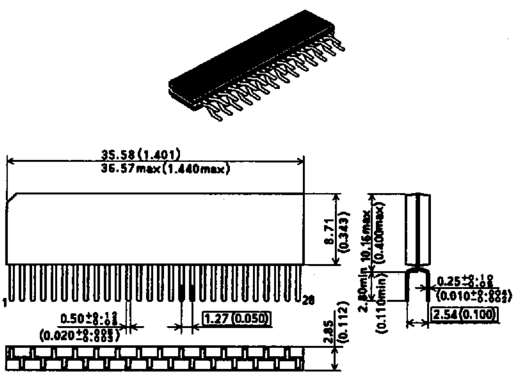
• ZP-20



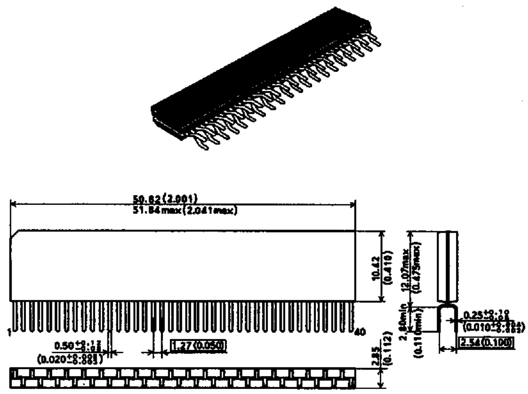
• ZP-24



• ZP-28



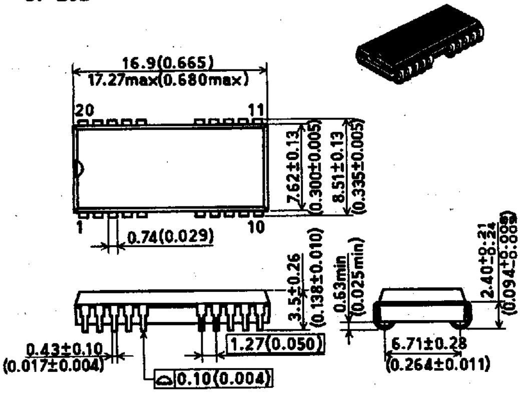
• ZP-40



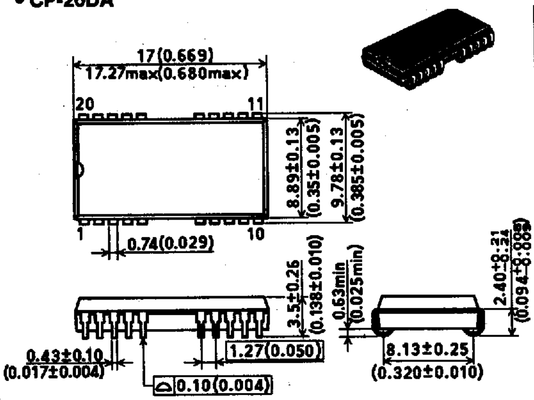
• Flat Package (J-bend Leads) HITACHI/ LOGIC/ARRAYS/MEM Unit: mm (inch) Scale 3/2

T-90-20

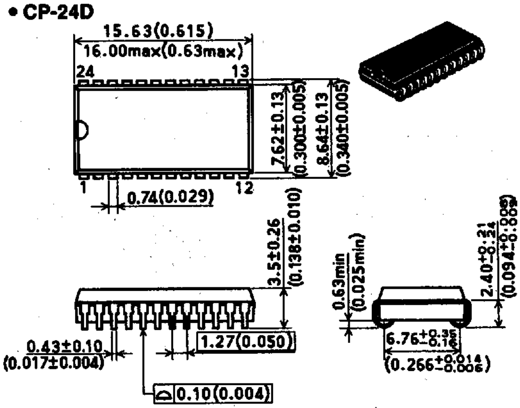
• CP-20D



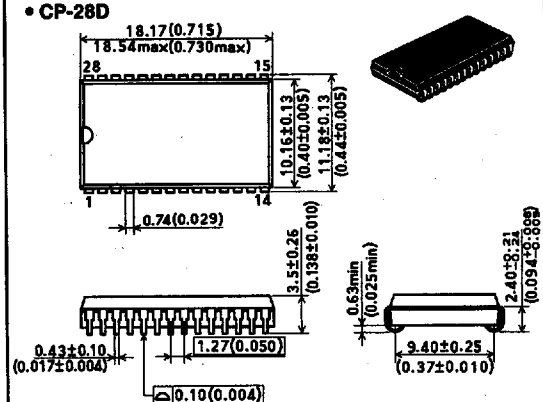
• CP-20DA



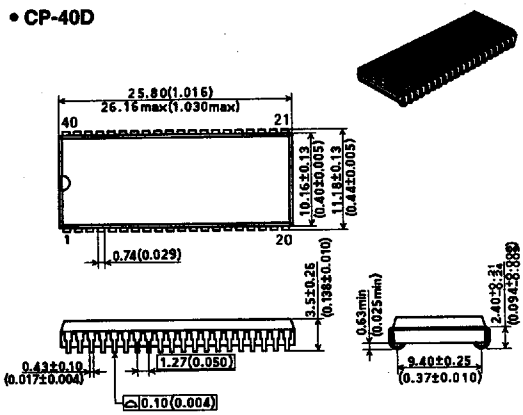
• CP-24D



• CP-28D



• CP-40D

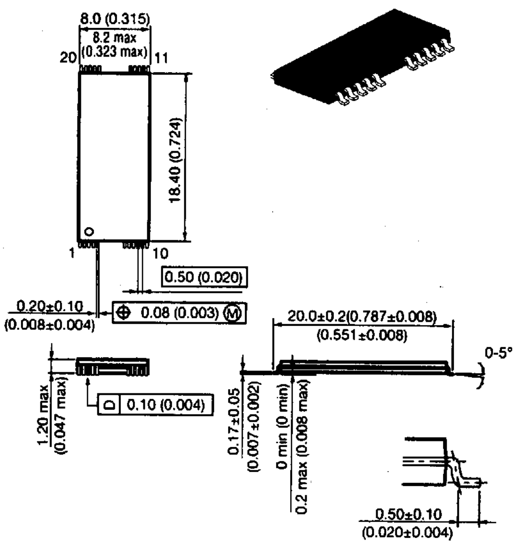


HITACHI/ LOGIC/ARRAYS/MEM

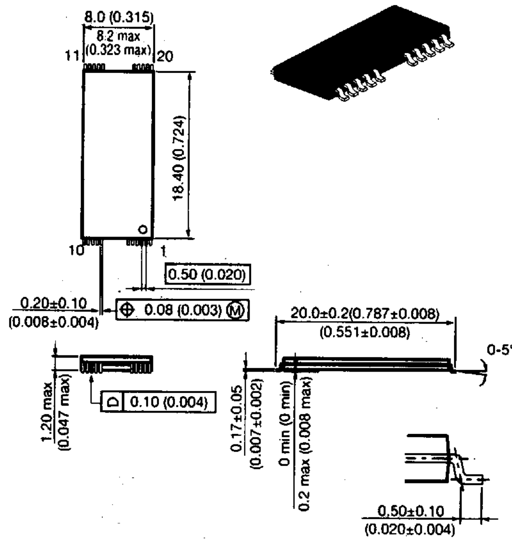
• TSOP (Thin Small Outline Package) Unit: mm (inch) Scale 3/2

T-90-20

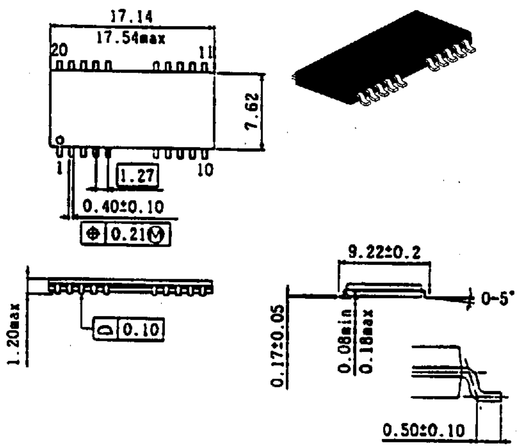
• TFP-20DA



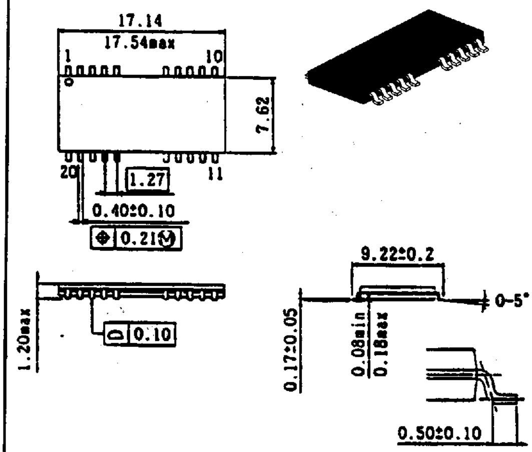
• TFP-20DAR



• TTP-20D



• TTP-20DR



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