

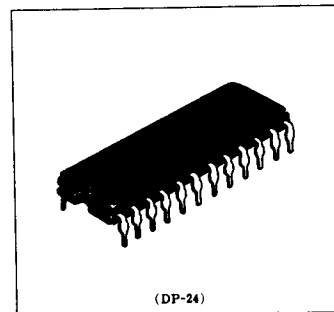
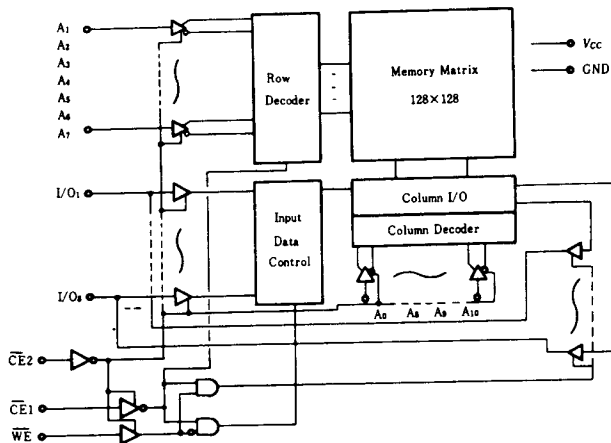
HM6117P-3, HM6117P-4

2048-word × 8-bit High Speed Static CMOS RAM

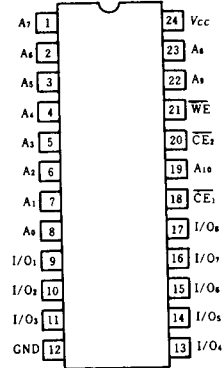
FEATURES

- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (typ.)
- Low Power Operation: Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{mb}	-10 to +85	°C

* Pulse width 50ns: -1.5V

TRUTH TABLE

$\overline{CE}_1$	$\overline{CE}_2$	WE	Mode	V_{CC} Current	I/O Pin
H	x	x	Not Selected	I_{ccL1}	High Z
x	H	x	Not Selected	I_{ccL2}	High Z
L	L	H	Read	I_{cc}	Dout
L	L	L	Write	I_{cc}	Din

RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-1.0*	—	0.8	V

* Pulse width: 50ns, DC: $V_{ILmax} = -0.3\text{V}$

DC AND OPERATING CHARACTERISTICS ($T_a = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, GND = 0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{IL} = \text{GND to } V_{CC}$	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CE}}_1 = V_{IH}$ or $\overline{\text{CE}}_2 = V_{IH}$ $V_{ILO} = \text{GND to } V_{CC}$	—	—	10	μA
Operating Power Supply Current: DC	I_{CC}	$\overline{\text{CE}}_1 = \overline{\text{CE}}_2 = V_{IL}$, $I_{ILO} = 0\text{mA}$	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{\text{CE}}_1 = V_{IL}$, $\overline{\text{CE}}_2 = V_{IL}$	—	40	80	mA
Standby Power Supply Current (1): DC	I_{CC1}^*	$\overline{\text{CE}}_1 \geq V_{CC} - 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	—	0.02	2	mA
Standby Power Supply Current (2): DC	I_{CC2}^*	$\overline{\text{CE}}_2 \geq V_{CC} - 0.2\text{V}$	—	0.02	2	mA
Output low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	V

Notes: 1) Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = +25^{\circ}\text{C}$

2) * : $V_{ILmax} = -0.3\text{V}$

CAPACITANCE ($T_a = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	3	5	pF
Input/Output Capacitance	C_{IO}	$V_{ILO} = 0\text{V}$	5	7	pF

Note: This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($T_a = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ unless otherwise noted)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

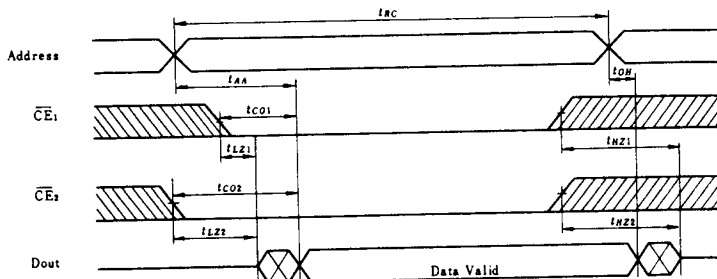
Input and Output Timing Reference Levels: 1.5V

Output Load: 1 TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{\text{CE}}_1$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{\text{CE}}_2$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{\text{CE}}_1$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{\text{CE}}_2$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{\text{CE}}_1$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{\text{CE}}_2$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

●TIMING WAVEFORM OF READ CYCLE (Notes 1)

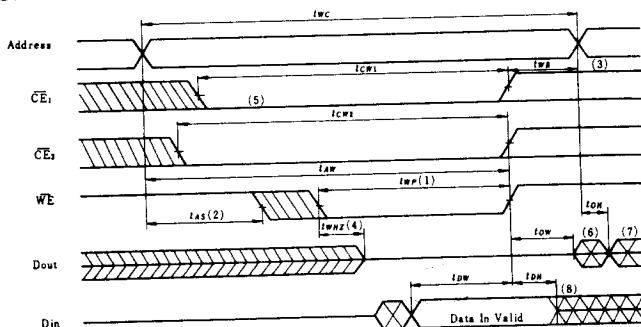


NOTES: 1. $\overline{WE}$ is High for Read Cycle.

●WRITE CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHz}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

●TIMING WAVEFORM OF WRITE CYCLE

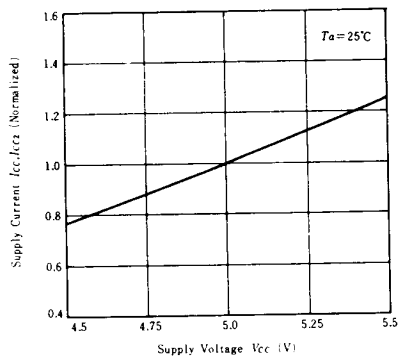


- NOTES: 1. A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the beginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end/of write cycle.

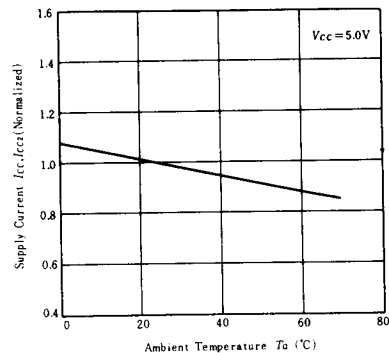
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.

6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

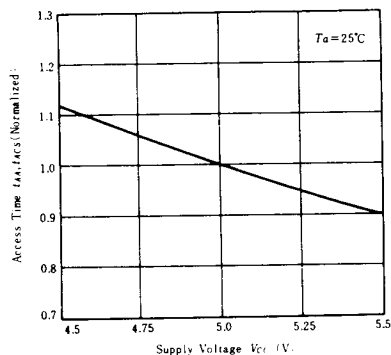
**SUPPLY CURRENT
vs. SUPPLY VOLTAGE**



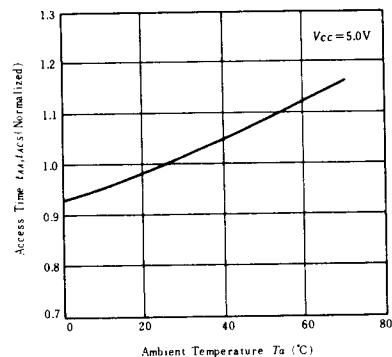
**SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**



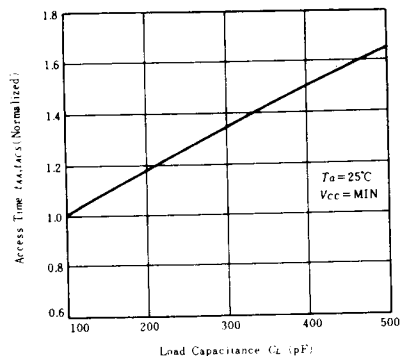
**ACCESS TIME
vs. SUPPLY VOLTAGE**



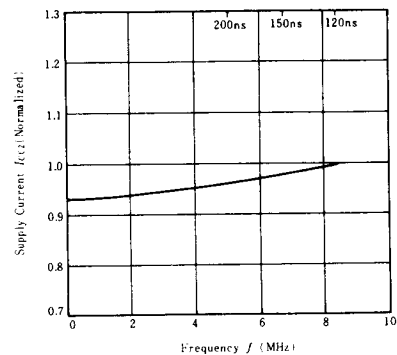
**ACCESS TIME
vs. AMBIENT TEMPERATURE**



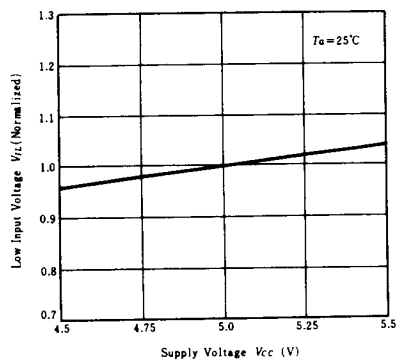
**ACCESS TIME
vs. LOAD CAPACITANCE**



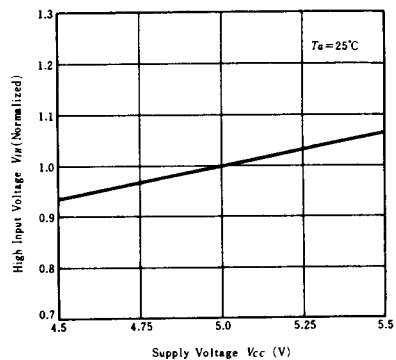
**SUPPLY CURRENT
vs. FREQUENCY**



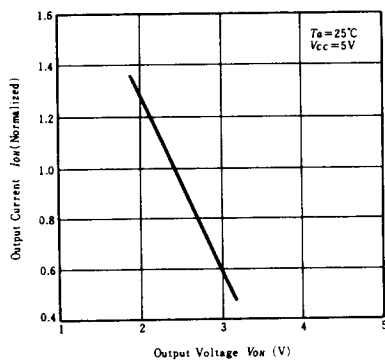
**INPUT LOW VOLTAGE
vs. SUPPLY VOLTAGE**



**INPUT HIGH VOLTAGE
vs. SUPPLY VOLTAGE**



**OUTPUT HIGH CURRENT
vs. OUTPUT HIGH VOLTAGE**



**OUTPUT LOW CURRENT
vs. OUTPUT LOW VOLTAGE**

