

16384-word x 1-bit High Speed CMOS Static RAM

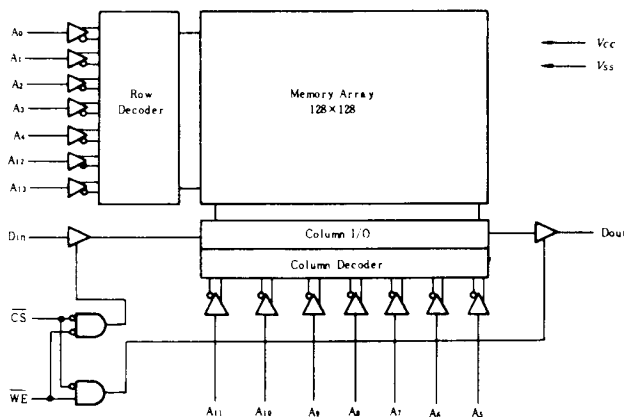
FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time – 85ns/100ns
- Low Power Stand-by and Low Power Operation
Stand-by $100\mu\text{W}$ typ./ $5\mu\text{W}$ typ. (L-version)
and Operating 150mW typ.
- Completely Static Memory No Clock nor Refresh Required
- Fully TTL Compatible – All Inputs and Output
- Separate Data Input and Output Three State Output
- Pin-Out Compatible with Intel 2167 Series
- Capability of Battery Back Up Operation (L-version)

ORDERING INFORMATION

Type No.	Access Time	Package
HM6167P-6	85ns	300mil 20pin Plastic DIP
HM6167P-8	100ns	
HM6167LP-6	85ns	
HM6167LP-8	100ns	

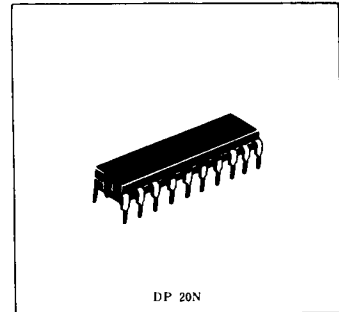
BLOCK DIAGRAM



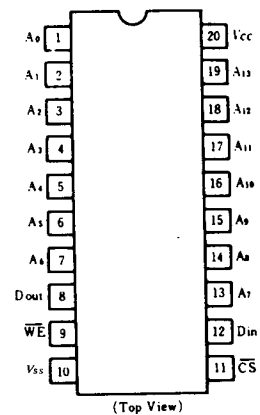
ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	-0.5^{*1} to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to $+70$	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to $+125$	$^{\circ}\text{C}$
Storage Temperature under bias	$T_{stg(bias)}$	-10 to $+85$	$^{\circ}\text{C}$

Note) *1. -3.5V for pulse width $\leq 20\text{ns}$



PIN ARRANGEMENT



■ RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.3^{*1}	—	0.8	V

Note) *1. -3.0V for pulse width $\leq 20\text{ns}$.

■ TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	x	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Item	Symbol	Test Conditions	min	typ ^{*1}	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{IN}=0\text{V} \sim V_{CC}$	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$, $V_{OUT}=0\text{V} \sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}$, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	5	20	mA
	I_{SB1}	$\overline{\text{CS}}=V_{CC}-0.2\text{V}$	—	0.02	2	mA
		$V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	—	1 ^{*2}	50 ^{*2}	μA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4\text{mA}$	2.4	—	—	V

Notes) *1. Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=25^{\circ}\text{C}$ and specified loading.

*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE ($T_a=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	$V_{IN}=0\text{V}$
Output Capacitance	C_{OUT}	6	pF	$V_{OUT}=0\text{V}$

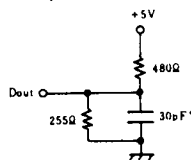
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^{\circ}\text{C}$, unless otherwise noted)

● AC TEST CONDITIONS

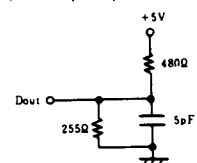
Input pulse levels: V_{SS} to 3.0V
 Input rise and fall times: 5ns
 Input timing reference levels: 1.5V
 Output reference levels: 1.5V
 Output load: See Figure

Output Load A



Output Load B

(for t_{HZ} , t_{LZ} , t_{WZ} & t_{OW})



* Including scope and jig.



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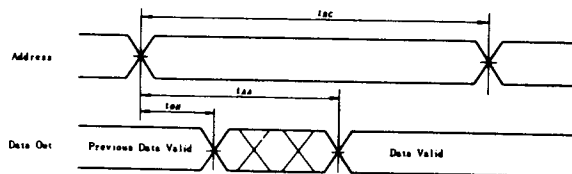
● READ CYCLE

Item	Symbol	HM6167-6		HM6167-8		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	85	—	100	—	ns
Address Access Time	t_{AA}	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	40	—	45	ns

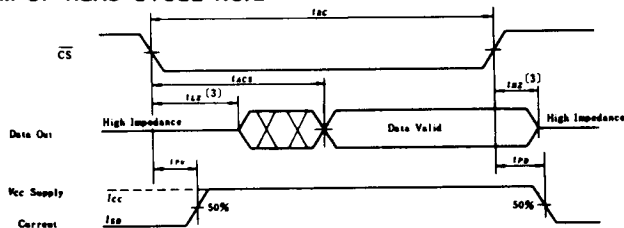
● WRITE CYCLE

Item	Symbol	HM6167-6		HM6167-8		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

- Notes: 1. If CS goes high simultaneously with WE high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 500 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

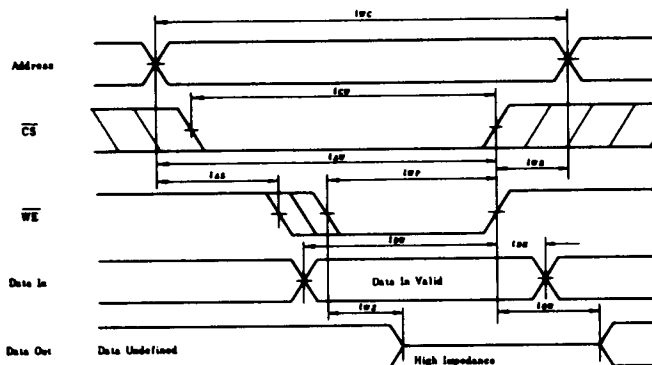
● TIMING WAVEFORM OF READ CYCLE NO.1¹⁾

●TIMING WAVEFORM OF READ CYCLE NO.2^{1), 3)}

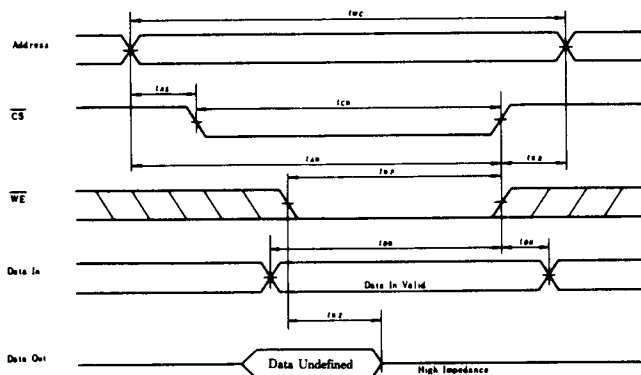


- NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
 2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

●TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ Controlled)



●TIMING WAVEFORM OF WRITE CYCLE No. 2 ($\overline{CS}$ Controlled)



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■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

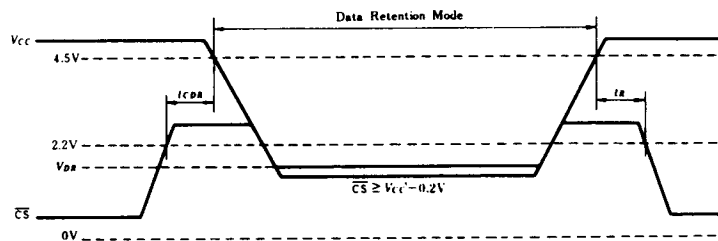
Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{\alpha} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{\alpha} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*2	μA
Chip Deselect to Data Retention Time	t_{CDR}		—	—	30*3	μs
Operation Recovery Time	t_R		0	—	—	ns
			$t_{ac} * 1$	—	—	ns

Notes) *1. t_{ac} —Read Cycle Time

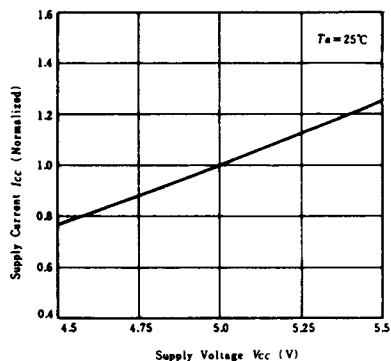
*2. $V_{CC} = 2.0\text{V}$

*3. $V_{CC} = 3.0\text{V}$

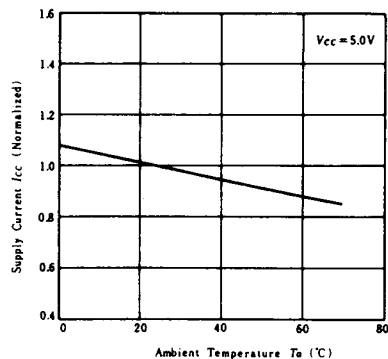
● LOW V_{CC} DATA RETENTION WAVEFORM

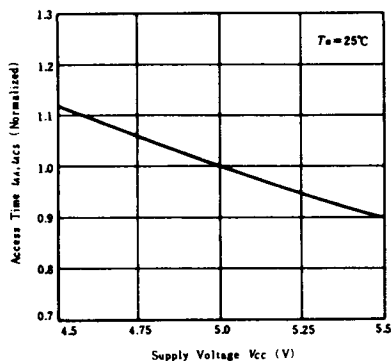
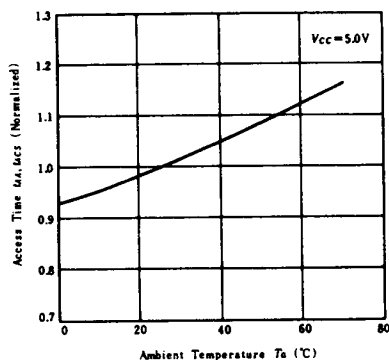
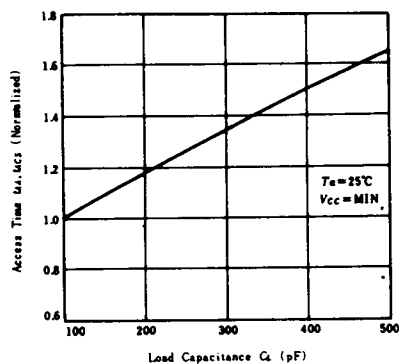
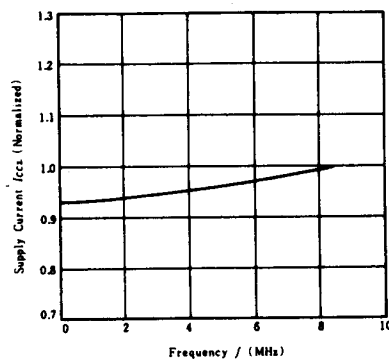
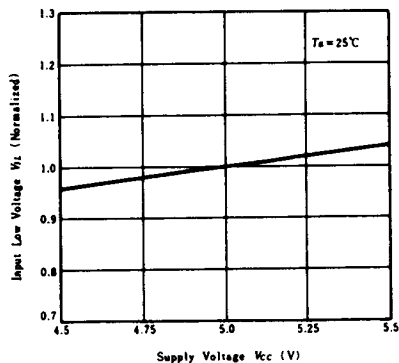
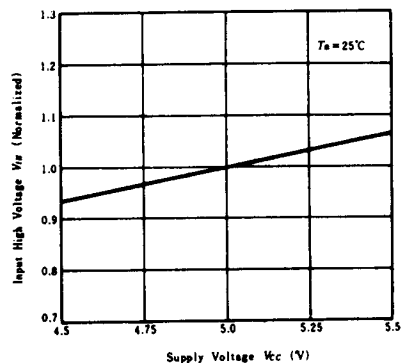


SUPPLY CURRENT vs. SUPPLY VOLTAGE

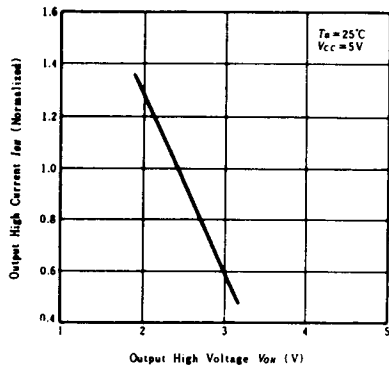


SUPPLY CURRENT vs. AMBIENT TEMPERATURE

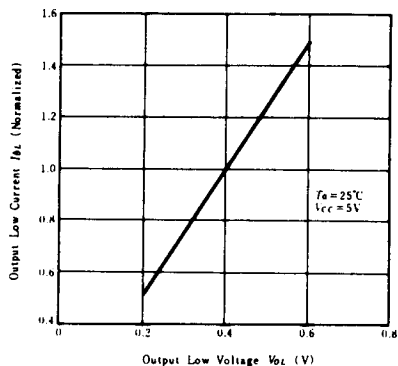


**ACCESS TIME vs.
SUPPLY VOLTAGE****ACCESS TIME vs.
AMBIENT TEMPERATURE****ACCESS TIME vs.
LOAD CAPACITANCE****SUPPLY CURRENT vs.
FREQUENCY****INPUT LOW VOLTAGE vs.
SUPPLY VOLTAGE****INPUT HIGH VOLTAGE vs.
SUPPLY VOLTAGE**

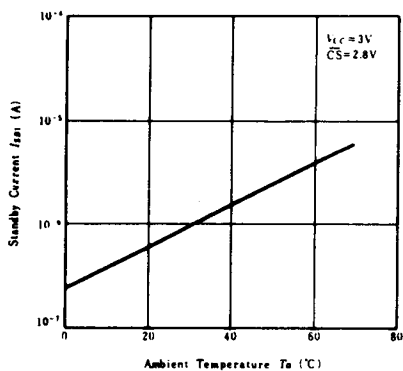
**OUTPUT HIGH CURRENT vs.
OUTPUT HIGH VOLTAGE**



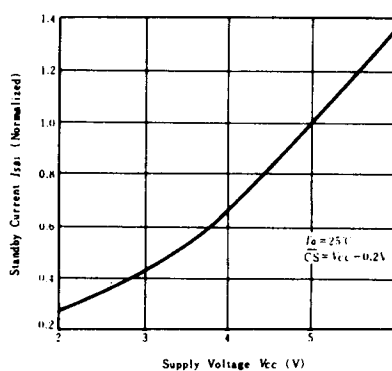
**OUTPUT LOW CURRENT vs.
OUTPUT LOW VOLTAGE**



**STANDBY CURRENT vs.
AMBIENT TEMPERATURE**



**STANDBY CURRENT vs.
SUPPLY VOLTAGE**



**STANDBY CURRENT vs.
INPUT VOLTAGE**

