

HM621400 Series

Preliminary

4,194,304-Word x 1-Bit High Speed CMOS Static RAM

T-46-23-05

■ FEATURES

- High Speed:
Fast access time 25/30/35/45 ns(max.) (P-version)
30/35/45 ns(max.) (LP-version)
- Single 5V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- TTL compatible: All inputs and outputs
- Thin plastic package for high density mounting

■ ORDERING INFORMATION

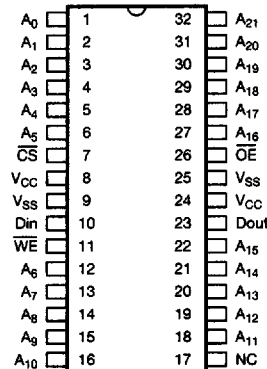
Type No.	Access Time	Package
HM621400JP-25	25 ns	400-mil, 32 pin SOJ (CP-32D)
HM621400JP-30	30 ns	
HM621400JP-35	35 ns	
HM621400JP-45	45 ns	
HM621400JLP-30	30 ns	32-pin TSOP (II)
HM621400JLP-35	35 ns	
HM621400JLP-45	45 ns	
HM621400P-25	25 ns	
HM621400P-30	30 ns	
HM621400P-35	35 ns	
HM621400P-45	45 ns	
HM621400LP-30	30 ns	
HM621400LP-35	35 ns	
HM621400LP-45	45 ns	



(CP-32D)

■ PIN ARRANGEMENT

HM621400 Series



(Top View)

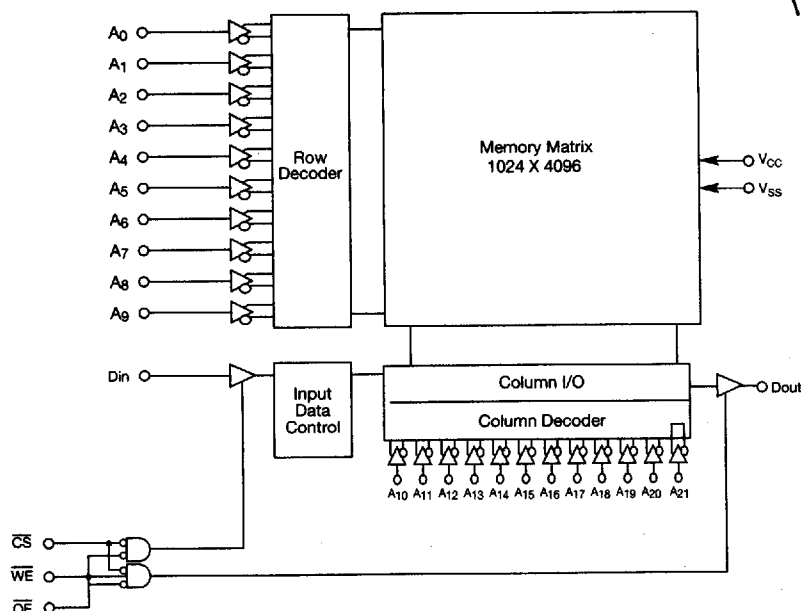
■ PIN DESCRIPTION

Pin Name	Function
A0-A21	Address Input
DIN	Data Input
DOUT	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
VSS	Ground
NC	No Connection



■ BLOCK DIAGRAM

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■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	WE	Mode	VCC Current	Dout Pin	Ref. Cycle
H	X	X	Deselect	ISB, ISBI	High-Z	—
L	L	H	Read	ICC	Dout	Read Cycle 1, 2, 3
L	H	L	Write	ICC	Din	Write Cycle 1
L	L	L	Write	ICC	Din	Write Cycle 2

Note: X: H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to VSS	V_T	-0.5^{*1} to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to $+70$	$^{\circ}C$
Storage Temperature	T_{stg}	-55 to $+125$	$^{\circ}C$
Storage Temperature Under Bias	T_{bias}	-10 to $+85$	$^{\circ}C$

Note 1. V_T min. = $-2.0V$ for pulse width ≤ 10 ns■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^{\circ}C$)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
	VSS	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.5^{*1}	—	0.8	V

Note 1. V_{IL} min. = $-2.0V$ for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

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Item	Symbol	HM621400P					HM621400LP				
		Min	Typ	Max	Unit	Test Conditions	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	$ I_{Li} $	—	—	2.0	μA	$V_{CC} = \text{Max.}$ $V_{in} = V_{SS} \text{ to } V_{CC}$	—	—	2.0	μA	$V_{CC} = \text{Max.}$ $V_{in} = V_{SS} \text{ to } V_{CC}$
Output Leakage Current	$ I_{LO} $	—	—	2.0	μA	$\overline{CS} = V_{IH}$ $V_{I/O} = V_{SS} \text{ to } V_{CC}$	—	—	2.0	μA	$\overline{CS} = V_{IH}$ $V_{I/O} = V_{SS} \text{ to } V_{CC}$
Operating V_{CC} Current	I_{CC}	—	—	150	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0 \text{ mA}$ Cycle = 25 ns	—	—	140	mA	$\overline{CS} = V_{IL}$, $I_{I/O} = 0 \text{ mA}$ Cycle = 30 ns
Standby V_{CC} Current	I_{SB}	—	—	60	mA	$\overline{CS} = V_{IH}$, Cycle = 25 ns	—	—	5	mA	$\overline{CS} = V_{IH}$, Cycle = 30 ns
	I_{SB1}	—	—	10	mA	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $0\text{V} \leq V_{in} \leq 0.2\text{V}$ or $V_{in} \geq V_{CC} - 0.2\text{V}$	—	—	0.1	mA	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $0\text{V} \leq V_{in} \leq 0.2\text{V}$ or $V_{in} \geq V_{CC} - 0.2\text{V}$
Output Voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8 \text{ mA}$	—	—	0.4	V	$I_{OL} = 8 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -4 \text{ mA}$	2.4	—	—	V	$I_{OH} = -4 \text{ mA}$

■ CAPACITANCE ($T_a = 25^\circ\text{C}$; $f = 1 \text{ MHz}$)

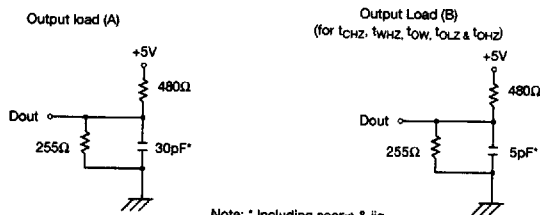
Item	Symbol	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	$V_{in} = 0\text{V}$
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O} = 0\text{V}$

Note 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} 5\text{V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 4ns
- Input and Output timing reference levels: Input 1.5V
Output 1.5V
- Output load: See Figures



Note: * Including scope & jig.

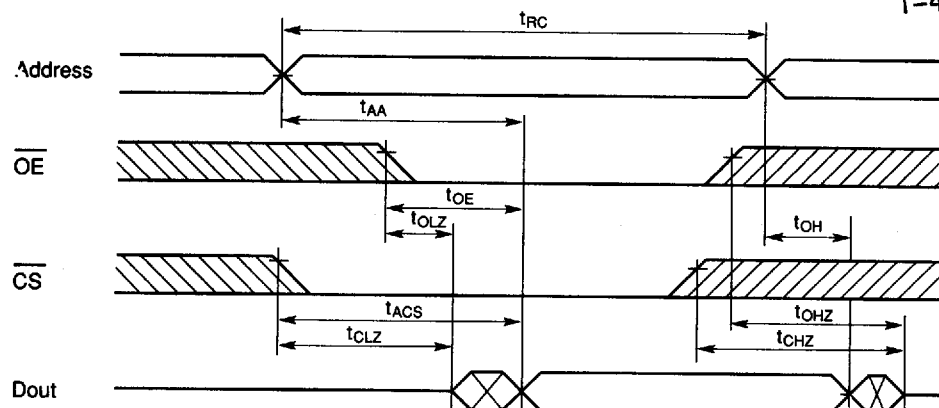
■ READ CYCLE

Item	Symbol	HM621400-25P		HM621400-30P/LP		HM621400-35P/LP		HM621400-45P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}^{*1}	5	—	5	—	5	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	15	—	20	ns
Output Enable to Output in Low-Z	t_{OLZ}^{*1}	0	—	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}^{*1}	0	10	0	10	0	15	0	15	ns
Chip Disable to Output in High-Z	t_{OHZ}^{*1}	0	10	0	10	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	30	—	30	ns

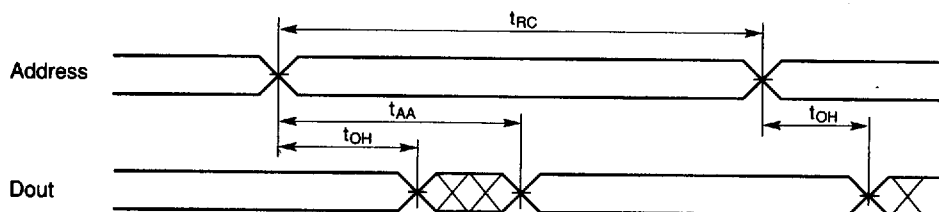


■ READ TIMING WAVEFORM (1)*1, *2

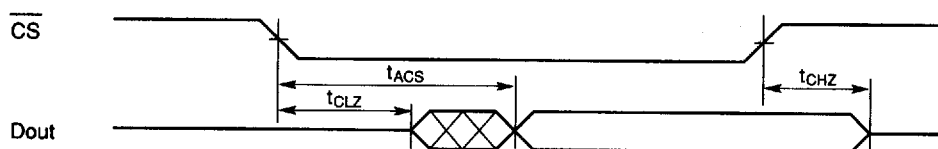
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■ READ TIMING WAVEFORM (2)*2, *3, *5



■ READ TIMING WAVEFORM (3)*1, *2, *4, *5

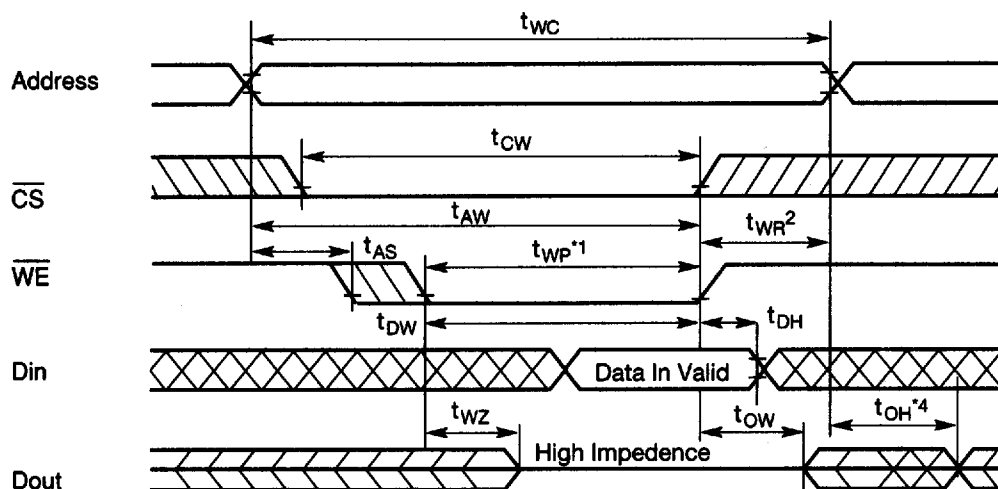


- Notes:
1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
 2. $\overline{WE}$ is high for read cycle.
 3. $\overline{CS}$ is low.
 4. Address valid prior to or coincident with $\overline{CS}$ transition low.
 5. $\overline{OE} = V_{IL}$.



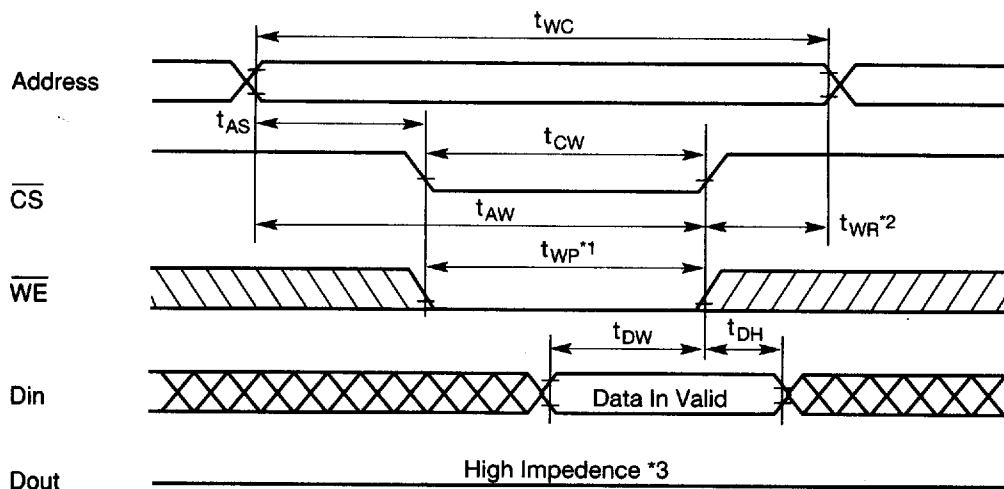
■ WRITE CYCLE

Parameter	Symbol	HM621400-25P		HM621400-30P/LP		HM621400-35P/LP		HM621400-45P/LP		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	25	—	30	—	35	—	45	—	ns	
Chip Selection to End of Write	t_{CW}	15	—	20	—	25	—	35	—	ns	
Address Valid to End of Write	t_{AW}	15	—	20	—	25	—	35	—	ns	
Address setup Time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	15	—	20	—	25	—	35	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	5	—	0	—	ns	
Output Disable to Output in High-Z	t_{OHZ}^{*5}	0	10	0	10	0	15	0	15	ns	
Write to Output in High-Z	t_{WHZ}^{*5}	0	10	0	10	0	15	0	15	ns	
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	30	—	ns	
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns	
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	0	—	ns	

■ WRITE TIMING WAVEFORM (1) ($\overline{WE}$ Controlled)

■ WRITE TIMING WAVEFORM (2) ($\overline{CS}$ Controlled)

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- Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
 2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
 3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
 4. Dout is the same phase of write data of this write cycle.
 5. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.



■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{in} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{in} \leq 0.2\text{V}$
Data Retention Current	I_{CCDR}	—	—	100^{*1}	μA	
Chip Select to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: 1. $V_{CC} = 3.0\text{V}$.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM

