HM624100 Series

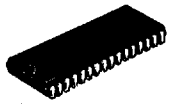
Preliminary

T-46-23-10

1,048,576-Word x 4-Bit High Speed CMOS Static Ram

■ FEATURES

- High Speed:
  Fast access time 25/30/35/45 ns(max.) (P-version)
  30/35/45 ns (max.) (LP-version)
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle time
- TTL compatible–All inputs and outputs
- Thin plastic package for high density mounting



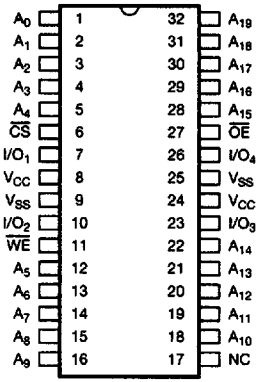
(CP-32D)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624100JP-25	25 ns	400 mil 32-pin SOJ (CP-32D)
HM624100JP-30	30 ns	
HM624100JP-35	35 ns	
HM624100JP-40	45 ns	
HM624100JLP-30	30ns	
HM624100JLP-35	35ns	
HM624100JLP-45	45ns	
HM624100P-25	25ns	32-pin TSOP (II)
HM624100P-30	30ns	
HM624100P-35	35ns	
HM624100P-45	45ns	
HM624100LP-30	30ns	
HM624100LP-35	35ns	
HM624100LP-45	45ns	

■ PIN ARRANGEMENT

HM624100 Series



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A19	Address Input
I/O1–I/O4	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
VSS	Ground
NC	No Connection

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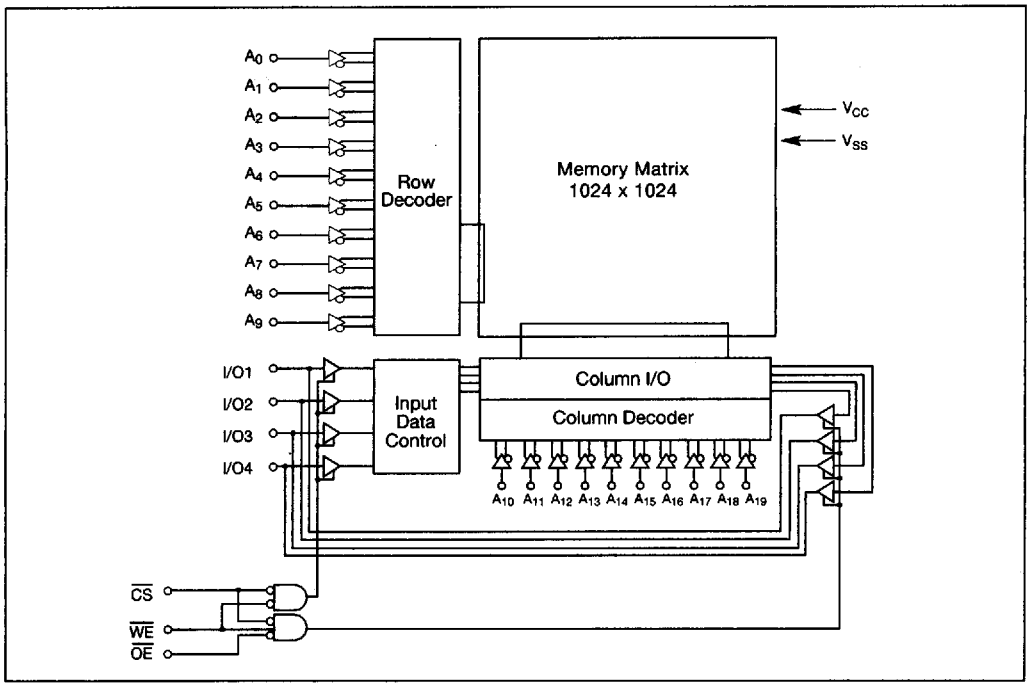
BLOCK DIAGRAM



FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Deselect	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read Cycle 1, 2, 3
L	H	L	Write	I_{CC}	Din	Write Cycle 1
L	L	L	Write	I_{CC}	Din	Write Cycle 2

Note: X: H or L

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5[1] to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

Note: 1. V_T min = −2.0 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	–0.5[1]	—	0.8	V

Note: 1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	HM624100P			HM624100LP			Unit	Test Conditions
		Min.	Typ	Max.	Min.	Typ	Max.		
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC}	—	—	150	—	—	140	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Cycle=25 ns. (P), 35 ns. (LP)
Standby VCC Current	I_{SB}	—	—	60	—	—	5	mA	$\overline{CS}$ = V_{IH} Cycle=25 ns. (P), 35 ns. (LP)
	I_{SB1}	—	—	10	—	—	0.1	mA	$\overline{CS}$ ≥ V_{CC} –0.2V 0 V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} –0.2V
Output Low Voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}= 8mA
	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4mA

■ CAPACITANCE (Ta = 25°C, f= 1 MHz)

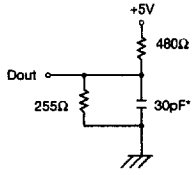
Item	Symbol	Min	Max	Unit	Test Conditions
Input Capacitance	C_{in}	—	5	pF	V_{in} = 0 V
Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

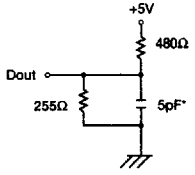
Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See Figures



Output Load (A)

* Including scope & jig.

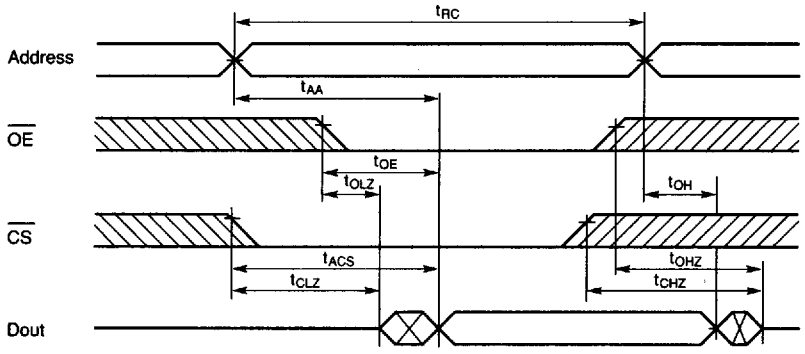


Output Load (B)
(for t_{CHZ}, t_{CLZ}, t_{WHZ} & t_{OW})

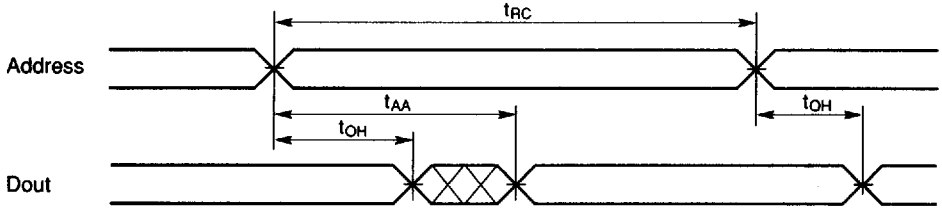
■ READ CYCLE

Item	Symbol	HM624100-25 P		HM624100-30 P/LP		HM624100-35 P/L		HM624100-45 P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}[1]	5	—	5	—	5	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	15	—	20	ns
Output Enable to Output in Low-Z	t_{OLZ}[1]	0	—	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}[1]	0	10	0	10	0	15	0	15	ns
Chip Disable to Output in High-Z	t_{OHZ}[1]	0	10	0	10	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	30	—	20	ns

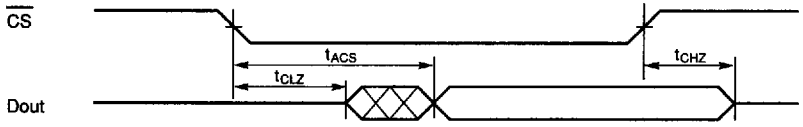
■ READ TIMING WAVEFORM (1) [1, 2]



■ READ TIMING WAVEFORM (2) [2, 3, 5]



■ READ TIMING WAVEFORM (3) [1, 2, 4, 5]



Notes: 1. Transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. $\overline{CS}$ is low.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE}$ = V_{IL}.

■ WRITE CYCLE

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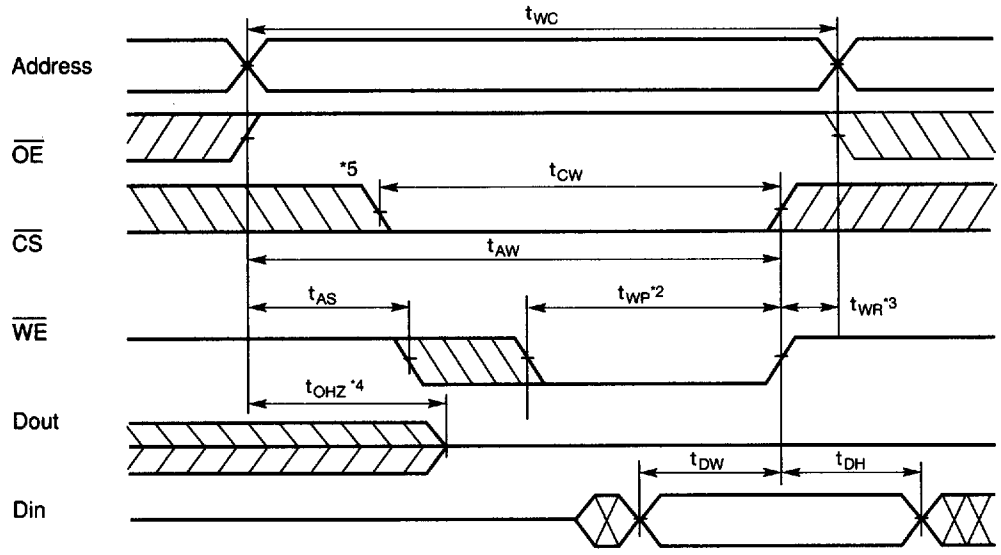
Parameter	Symbol	HM624100-25 P		HM624100-30 P/LP		HM624100-35 P/L		HM624100-45 P/LP		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	25	—	30	—	35	—	45	—	ns
Chip Selection to End of Write	tCW	15	—	20	—	25	—	35	—	ns
Address Valid to End of Write	tAW	15	—	20	—	25	—	35	—	ns
Address Setup Time	tAS	0	—	0	—	0	—	0	—	ns
Write Pulse Width	tWP	15	—	20	—	25	—	35	—	ns
Write Recovery Time	tWR	0	—	0	—	0	—	0	—	ns
Output Disable to Output in High-Z	tOHZ	0	10	0	10	0	15	0	15	ns
Write to Output in High-Z[1]	tWHZ	0	10	0	10	0	15	0	15	ns
Data to Write Time Overlap	tDW	12	—	15	—	20	—	30	—	ns
Data Hold from Write Time	tDH	0	—	0	—	0	—	0	—	ns
Output Active from End of Write	tOW	0	—	0	—	0	—	0	—	ns

■ WRITE TIMING WAVEFORM (1)



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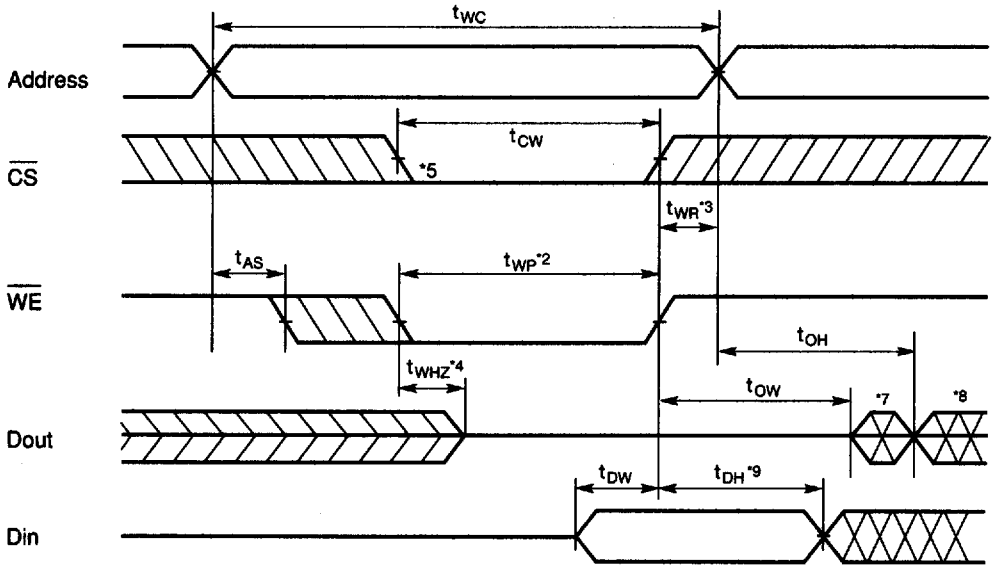
■ WRITE TIMING WAVEFORM (2) [6]



Notes:
1. Transition is measured ± 200 mV from high impedance voltage with Load (B). This parameter is sampled not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or WE going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the WE transition, output remain a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

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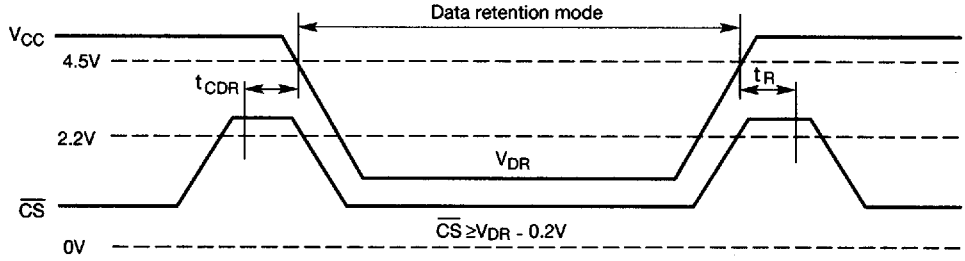
This characteristic is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$–0.2V, $V_{in} \geq V_{CC}$ -0.2V or 0V ≤ V_{in} ≤ 0.2V
Data Retention Current	I_{CCDR}	—	—	100[1]	µA	
Chip Select to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

Note: V_{CC} = 3.0 V.

■ LOW V_{CC} DATA RETENTION TIMING WAVEFORM



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