T-46-23-10

HM624100 Series — Preliminary

1048576-word × 4-bit High Speed CMOS Static RAM

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM624100 is a high speed CMOS static RAM organized 1-Mword × 4bit. It realizes higher performance and low power consumption by employing 0.6μm Hi-CMOS process technology. The device, packaged in a SOJ or TSOP is available for high density mounting.

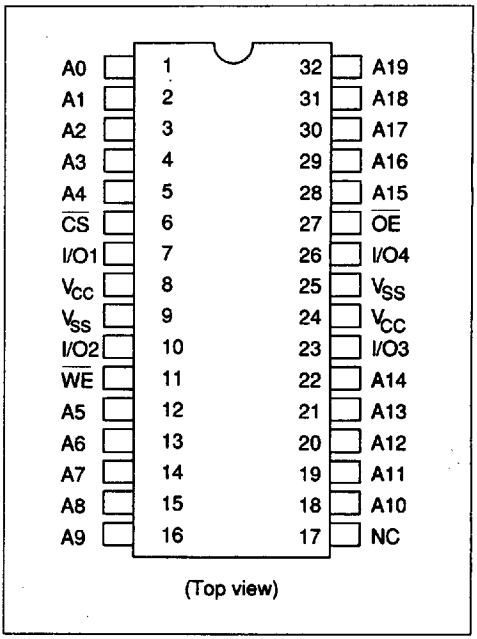
Features

- High speed
  - — Access time:
    - 25/30/35 ns (max)(P-version)
    - 30/35/45 ns (max)(LP-version)
- Single 5 V supply
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle time
- TTL compatible
  - — All inputs and outputs
- Thin plastic package for high density mounting

Ordering Information

Type No.	Access time	Package
HM624100JP-25	25 ns	400-mil 32-pin SOJ (CP-32DB)
HM624100JP-30	30 ns	
HM624100JP-35	35 ns	
HM624100LJP-30	30 ns	
HM624100LJP-35	35 ns	
HM624100LJP-45	45 ns	
HM624100TT-25	25 ns	400-mil 32-pin TSOPII (TTP-32DA)
HM624100TT-30	30 ns	
HM624100TT-35	35 ns	
HM624100LTT-30	30 ns	
HM624100LTT-35	35 ns	
HM624100LTT-45	45 ns	

Pin Arrangement

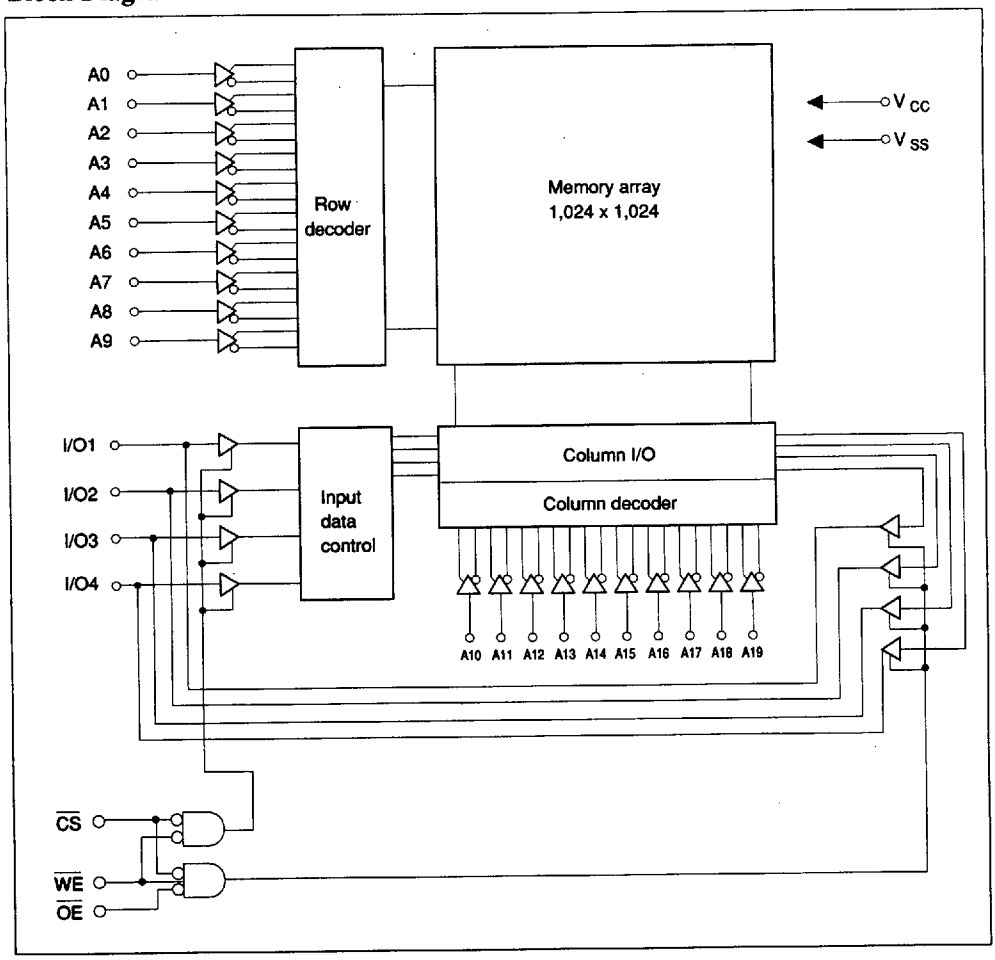


Pin Description

Pin name	Function
A0 – A19	Address input
I/O1 – I/O4	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



HM624100 Series

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Deselect	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1), (2), (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. V_T min = −2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}	−0.5 *1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM624100					HM624100L				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC}	—	—	150	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0 mA Cycle = 25 ns	—	—	140	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0 mA Cycle = 30 ns
Standby V_{CC} current	I_{SB}	—	—	60	mA	$\overline{CS}$ = V_{IH} Cycle = 25 ns	—	—	5	mA	$\overline{CS}$ = V_{IH} Cycle = 30 ns
	I_{SB1}	—	—	10	mA	$\overline{CS}$ ≥ Vcc – 0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V	—	—	0.1	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	—	—	0.4	V	I_{OL} = 8 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	2.4	—	—	V	I_{OH} = –4 mA

Capacitance (Ta = 25°C, f = 1 MHz)

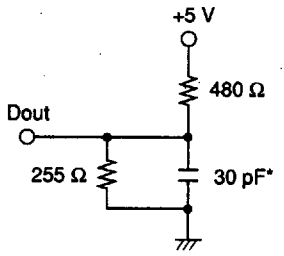
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Input capacitance	Cin	—	5	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	8	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

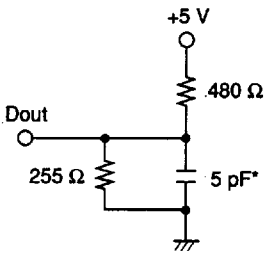
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: Vss to 3.0V
- Input rise and fall time: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures



Output Load (A)



Output Load (B)

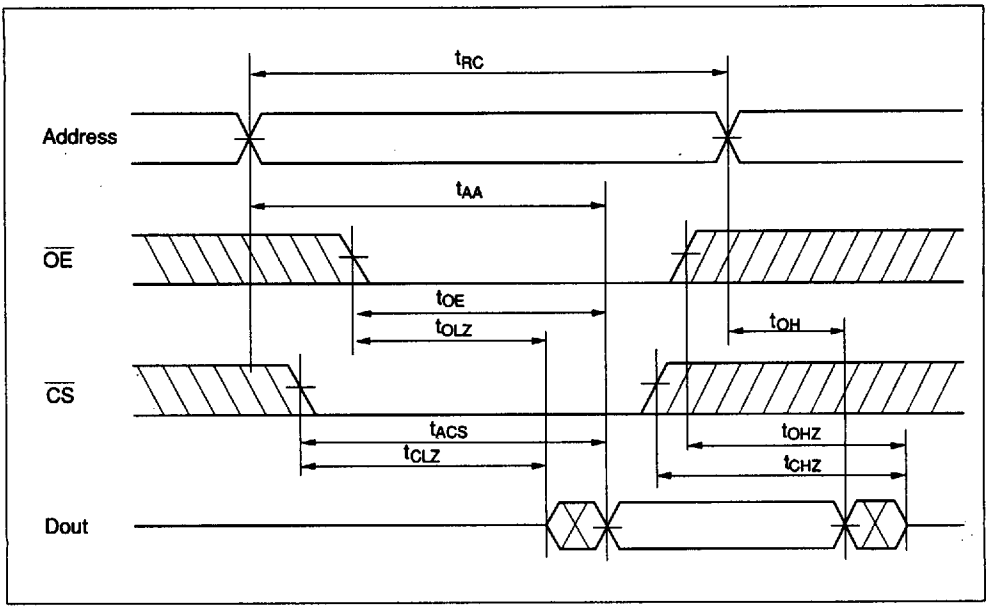
(for t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ})

* Including scope & jig

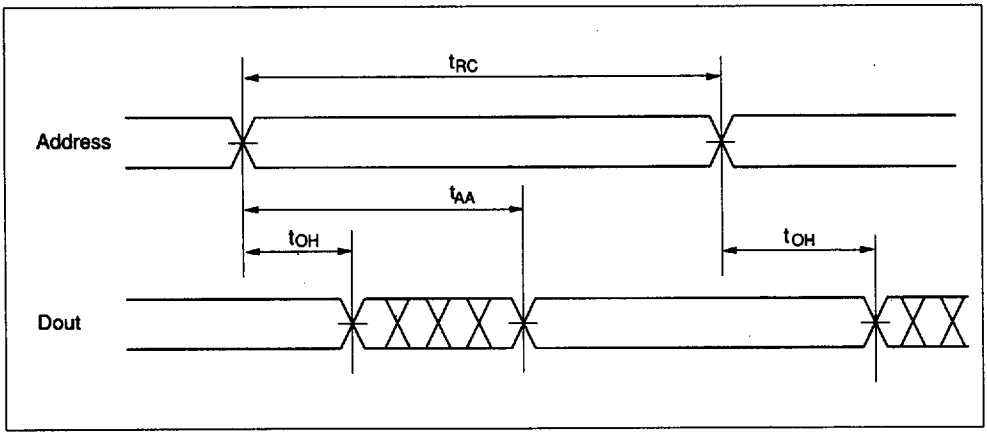
Read Cycle

Parameter	Symbol	HM624100 -25		HM624100 -30,-30L		HM624100 -35,-35L		HM624100 -45L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	30	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	30	—	35	—	45	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	5	—	10	—	ns
Output enable to output valid	t_{OE}	—	10	—	13	—	15	—	20	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	10	0	10	0	15	0	15	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	10	0	10	0	15	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	20	—	20	—	30	—	30	ns

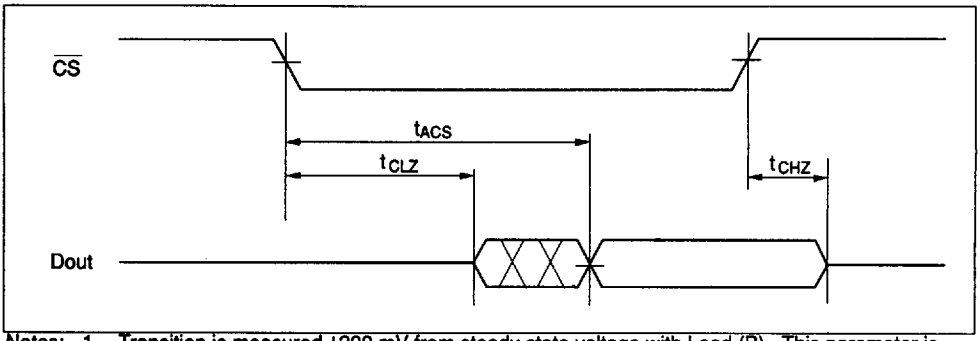
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5

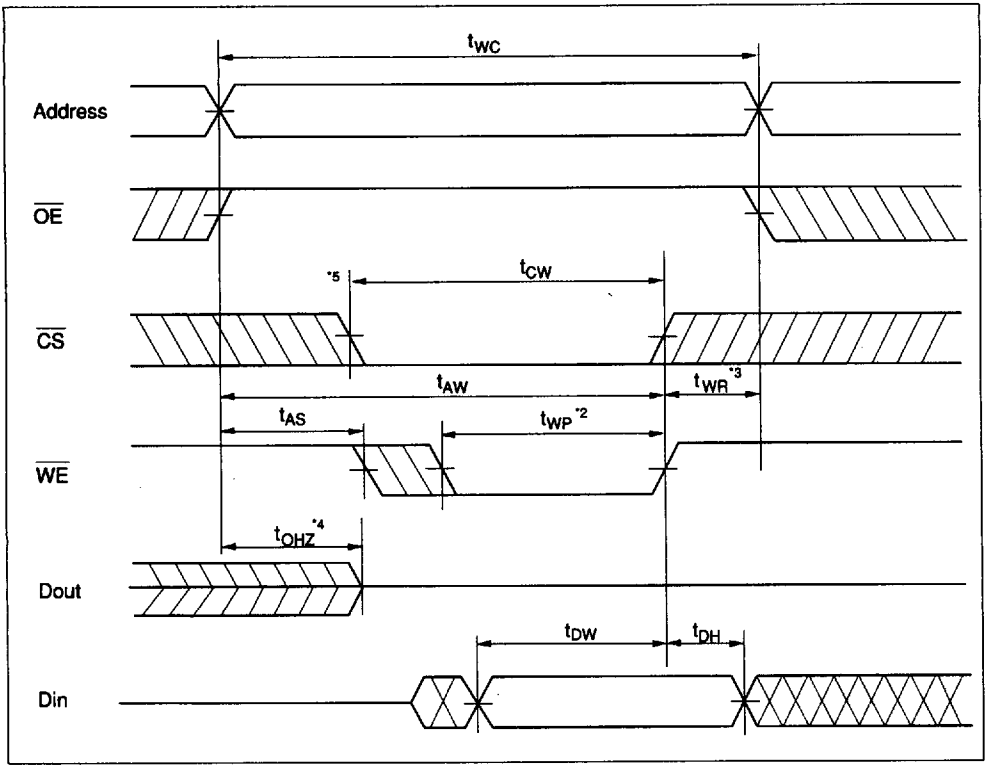


Notes: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is high for read cycle.
3. $\overline{CS}$ is low.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.
5. $\overline{OE} = V_{IL}$

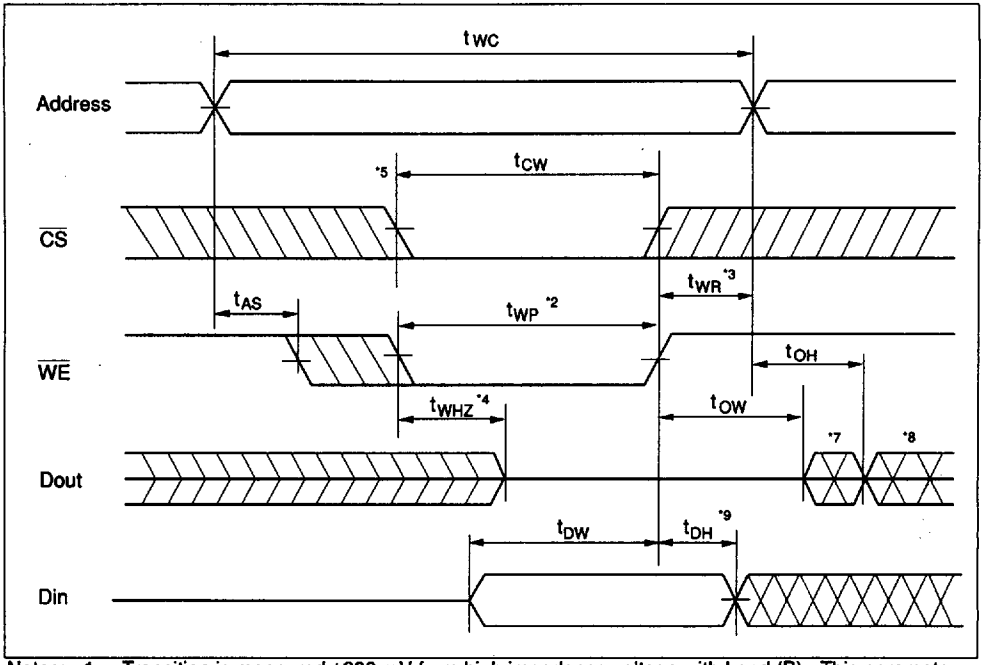
Write Cycle

		HM624100 -25		HM624100 -30,-30L		HM624100 -35,-35L		HM624100 -45L		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	25	—	30	—	35	—	45	—	ns
Chip selection to end of write	t_{CW}	15	—	20	—	25	—	35	—	ns
Address valid to end of write	t_{AW}	15	—	20	—	25	—	35	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	25	—	35	—	ns
Write recovery time	t_{WR}	3	—	3	—	3	—	3	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	10	0	10	0	15	0	15	ns
Write to output in high-Z*1	t_{WHZ}	0	10	0	10	0	15	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	20	—	30	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	0	—	0	—	0	—	0	—	ns

Write Timing Waveform (1)



Write Timing Waveform (2)*6



Notes:
1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$).
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.