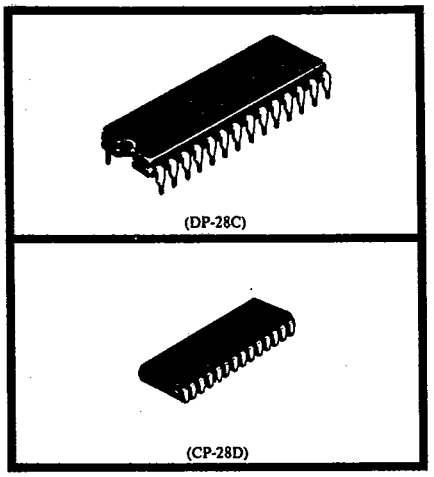
HM624256 Series

T-46-23-14

262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624256 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256, packaged in a 400-mil plastic SOJ is available for high density mounting.



(DP-28C)

(CP-28D)

■ FEATURES

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed: Fast access time 35/45 ns (max.)
- Low power
  Operation: 350 mW (typ.)
  Standby: 100 μW (typ.)
- Completely static memory:
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624256P-35	35 ns	400 mil
HM624256P-45	45 ns	28-pin
HM624256LP-35	35 ns	Plastic DIP
HM624256LP-45	45 ns	(DP28C)
HM624256JP-35	35 ns	400 mil
HM624256JP-45	45 ns	28-pin
HM624256LJP-35	35 ns	Plastic SOJ
HM624256LJP-45	45 ns	(CP-28D)

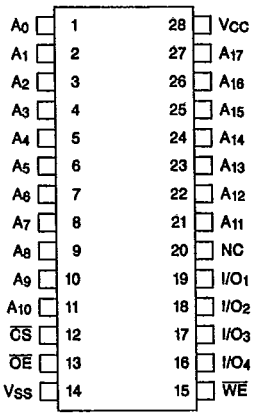
■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{17}	Address
I/O_1-I/O_4	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

PIN ARRANGEMENT

(DIP and SOJ)
Top View



■ BLOCK DIAGRAM

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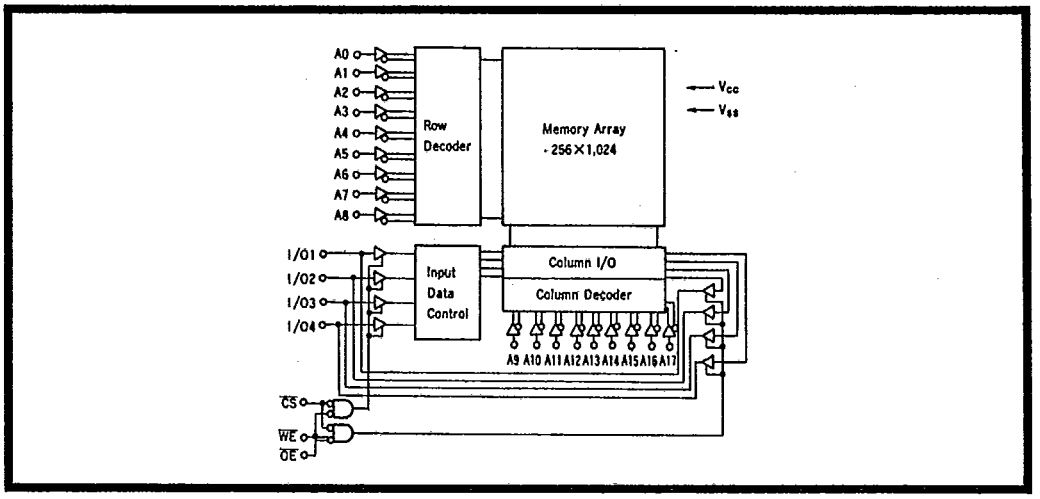

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1)-(3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle(2)

NOTE: X : H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	-0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: *1. V_T min. = -2.0 V for pulse width ≤ 10 ns.

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■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	−0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = −2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	μA	$\overline{CS}$ = V_{IH} V_{out} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, I_{out} = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}*2 I_{SB1}*3	— —	0.02 —	2.0 0.2	mA mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} − 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4.0 mA

NOTES: *1. Typical limits are at V_{CC} = 5.0 V, T_a = 25°C and specified loading.
*2. JP-version
*3. LJP-version

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

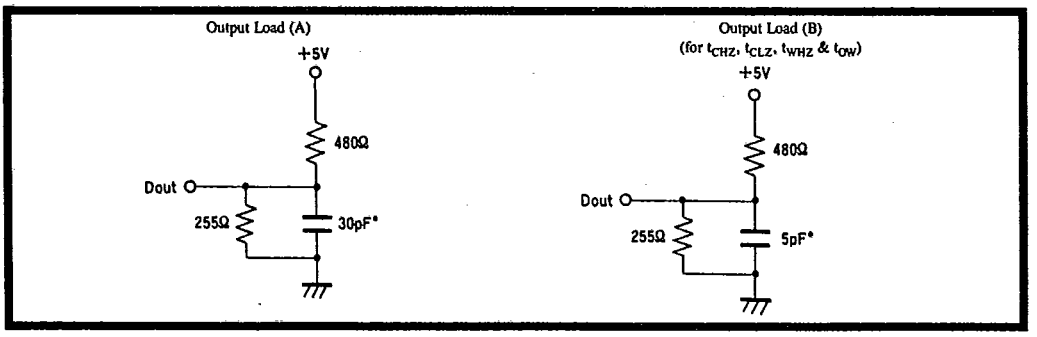
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures



NOTE: *Including scope & jig.

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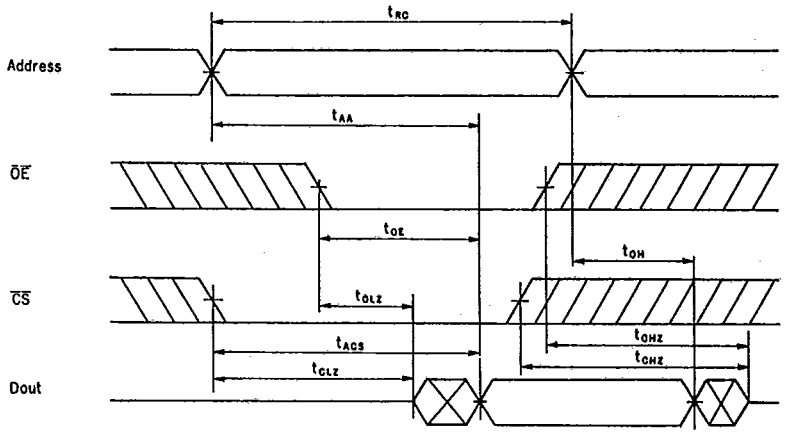
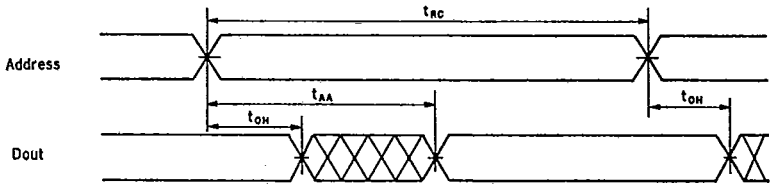
■ Read Cycle

Item	Symbol	HM624256-35		HM624256-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}*1	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	18	—	23	ns
Output Enable to Output in Low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}*1	0	20	0	20	ns
Chip Disable to Output in High-Z	t_{OHZ}*1	0	10	0	15	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

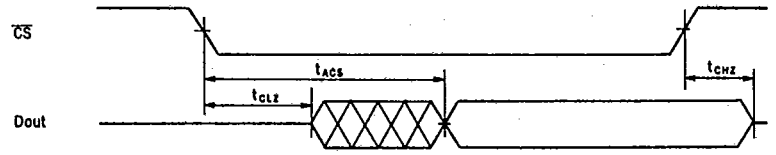
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5



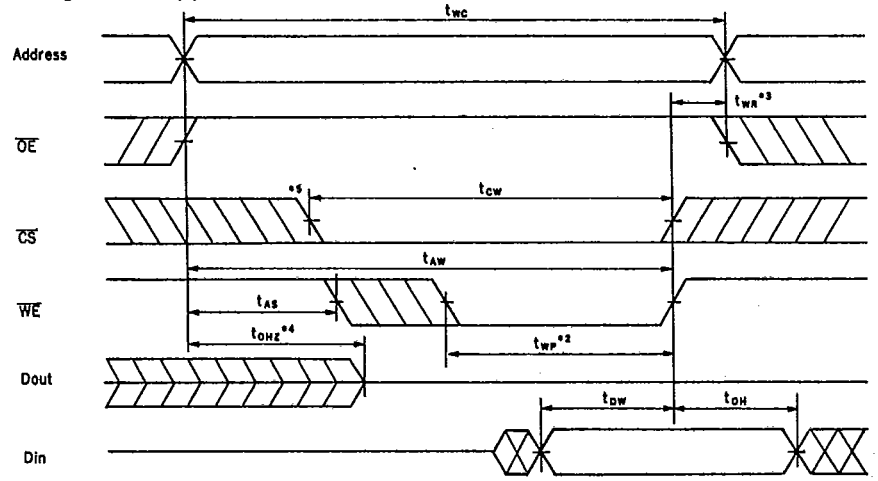
NOTES: *1. Transition is measured ±200 mv from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. $\overline{OE}$ = V_{IL}.

■ Write Cycle

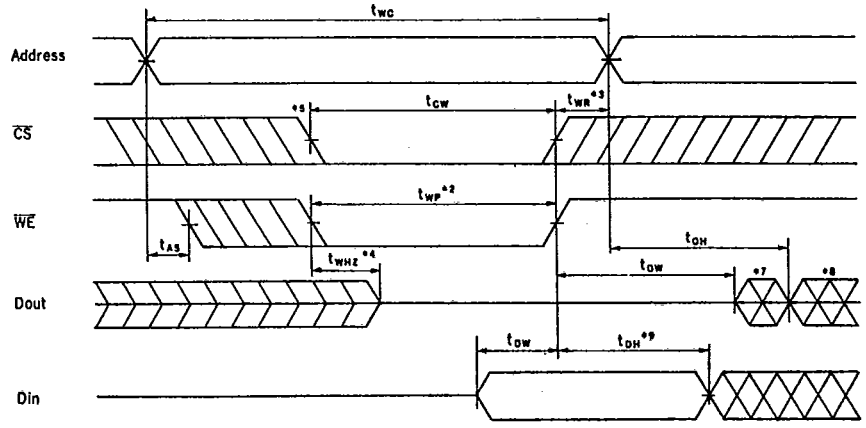
Item	Symbol	HM624256-35		HM624256-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Output Disable to Output in High-Z*1	t_{OHZ}	0	10	0	15	ns
Write to Output in High-Z*1	t_{WHZ}	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	20	—	25	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	ns
Output Active From End of Write*1	t_{OW}	0	—	0	—	ns

NOTE: 1. Transition is measured ± 200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1)



Write Timing Waveform (2) *6



NOTES:

*1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

*5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.

*6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})

*7. D_{OUT} is the same phase of write data of this write cycle.

*8. D_{OUT} is the read data of next address.

*9. If $\overline{CS}$ is low during this period, I/O pins are the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.