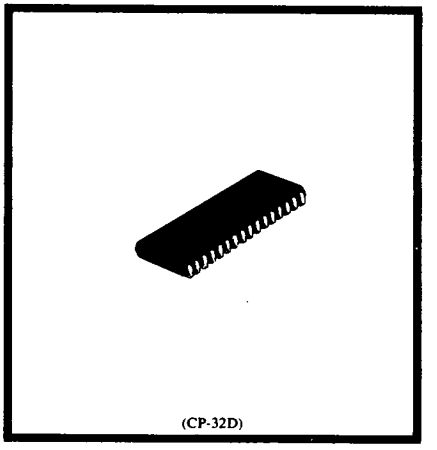
262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624257 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257, packaged in a 400-mil plastic SOJ is available for high density mounting.



■ FEATURES

- Single 5 V supply and high density 32-pin package (SOJ)
- High speed: Access time 35/45 ns (max.)
- Low power dissipation
  Active mode: 350 mW (typ.)
  Standby: 100 μW (typ.)
- Completely static memory:
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

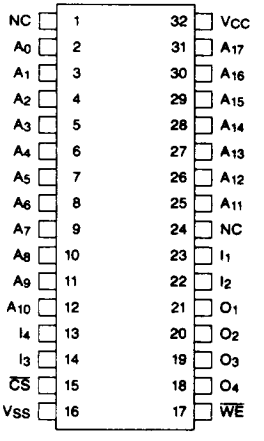
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624257JP-35	35 ns	400 mil 32-pin Plastic SOJ (CP-32D)
HM624257JP-45	45 ns	
HM624257LJP-35	35 ns	
HM624257LJP-45	45 ns	

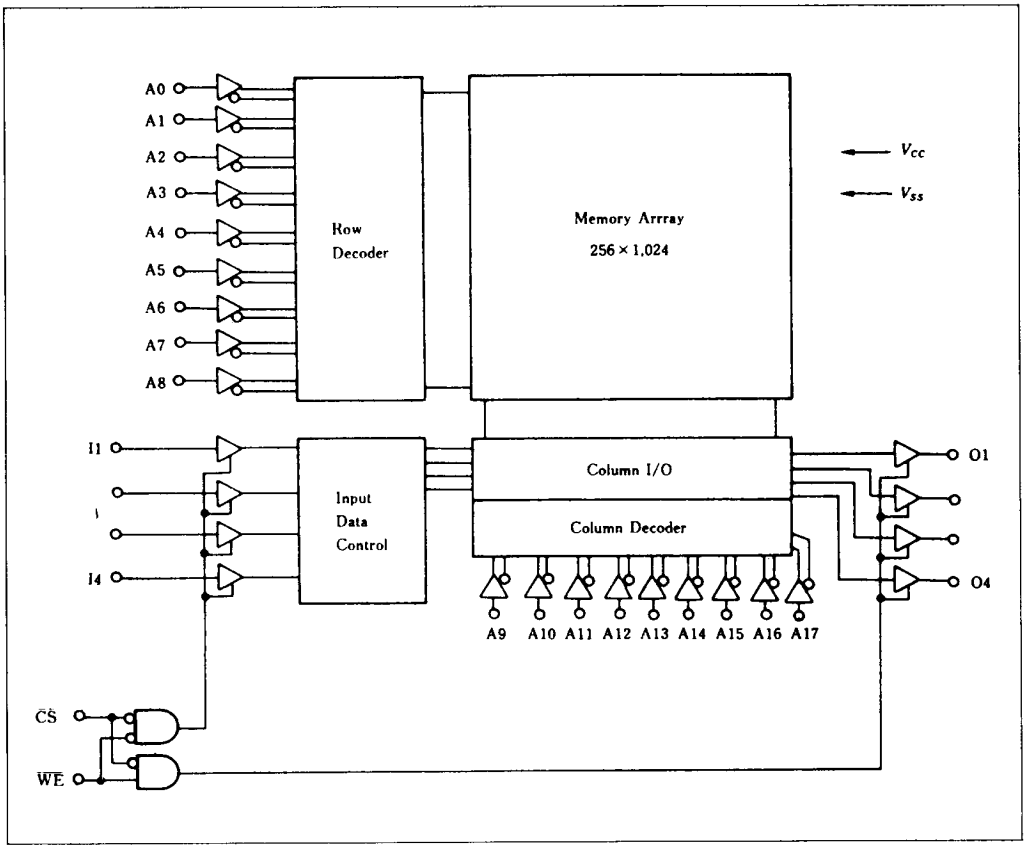
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{17}	Address
I_1–I_4	Data Input
I_1–O_4	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

PIN ARRANGEMENT
Top View



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{in}	-0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: *1. V_{in} min. = -2.0 V for pulse width ≤ 10 ns.

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle(1)-(2)
L	L	Write	I_{CC}	High-Z	Write Cycle(1)-(2)

NOTE: X : H or L

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■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = -2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

NOTE: 1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

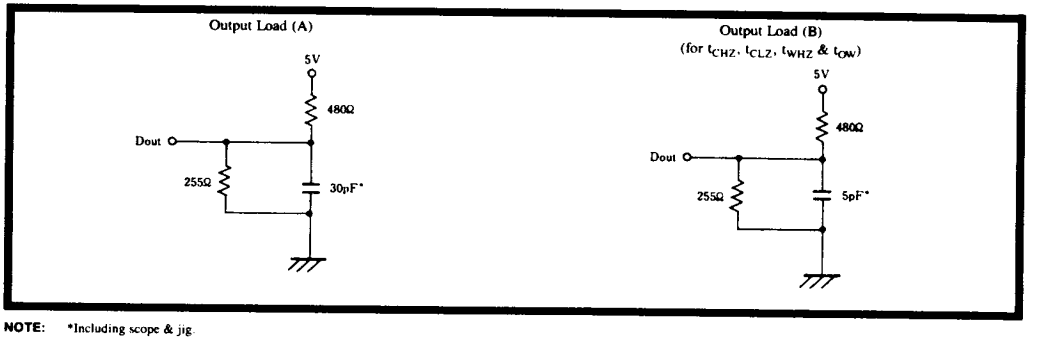
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Output Capacitance	C_{out}	—	11	pF	V_{out} = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures



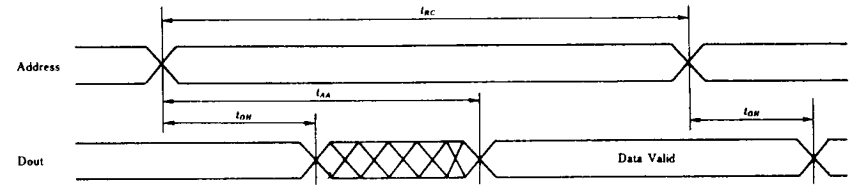
NOTE: *Including scope & jig.

■ Read Cycle

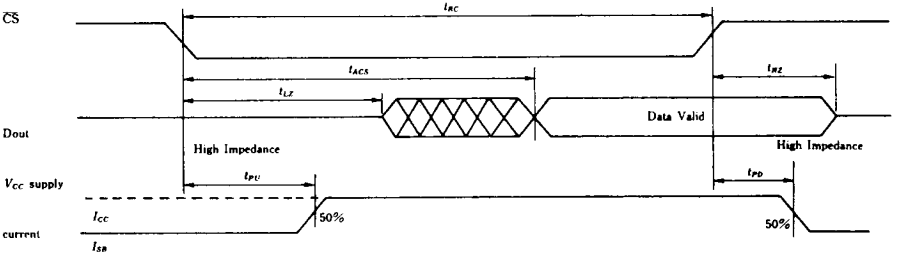
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—		—	30	ns

NOTE: 1. Transition is measured ±200 mV from steady voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



NOTES: *1. $\overline{WE}$ is high for read cycle.

*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

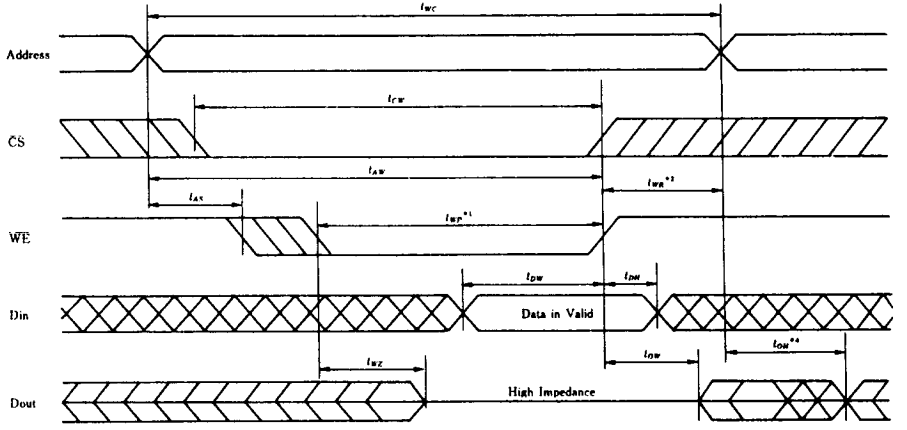
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ Write Cycle

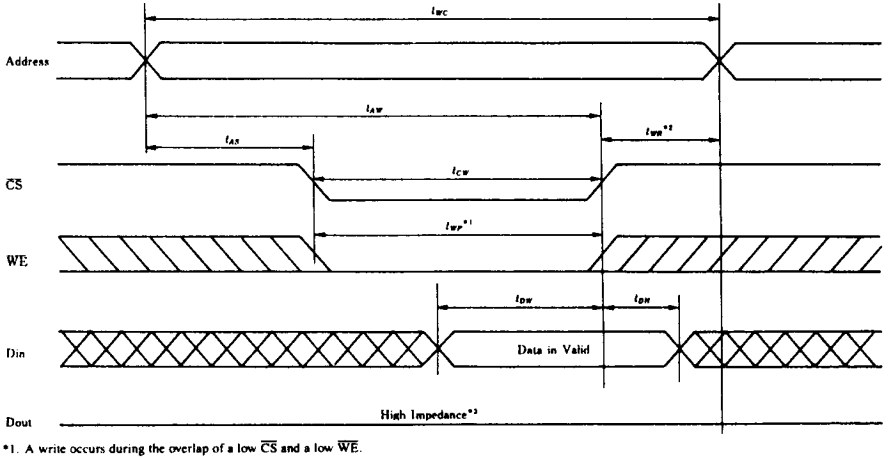
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	20	—		—	ns
Data Hold Time	t_{DH}	3	—	3	—	ns
Write Enabled to Output in High-Z	t_{WZ}*1	0	15	0	20	ns
Output Active From End of Write	t_{OW}*1	5	—	5	—	ns

NOTE: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



NOTES: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output buffers remain in a high impedance state.

*4. D_{OUT} is the same phase of write data of this write cycle.

■ Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or 0 V ≤ V_{in} ≤ 0.2 V
Data Retention Current	I_{CCDR}	—	2	100*1	µA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

NOTE: *1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform