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# HM628128BI Series

131,072-word  $\times$  8-bit High speed CMOS Static RAM

## HITACHI

ADE-203-363A(Z)

Rev. 1.0

Apr. 28, 1995

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The Hitachi HM628128BI is a CMOS static RAM organized 131,072-word  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8  $\mu$ m Hi-CMOS shrink process technology. It offers low power standby power dissipation, therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP or a 600-mil plastic DIP is available.

### Features

- High speed  
Fast access time: 85/100 ns (max)
- Low power  
standby: 10  $\mu$ W (typ)  
Operation: 50 mW/MHz (typ)
- Single 5 V supply
- Completely static memory  
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output  
Three state output
- Directly TTL compatible  
All inputs and outputs
- Capability of battery back up operation
- 2 chip selection for battery back up
- Operating temperature range
- $-40$  to  $+85^{\circ}\text{C}$

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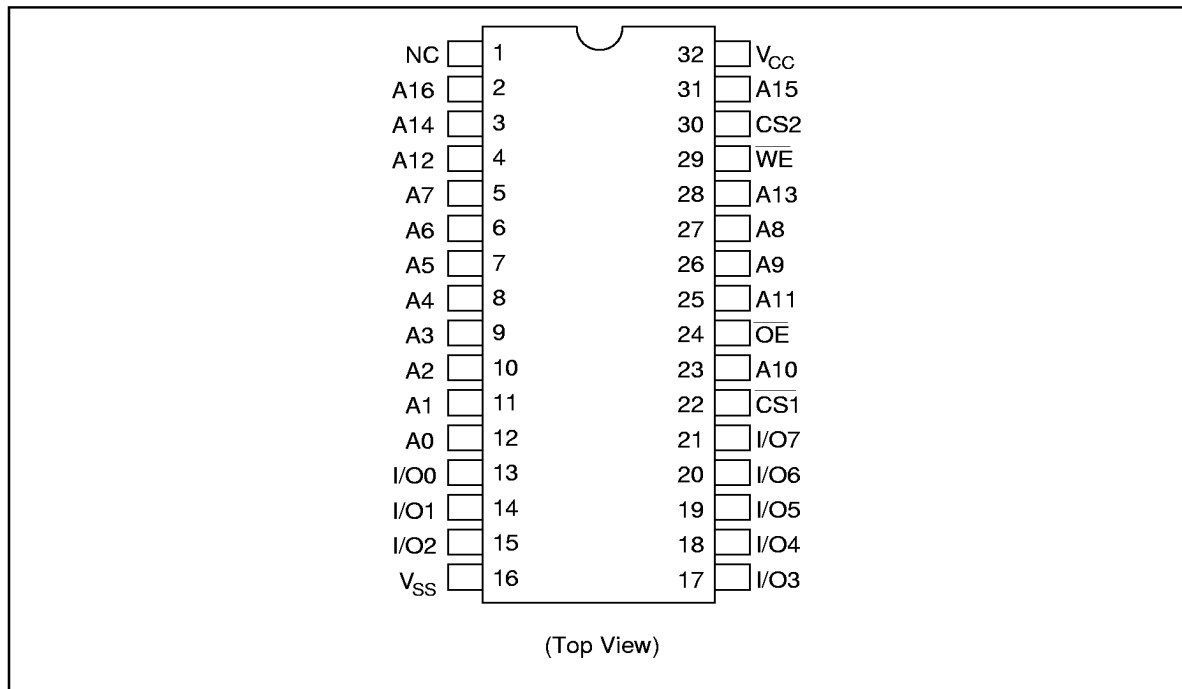
## HM628128BI Series

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### Ordering Information

Part No.	Access time	Data Retention Current	Package
HM628128BLPI-8	85 ns	50 $\mu$ A	600-mil
HM628128BLPI-10	100 ns	50 $\mu$ A	32-pin plastic DIP (DP-32)
HM628128BLFPI-8	85 ns	50 $\mu$ A	525-mil
HM628128BLFPI-10	100 ns	50 $\mu$ A	32-pin plastic SOP (FP-32D)

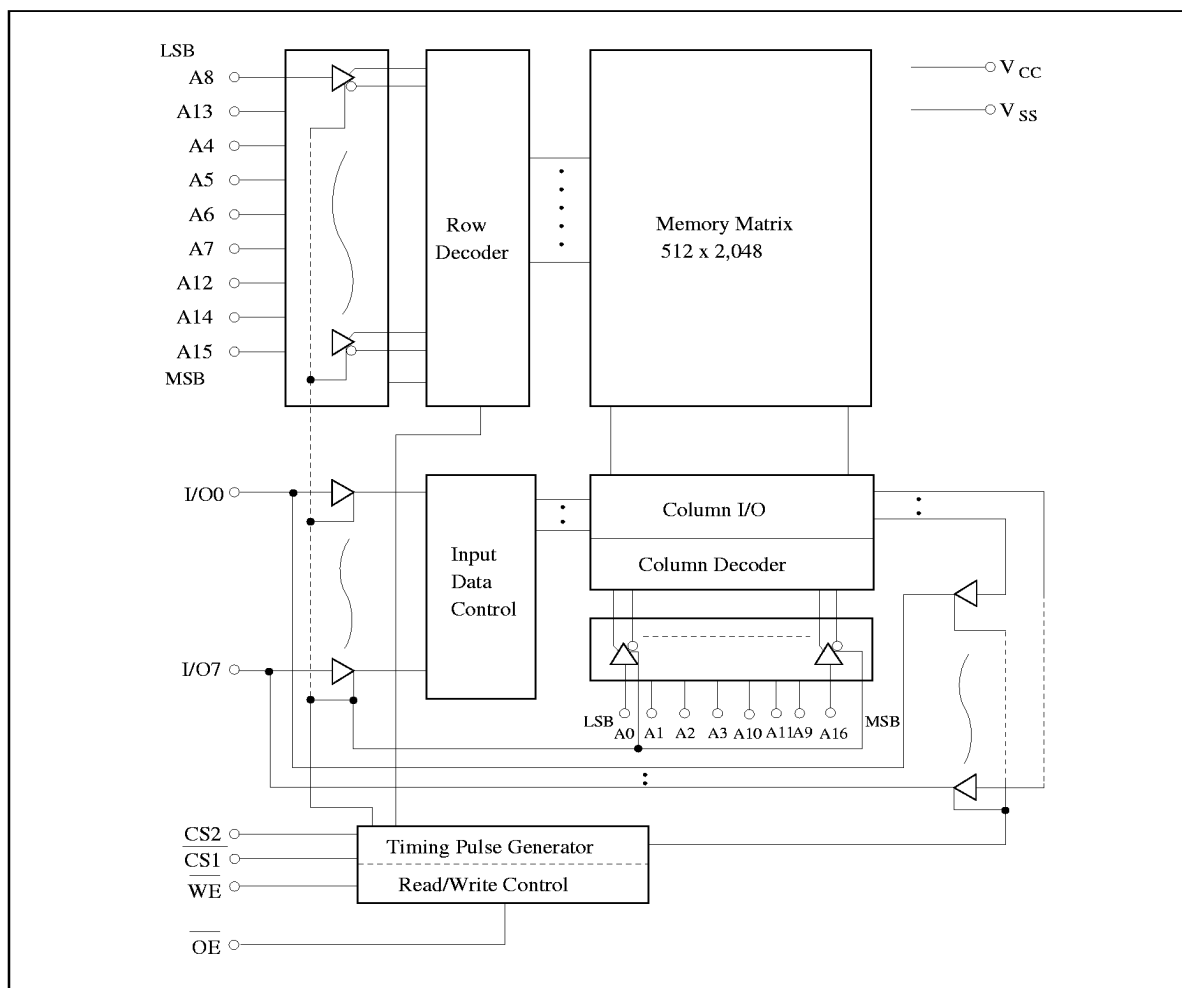
### Pin Arrangement



**Pin Description**

Pin name	Function
A0 to A16	Address
I/O0 to I/O7	Input/output
$\overline{\text{CS1}}$	Chip select 1
CS2	Chip select 2
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
NC	No connection
$V_{\text{cc}}$	Power supply
$V_{\text{ss}}$	Ground

### Block Diagram



**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>1</sup> to $V_{CC}+0.3$ <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +125	°C
Storage temperature under bias	Tbias	-40 to +85	°C

Notes: 1. -3.0 V for pulse half-width  $\leq$  30 ns  
2. Maximum voltage is 7.0 V.

**Function Table**

WE	CS1	CS2	OE	Mode	$V_{CC}$ current	I/O pin	Ref. cycle
X	H	X	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
X	X	L	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	H	Output disable	$I_{CC}$	High-Z	—
H	L	H	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	H	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: 1. X:H or L

**Recommended DC Operating Conditions ( $T_a = -40$  to  $+85^\circ\text{C}$ )**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage ( logic 1 )	$V_{IH}$	2.4	—	$V_{CC} + 0.3$	V
Input low voltage ( logic 0 )	$V_{IL}$	-0.3 <sup>1</sup>	—	0.6	V

Note9 1. -3.0 V for pulse half-width  $\leq$  30ns

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**DC Characteristics** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{cc} = 5\text{V} \pm 10\%$ ,  $V_{ss} = 0\text{V}$ )

Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{Li} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{ss}$ to $V_{cc}$
Output leakage current	$ I_{Lo} $	—	—	1	$\mu\text{A}$	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{IO} = V_{ss}$ to $V_{cc}$
Operating power supply current : DC	$I_{cc}$	—	15	30	mA	$\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0\text{mA}$
Operating power supply current	$I_{cc1}$	—	35	70	mA	Min.cycle, duty = 100 %, $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0\text{mA}$
	$I_{cc2}$	—	10	25	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100 % $I_{IO} = 0\text{mA}$ , $\overline{CS1} \leq 0.2\text{V}$ $CS2 \geq V_{cc} - 0.2\text{V}$ , Others = $V_{IH}/V_{IL}$ , $V_{IH} \geq V_{cc} - 0.2\text{V}$ , $V_{IL} \leq 0.2\text{V}$
Standby $V_{cc}$ current : DC	$I_{SB}$	—	1	2	mA	$CS2 = V_{IL}$ or $CS2 = V_{IH}$ , $\overline{CS1} = V_{IH}$
Standby $V_{cc}$ current (1): DC	$I_{SB1}$	—	2	100	$\mu\text{A}$	$0\text{V} \leq V_{in} \leq V_{cc}$ , (1) $0\text{V} \leq CS2 \leq 0.2\text{V}$ or (2) $CS2 \geq V_{cc} - 0.2\text{V}$ , $\overline{CS1} \geq V_{cc} - 0.2\text{V}$
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1\text{mA}$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0\text{mA}$

Notes: 1. Typical values are at  $V_{cc} = 5.0\text{V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	$C_{in}^{**}$	—	—	8	pF	$V_{in} = 0\text{V}$
Input/output capacitance	$C_{IO}^{**}$	—	—	10	pF	$V_{IO} = 0\text{V}$

Note: 1. This parameter is sampled and not 100 % tested.

**AC Characteristics** (Ta = -40 to +85°C, V<sub>cc</sub> = 5 V ±10%, unless otherwise noted.)

**Test Conditions**

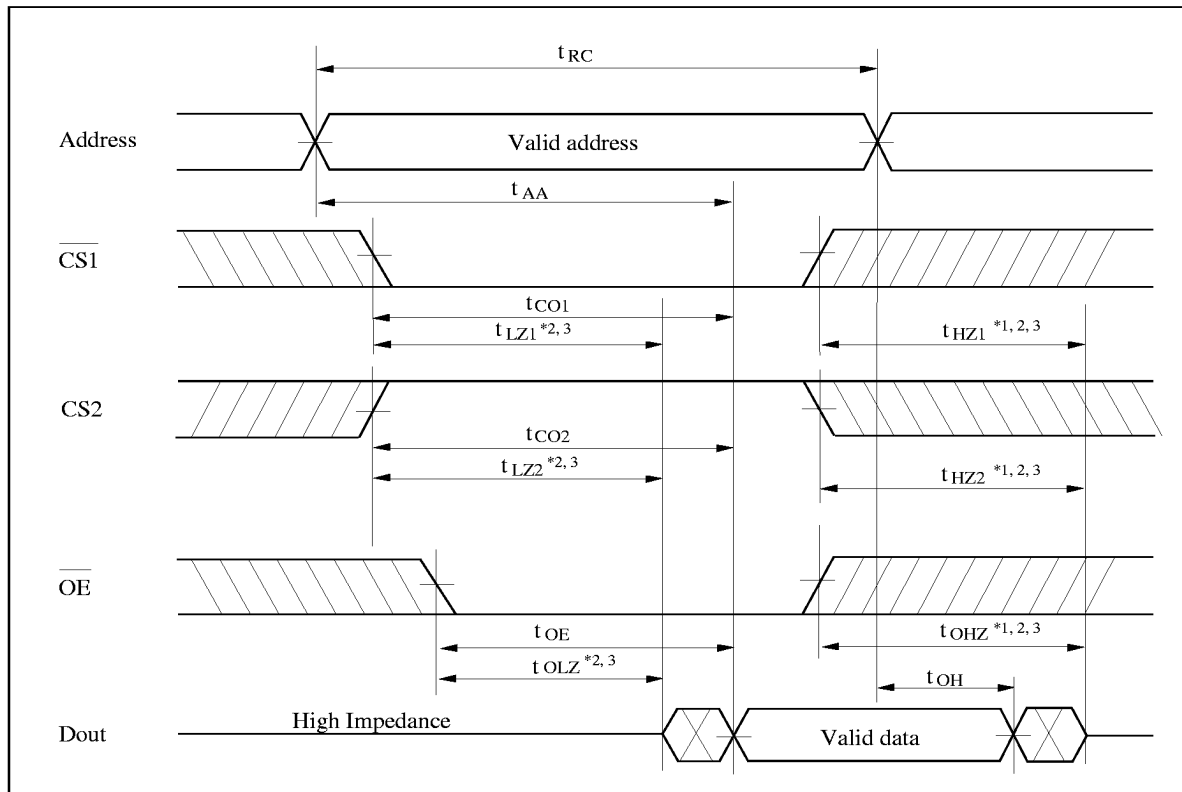
- Input pulse levels : 0.5 V to 2.5 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels : 1.5 V
- Output load : 1 TTL Gate and C<sub>L</sub> (100pF) (Including scope and jig)

**Read Cycle**

		HM628128BI					
		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	85	—	100	—	ns	
Address access time	t <sub>AA</sub>	—	85	—	100	ns	
Chip selection to output valid	t <sub>CO1</sub>	—	85	—	100	ns	
	t <sub>CO2</sub>	—	85	—	100	ns	
Output enable to output valid	t <sub>OE</sub>	—	45	—	50	ns	
Chip selection to output in low-Z	t <sub>LZ1</sub>	10	—	10	—	ns	2, 3
	t <sub>LZ2</sub>	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t <sub>HZ1</sub>	0	30	0	35	ns	1, 2, 3
	t <sub>HZ2</sub>	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	30	0	35	ns	1, 2, 3
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	

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### Read Cycle Timing<sup>\*4</sup>



- Notes:
1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  3. This parameter is sampled and not 100 % tested.
  4.  $\overline{WE}$  is high for read cycle.

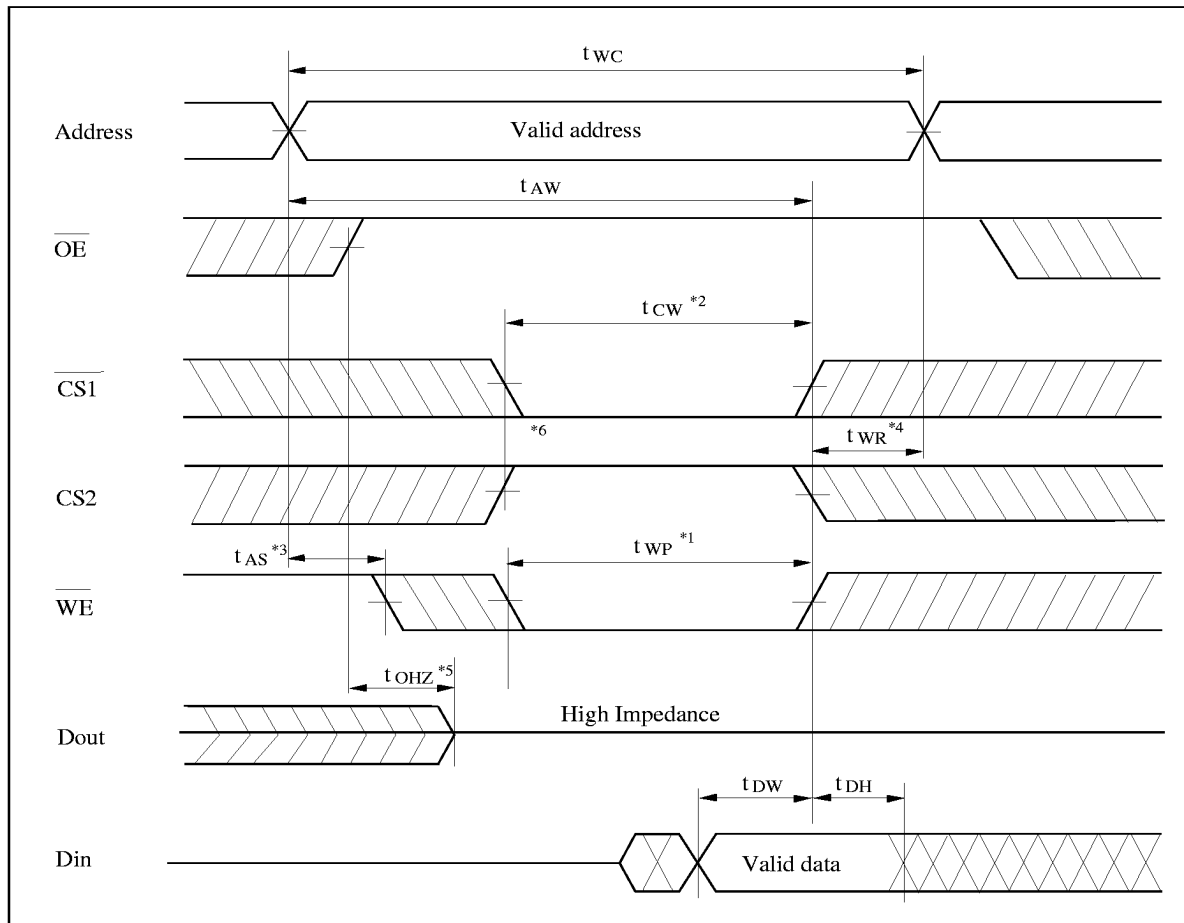


**Write Cycle**

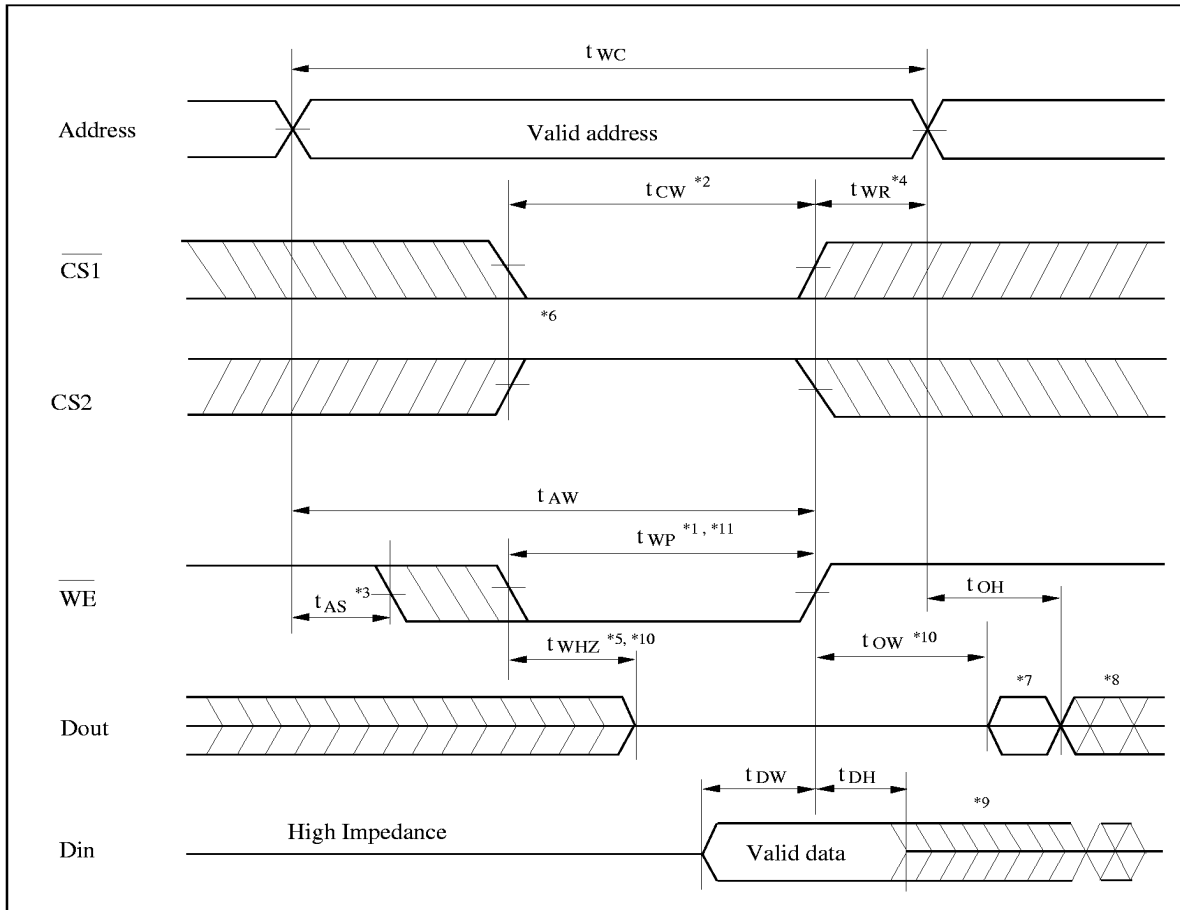
		HM628128BI					
		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	85	—	100	—	ns	
Chip selection to end of write	t <sub>CW</sub>	75	—	80	—	ns	
Address setup time	t <sub>AS</sub>	0	—	0	—	ns	
Address valid to end of write	t <sub>AW</sub>	75	—	80	—	ns	
Write pulse width	t <sub>WP</sub>	55	—	60	—	ns	11
Write recovery time	t <sub>WR</sub>	0	—	0	—	ns	
Write to output in high-Z	t <sub>WHZ</sub>	0	30	0	35	ns	10
Data to write time overlap	t <sub>DW</sub>	35	—	40	—	ns	
Write hold from write time	t <sub>DH</sub>	0	—	0	—	ns	
Output active from end of write	t <sub>OW</sub>	5	—	5	—	ns	10

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### Write Cycle Timing (1) ( $\overline{\text{OE}}$ Clock)



Write Cycle Timing (2) ( $\overline{\text{OE}}$  low fix)



- Notes:
1. A write occurs during the overlap of a low  $\overline{\text{CS1}}$ , a high CS2, and a low  $\overline{\text{WE}}$ . A write begins at the latest transition among  $\overline{\text{CS1}}$  going low, CS2 going high, and  $\overline{\text{WE}}$  going low. A write ends at the earliest transition among  $\overline{\text{CS1}}$  going high, CS2 going low, and  $\overline{\text{WE}}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  2.  $t_{CW}$  is measured from the later of  $\overline{\text{CS1}}$  going low or CS2 going high to the end of write.
  3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  4.  $t_{WR}$  is measured from the earliest of  $\overline{\text{CS1}}$  or  $\overline{\text{WE}}$  going high or CS2 going low to the end of write cycle.
  5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  6. If the  $\overline{\text{CS1}}$  goes low simultaneously with  $\overline{\text{WE}}$  going low or after the  $\overline{\text{WE}}$  going low, the outputs remain in a high impedance state.
  7. Dout is the same phase of the latest written data in this write cycle.
  8. Dout is the read date of next address.

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9. If  $\overline{CS1}$  is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

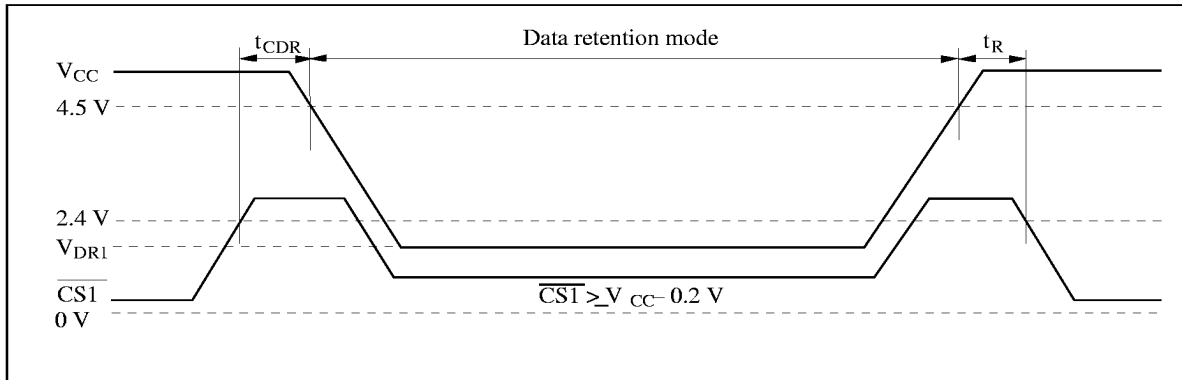
10. This parameter is sampled and not 100 % tested.

11. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention,  $t_{WP} \geq t_{DW} (\text{min}) + t_{WHZ} (\text{max})$ .

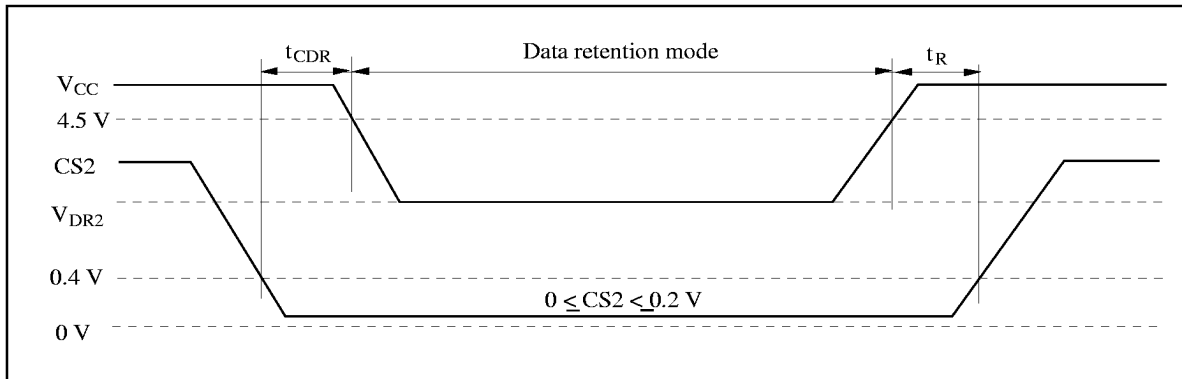
### Low $V_{CC}$ Data Retention Characteristics ( $T_a = -40$ to $+85^\circ\text{C}$ )

Parameter	Symbol	Min	Typ <sup>2</sup>	Max	Unit	Test conditions <sup>3</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$0\text{ V} \leq V_{in} \leq V_{CC}$ , (1) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{ V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$
Data retention current	$I_{CCDR}$	—	1	$50^{-1}$	$\mu\text{A}$	$V_{CC} = 3\text{ V}$ , $0\text{ V} \leq V_{in} \leq 3\text{ V}$ (1) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{ V}$ , $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$5^{-4}$	—	—	ms	

Low  $V_{CC}$  Data Retention Waveform (1) ( $\overline{CS1}$  Controlled)\*3



Low  $V_{CC}$  Data Retention Waveform (2) ( $CS2$  Controlled)\*3

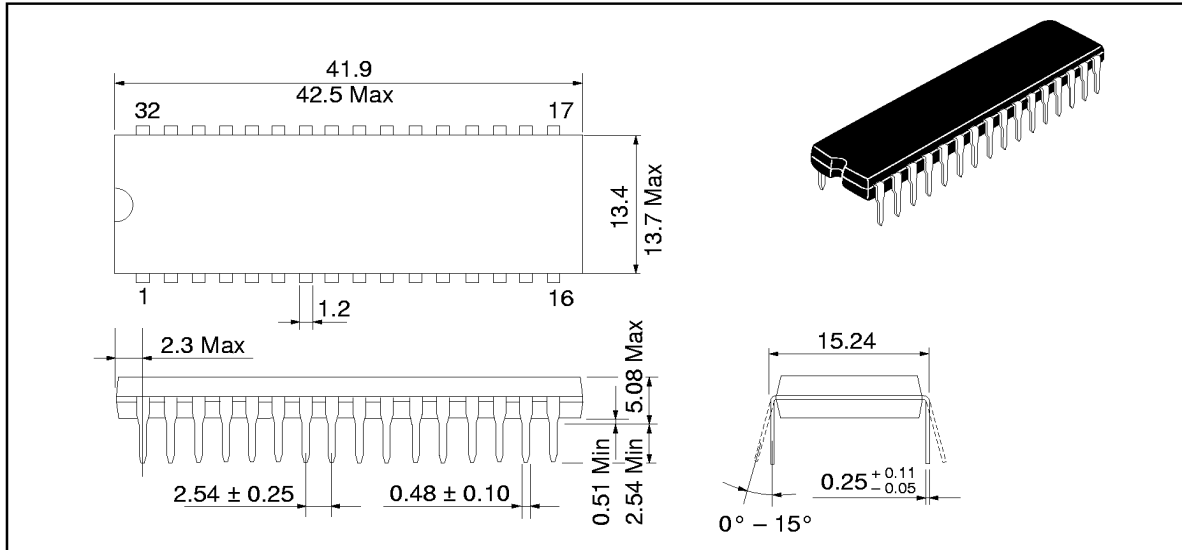


- Notes:
1. This characteristics is guaranteed 20  $\mu\text{A}$  max. at  $T_a = -40$  to  $+40^\circ\text{C}$ .
  2. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.
  3.  $CS2$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer, and Din buffer. If  $CS2$  controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode,  $CS2$  must be  $CS2 \geq V_{CC} - 0.2 \text{ V}$  or  $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
  4.  $V_{CC}$  rising time must be more than 50 ms. When  $V_{CC}$  rising time is less than 50 ms,  $t_R$  must be 50 ms or more.

## HM628128BI Series

### Package Dimensions

#### DP-32



#### FP-32D

