
HM62864 Series

512 k SRAM (64-kword $\times$ 8-bit)

HITACHI

ADE-203-255C (Z)

Rev. 3.0

Nov. 1997

Description

The Hitachi HM62864 is a CMOS static RAM organized 64-kword $\times$ 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μ m Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) and a 8 $\times$ 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards.

Features

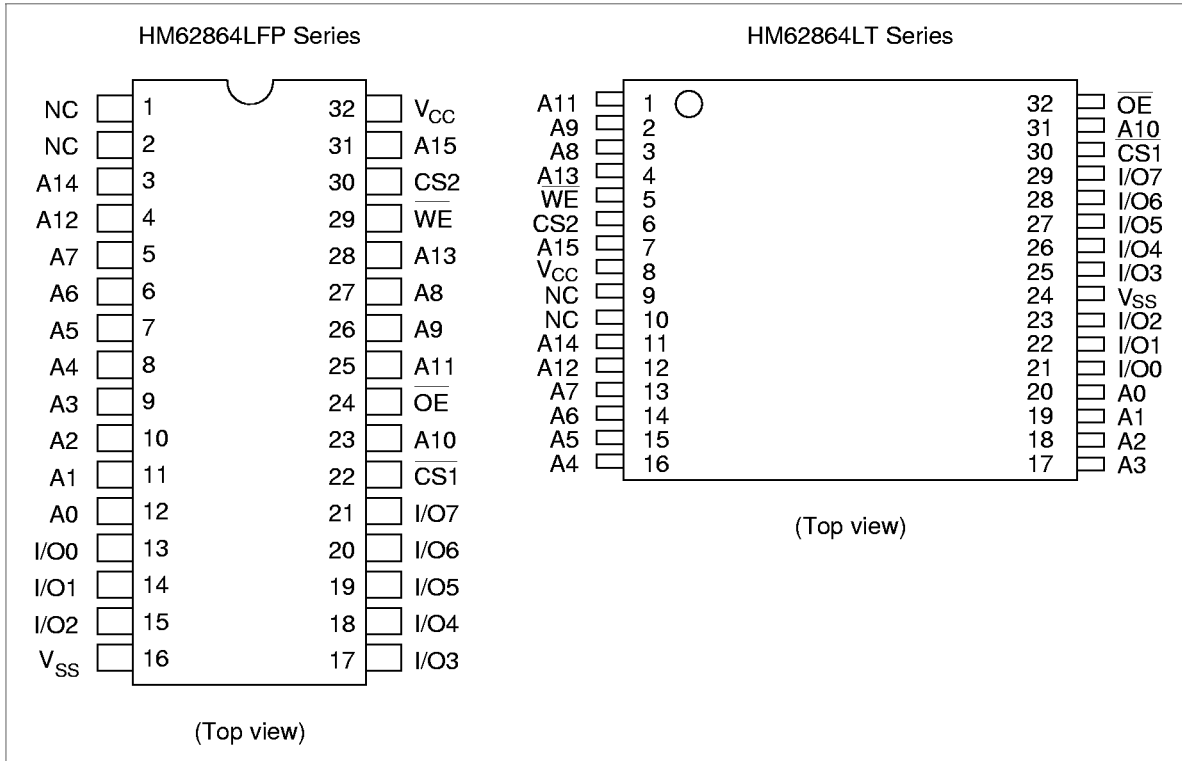
- High speed
 - Fast access time: 55/70/85 ns (max)
- Low power
 - Active: 50 mW (typ) (f = 1 MHz)
 - Standby: 2 μ W (typ)
- Single 5 V supply
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Capability of battery backup operation
 - 2 chip selection for battery backup

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Ordering Information

Type No.	Access Time	Package
HM62864LFP-7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62864LFP-8	85 ns	
HM62864LFP-5SL	55 ns	
HM62864LFP-7SL	70 ns	
HM62864LFP-8SL	85 ns	
HM62864LT-7	70 ns	8 mm × 20 mm 32-pin TSOP (normal type) (TFP-32D)
HM62864LT-8	85 ns	
HM62864LT-5SL	55 ns	
HM62864LT-7SL	70 ns	
HM62864LT-8SL	85 ns	

Pin Arrangement

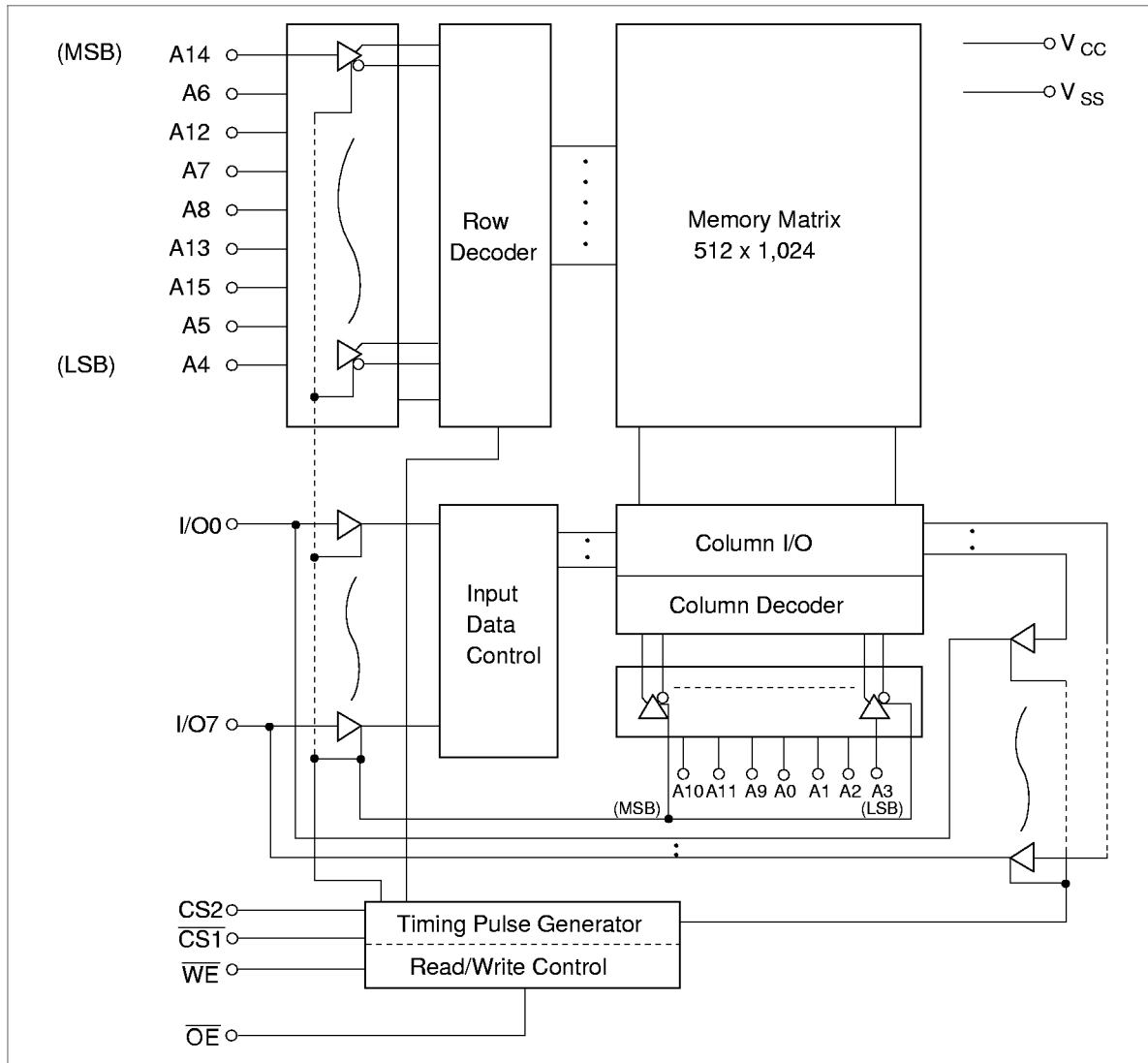


Pin Description

Pin Name	Function
A0 to A15	Address
I/O0 to I/O7	Input/output
$\overline{\text{CS1}}$	Chip select 1
CS2	Chip select 2
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
NC	No connection
V_{cc}	Power supply
V_{ss}	Ground

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Block Diagram



Function Table

$\overline{\text{CS1}}$	CS2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	X	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
X	L	X	X	Not selected	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	H	H	Output disable	I_{CC}	High-Z	—
L	H	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	H	L	Write	I_{CC}	Din	Write cycle (1)
L	H	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: High or Low

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage ^{*1}	V_{CC}	−0.5 to +7.0	V
Terminal voltage ^{*1}	V_{T}	−0.5 ^{*2} to $V_{\text{CC}} + 0.3$ ^{*3}	V
Power dissipation	P_{T}	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C
Storage temperature under bias	T_{bias}	−10 to +85	°C

Notes: 1. Relative to V_{SS}

2. V_{T} min: −3.0 V for pulse half-width ≤ 50 ns

3. Maximum voltage is 7.0V

Recommended DC Operating Conditions ($T_{\text{a}} = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	$V_{\text{CC}} + 0.3$	V
Input low (logic 0) voltage	V_{IL}	−0.3 ^{*1}	—	0.8	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 50 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{SS} ≤ Vin ≤ V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS1} = V_{IH}$ or CS2 = V _{IL} or $\overline{OE} = V_{IH}$ or WE = V _{IL} , V _{SS} ≤ V _{I/O} ≤ V _{CC}
Operating power supply current	I _{CC}	—	10	15	mA	$\overline{CS1} = V_{IL}$, CS2 = V _{IH} , Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Average operating power supply current	HM62864-5 I _{CC1}	—	55	70	mA	Min cycle, duty = 100%, CS1 = V _{IL} , CS2 = V _{IH} ,
	HM62864-7 I _{CC1}	—	55	70		Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
	HM62864-8 I _{CC1}	—	45	60		
	I _{CC2}	—	10	15	mA	Cycle time = 1 μs, duty = 100%, I _{I/O} = 0 mA, $\overline{CS1} \leq V_{IL}$, CS2 ≥ V _{IH} , Others = V _{IH} /V _{IL} , V _{IH} ≥ V _{CC} - 0.2 V, 0 V ≤ V _{IL} ≤ 0.2 V
Standby power supply current	I _{SB}	—	0.7	3	mA	(1) or (2) (1) CS1 = V _{IH} , CS2 = V _{IH} (2) CS2 = V _{IL}
	I _{SB1}	—	0.4	100	μA	0 V ≤ Vin ≤ V _{CC} (1) or (2) (1) $\overline{CS1} \geq V_{CC} - 0.2$ V,
	I _{SB1}	—	0.4	50 ²		CS2 ≥ V _{CC} - 0.2V (2) 0 V ≤ CS2 ≤ 0.2 V
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

2. This characteristics is guaranteed only for SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)^{*1}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C _{in}	—	—	5	pF	Vin = 0 V
Input/output capacitance	C _{I/O}	—	—	8	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: HM62864-5: 1 TTL + 30 pF (Including scope & jig)
HM62864-7/8: 1 TTL + 100 pF (Including scope & jig)

Read Cycle

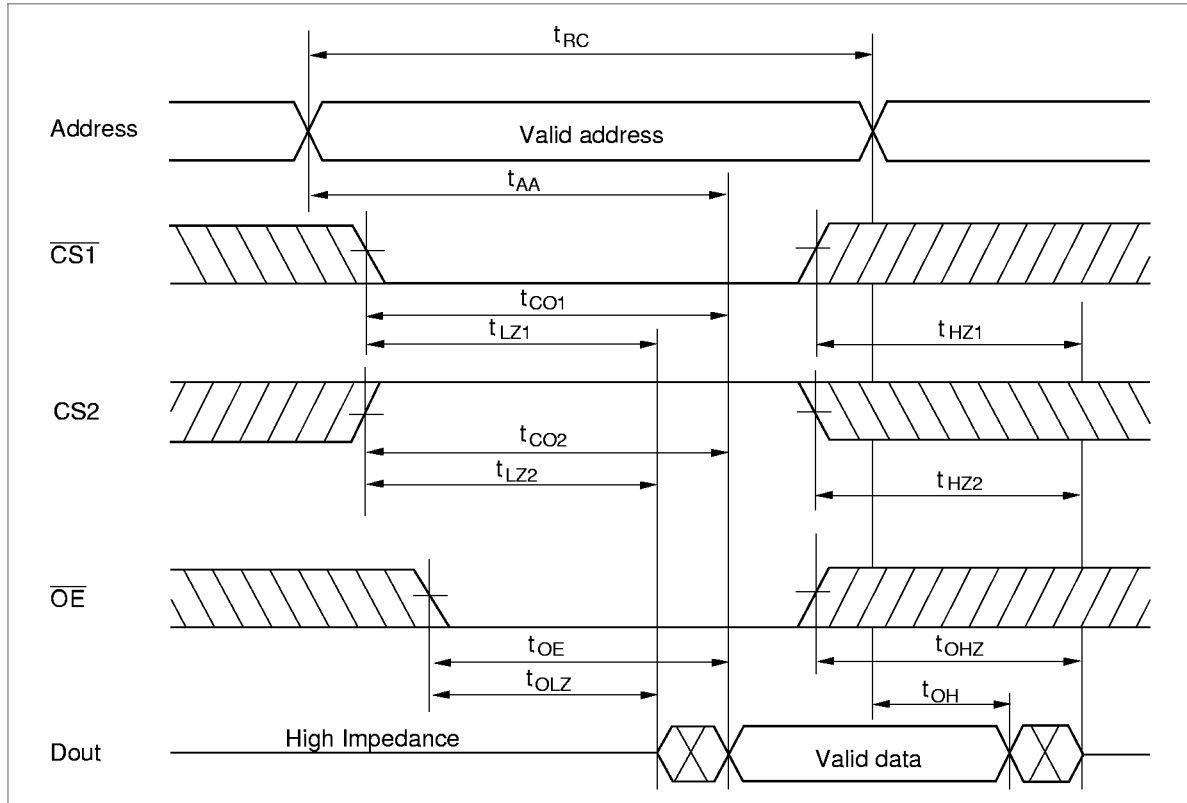
Parameter	Symbol	HM62864-5		HM62864-7		HM62864-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	55	—	70	—	85	—	ns	
Address access time	t _{AA}	—	55	—	70	—	85	ns	
Chip select access time	$\overline{\text{CS1}}$ t _{CO1}	—	55	—	70	—	85	ns	
	CS2 t _{CO2}	—	55	—	70	—	85	ns	
Output enable to output valid	t _{OE}	—	30	—	40	—	45	ns	
Chip selection to output in	$\overline{\text{CS1}}$ t _{LZ1}	5	—	10	—	10	—	ns	2
low-Z	CS2 t _{LZ2}	5	—	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection in output in	$\overline{\text{CS1}}$ t _{HZ1}	0	20	0	25	0	30	ns	1, 2
high-Z	CS2 t _{HZ2}	0	20	0	25	0	30	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	0	30	ns	1, 2
Output hold from address change	t _{OH}	5	—	10	—	10	—	ns	

Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

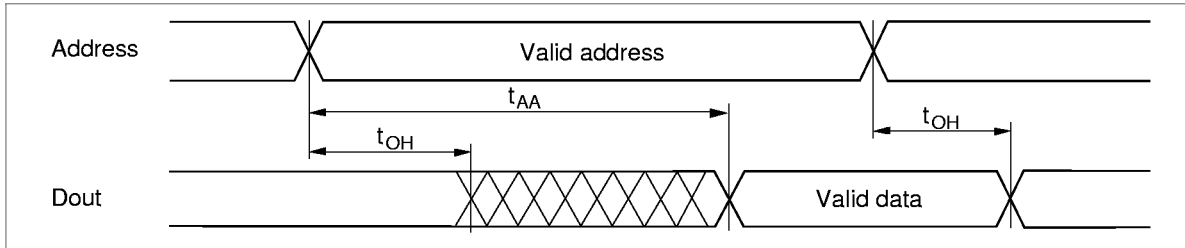
2. This parameter is sampled and not 100% tested.

HM62864 Series

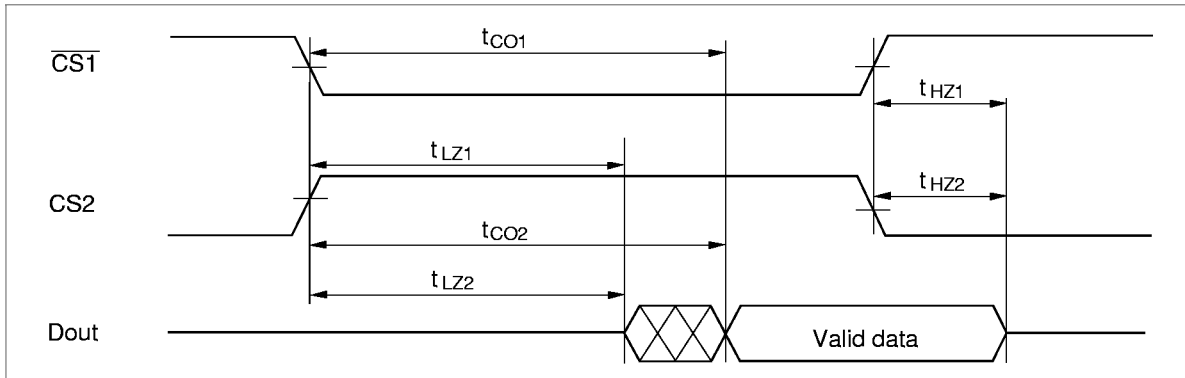
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



Read Timing Waveform (2) ($\overline{WE} = V_{IH}$)



Read Timing Waveform (3) ($\overline{WE} = V_{IH}$)



HM62864 Series

Write Cycle

Parameter	Symbol	HM62864-5		HM62864-7		HM62864-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	55	—	70	—	85	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	75	—	ns	4
Address setup time	t_{AS}	0	—	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	50	—	60	—	75	—	ns	
Write pulse width	t_{WP}	40	—	50	—	55	—	ns	3, 8
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	6
Write to output in high-Z	t_{WHZ}	0	20	0	25	0	30	ns	1, 2, 7
Data to write time overlap	t_{DW}	30	—	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	ns	1, 2, 7

Notes: 1. t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

4. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

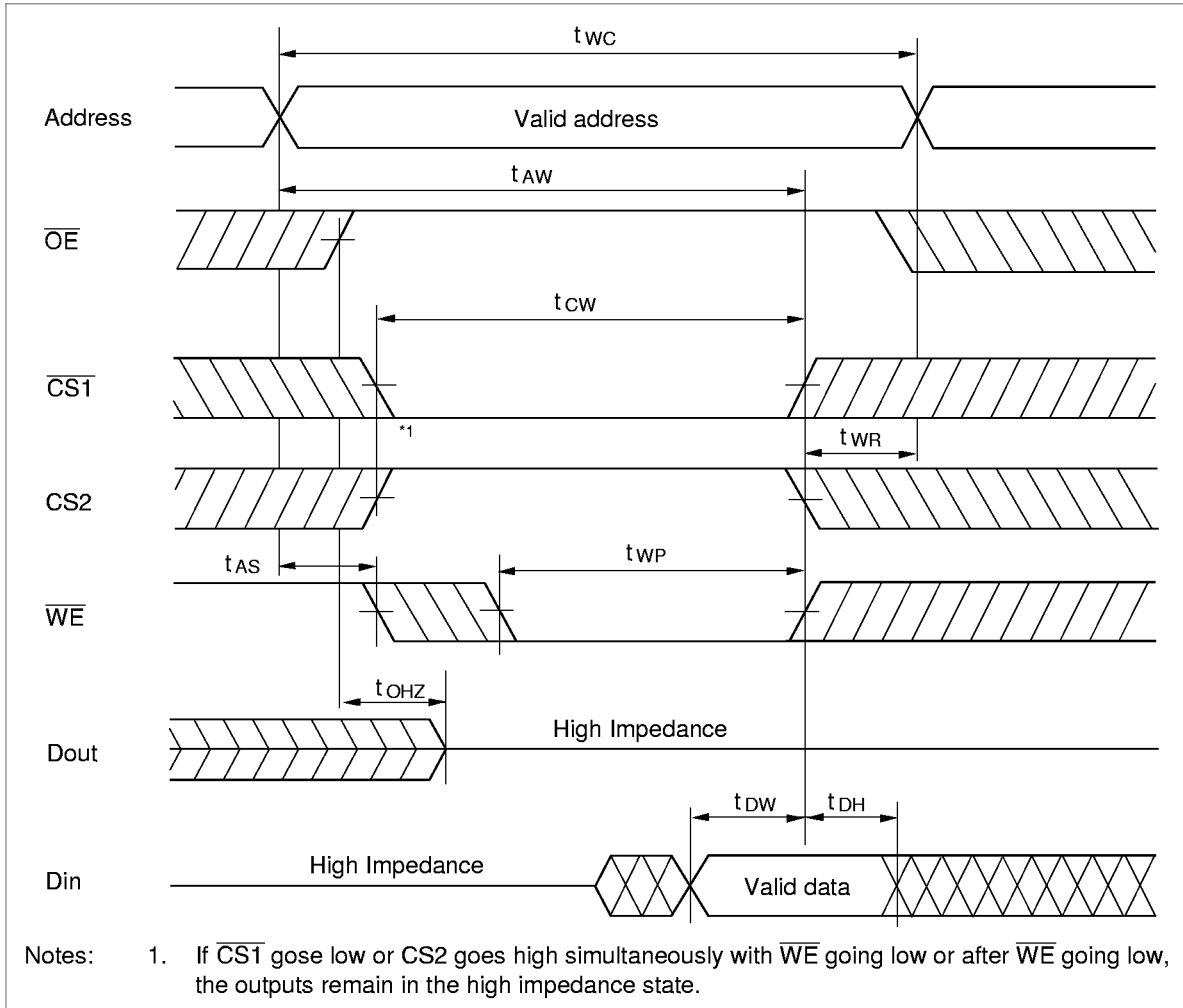
5. t_{AS} is measured from the address valid to the beginning of write.

6. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

7. During this period, I/O pin are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

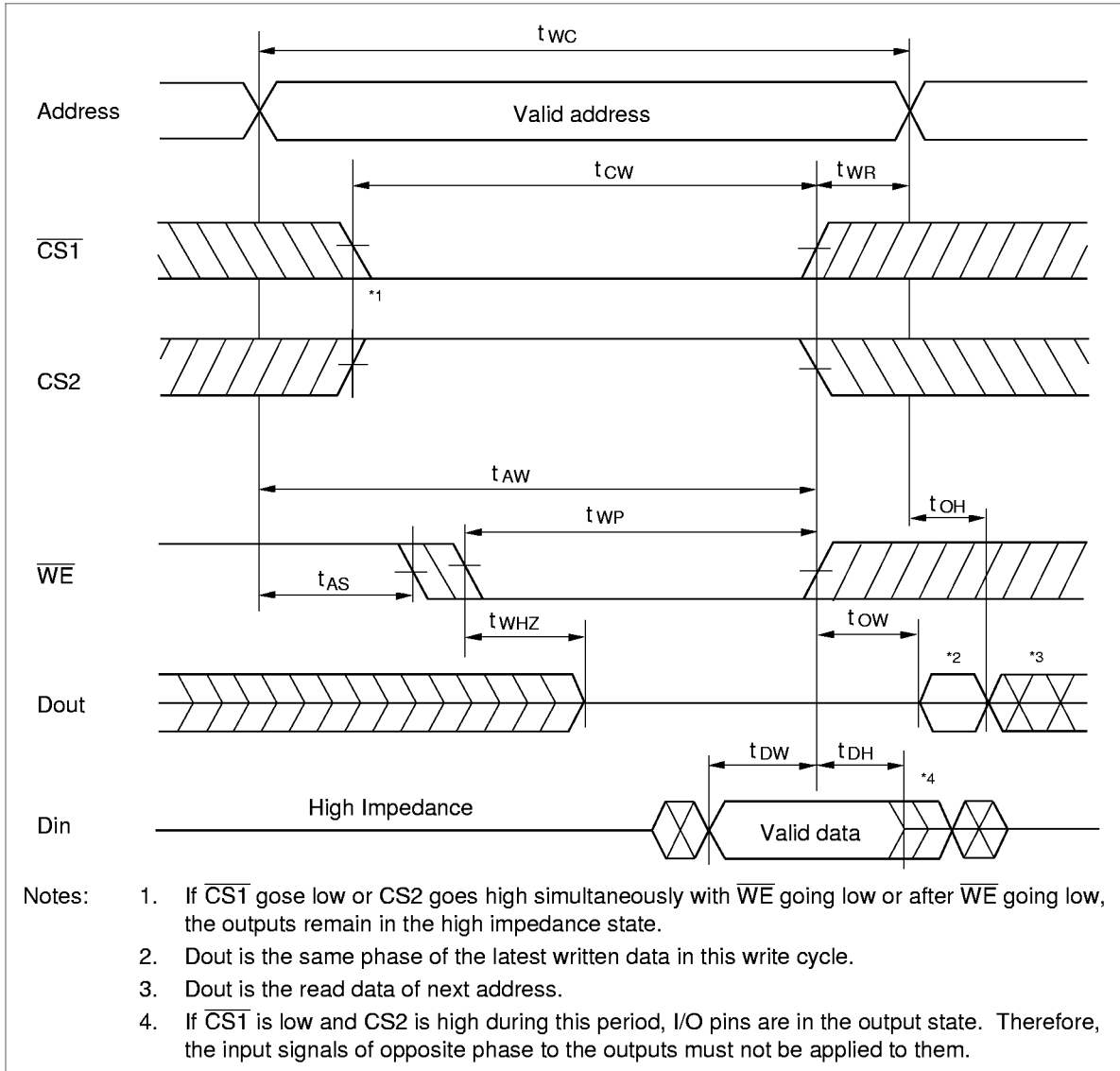
8. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, $t_{WP} \geq t_{WHZ} \text{ max} + t_{DW} \text{ min}$.

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



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Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)



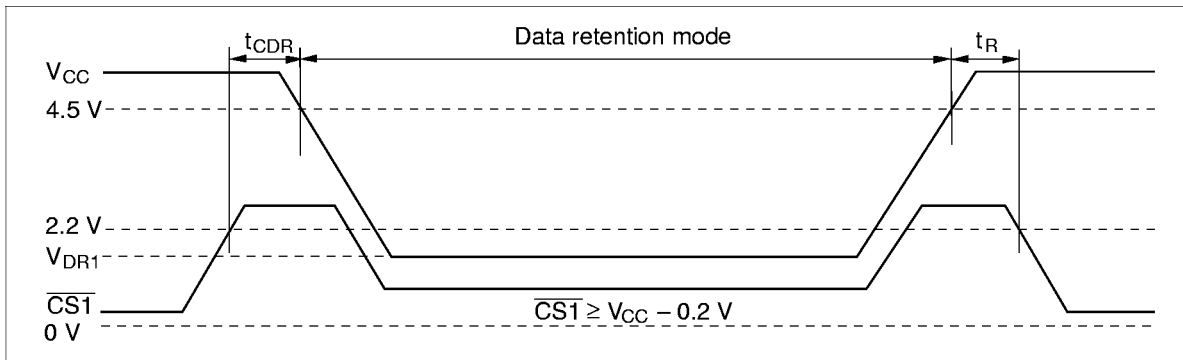
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test conditions ⁵
V_{CC} for data retention	V_{DR}	2.0	—	5.5	V	$0\text{ V} \leq V_{in} \leq V_{CC}$, (1) or (2) (1) $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ (2) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$
Data retention current	I_{CCDR}	—	0.1	30^{*2}	μA	$V_{CC} = 3.0\text{ V}$, $0\text{ V} \leq V_{in} \leq V_{CC}$, (1) or (2) (1) $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ (2) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$
	I_{CCDR}	—	0.1	10^{*3}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*4}	—	—	ns	

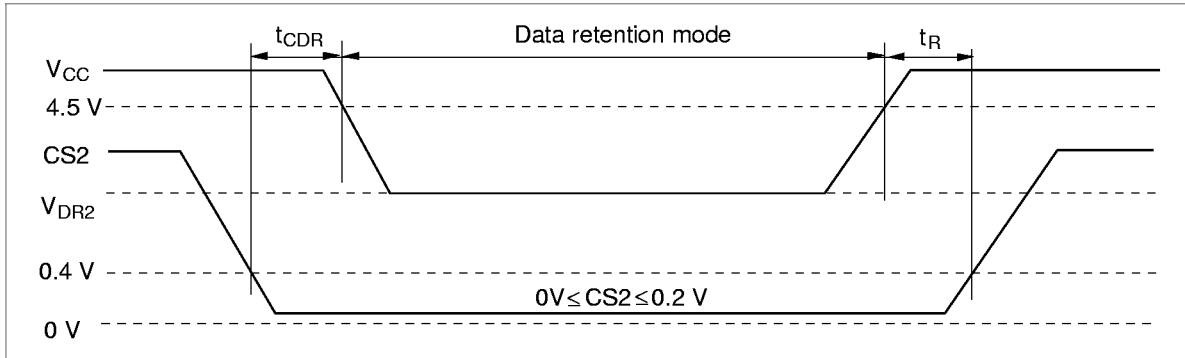
- Notes: 1. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = 25^\circ\text{C}$ and not guaranteed.
2. $10\text{ }\mu\text{A}$ max at $T_a = 0$ to 40°C .
3. This characteristics guaranteed for only L-SL version. $3\text{ }\mu\text{A}$ max at $T_a = 0$ to 40°C .
4. t_{RC} = Read cycle time.
5. $\overline{CS2}$ controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $\overline{CS2}$ controls data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, $CS2$ must be $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq 0.2\text{ V}$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



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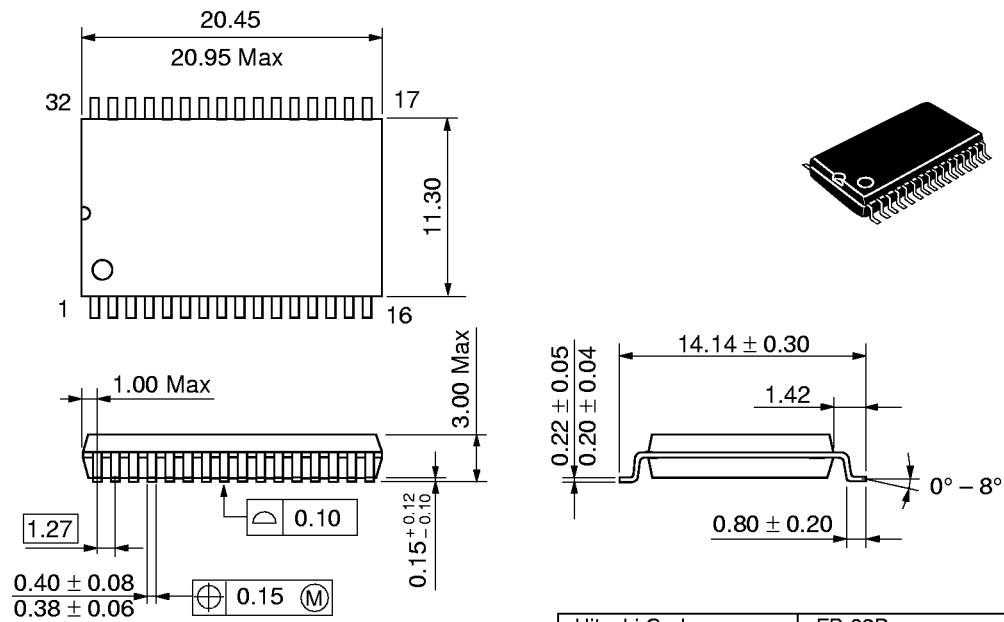
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM62864LFP Series (FP-32D)

Unit: mm

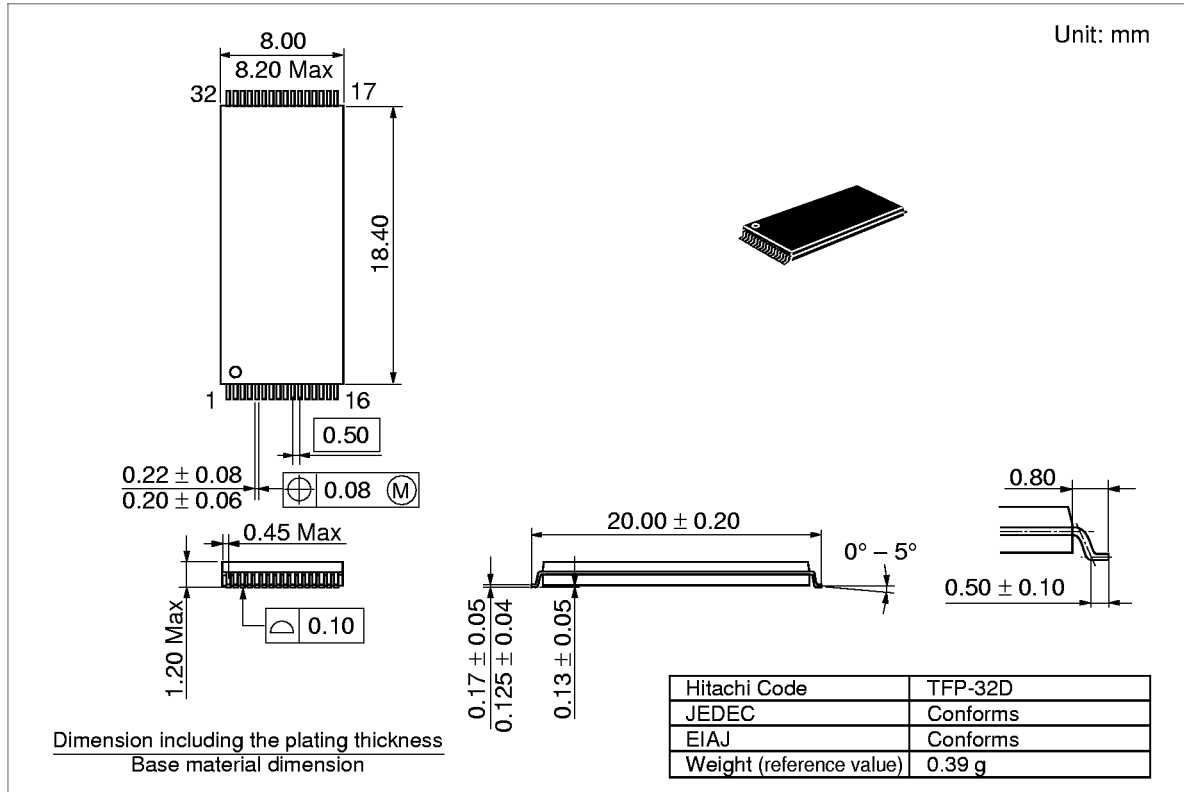


Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

HM62864 Series

HM62864LT Series (TFP-32D)



HM62864 Series

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	May. 12, 1994	Initial issue	M.Higuchi	K.Yoshizaki
1.0	Nov. 15, 1995	Deletion of HM62864L-L Series Addition of HM62864L-5SL Series DC Characteristics I_{CC} (typ): 55/45 mA to 55/45/45 mA I_{CC} (max): 70/60 mA to 70/70/60 mA AC Characteristics t_{RC} (min): 70/85 ns to 55/70/85 ns t_{AA} (max): 70/85 ns to 55/70/85 ns t_{CO1} (max): 70/85 ns to 55/70/85 ns t_{CO2} (max): 70/85 ns to 55/70/85 ns t_{OE} (max): 40/45 ns to 30/40/45 ns t_{LZ1} (min): 10/10 ns to 5/10/10 ns t_{LZ2} (min): 10/10 ns to 5/10/10 ns t_{OLZ} (min): 5/5 ns to 5/5/5 ns t_{HZ1} (min): 0/0 ns to 0/0/0 ns t_{HZ1} (max): 25/30 ns to 20/25/30 ns t_{HZ2} (min): 0/0 ns to 0/0/0 ns t_{HZ2} (max): 25/30 ns to 20/25/30 ns t_{OHZ} (min): 0/0 ns to 0/0/0 ns t_{OHZ} (max): 25/30 ns to 20/25/30 ns t_{OH} (min): 10/10 ns to 5/10/10 ns t_{WC} (min): 70/85 ns to 55/70/85 ns t_{CW} (min): 60/75 ns to 50/60/75 ns t_{AS} (min): 0/0 ns to 0/0/0 ns t_{AW} (min): 60/75 ns to 50/60/75 ns t_{WP} (min): 50/55 ns to 40/50/55 ns t_{WR} (min): 0/0 ns to 0/0/0 ns t_{WHZ} (min): 0/0 ns to 0/0/0 ns t_{WHZ} (max): 25/30 ns to 20/25/30 ns t_{DW} (min): 30/35 ns to 30/30/35 ns t_{DH} (min): 0/0 ns to 0/0/0 ns t_{OW} (min): 5/5 ns to 5/5/5 ns Addition of note 11,12 Low V_{CC} Data Retention Characteristics Deletion of note 2 Addition of note 4,5 t_R min: 5 ms to t_{RC} ns	Y.Saitou	K.Yoshizaki
2.0	Jul. 4, 1995	Low power Standby: 3 μ W (typ) to 2 μ W (typ) Absolute Maximum Ratings Change of note 2 Recommended DC Operating Conditions Change of note 1 DC Characteristics I_{SB} (typ): 0.5 mA to 0.7 mA I_{SB2} (typ): 0.6 μ A to 0.4 μ A	M. Higuchi	K. Yoshizaki

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Revision Record (cont)

Rev.	Date	Contents of Modification	Drawn by	Approved by
2.0	Jul. 4, 1995	Capacitance C _{in} (max): 8 pF to 5 pF C _{I/O} (max): 10 pF to 8 pF Low V _{CC} Data Retention Characteristics I _{CCDR} (typ): 0.5 μA to 0.1 μA Change of note 4 _Addition of Read Timing Waveform 2,3	M. Higuchi	K. Yoshizaki
3.0	Nov. 1997	Change of Subtitle		